PIDS WG: 新構造素子による性能向上に期待

--- Emerging Research Devices ---

(STRJ Workshop)

平本俊郎
東京大学大規模集積システム設計教育研究センター
東京大学生産技術研究所

1. 本章の目的
2. ノンクラシカルCMOS
3. 新メモリデバイス
4. 新ロジックデバイスとアーキテクチャ
5. まとめ

新探究デバイス

目的

RMの延長上あるいはRMを越える新概念の研究・発明を加速

1. マイクロエレクトロニクスの延長上にある技術
   - ・Non-Classical CMOS
   - ・Memory Technology
   - → S値，移動度，IonなどのTr.の特性改善
2. Beyond RM: 全く新しい技術および概念の導入
   - ・ Emerging Logic and Architecture (Non-CMOS)

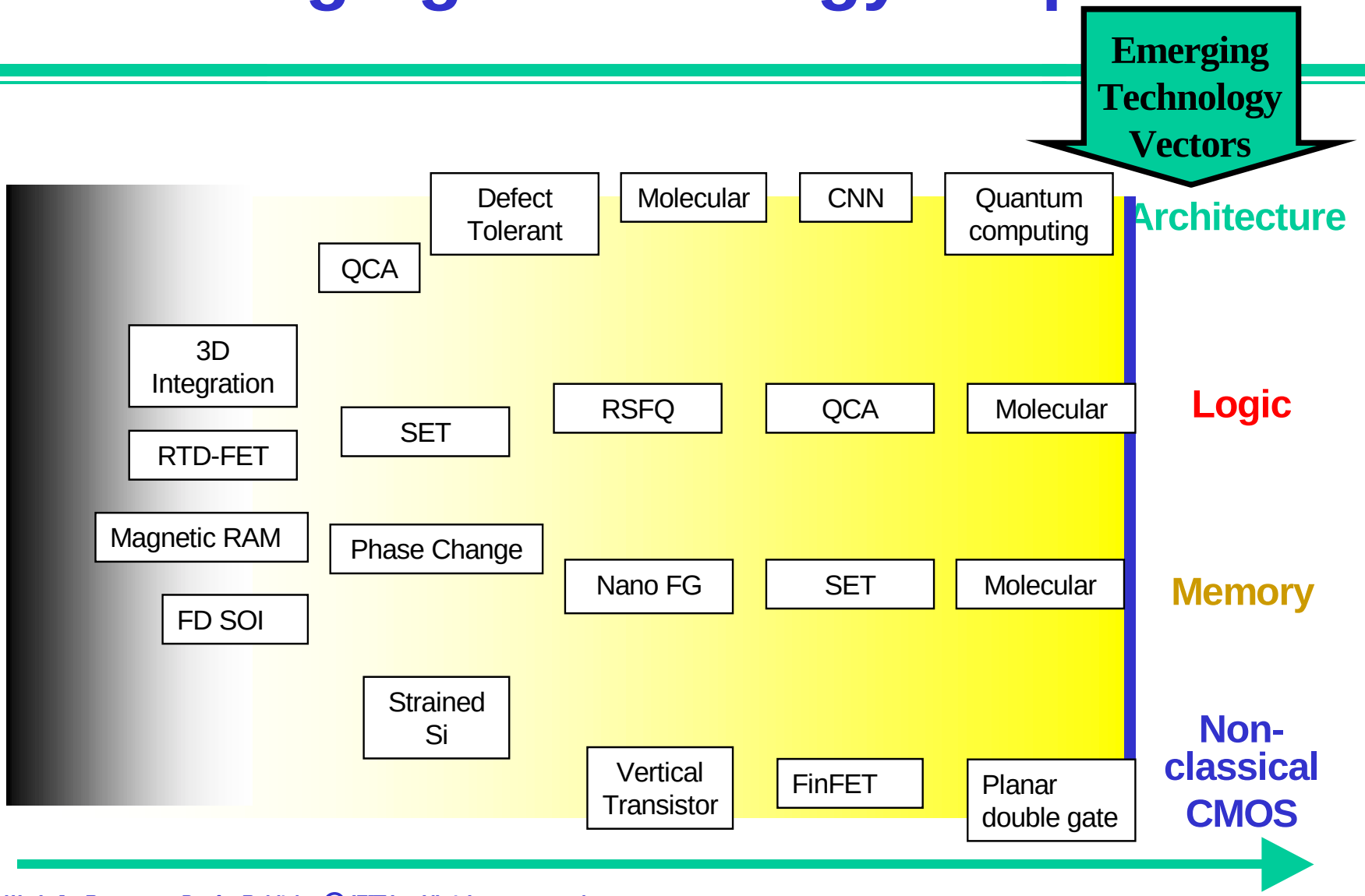
1999年版：PIDS内に表数枚（Beyond CMOS/Novel Devices)

2001年版：Emerging Research Devicesの章（21ページ）

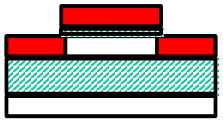
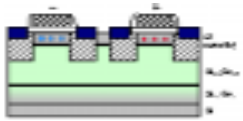
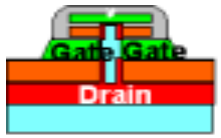
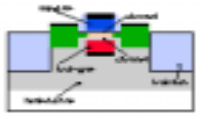
ここに掲載された技術が本命であると保証したわけではない.

ここに掲載されていない新しい技術がでてくる可能性がある.

Emerging Technology Sequence



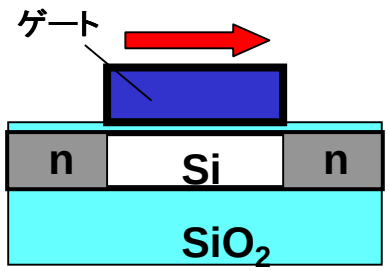
Non-Classical CMOS

					
Device	*Ultra-Thin Body SOI*	*Band-Engineered Transistor*	*Vertical Transistor*	*FinFET*	*Double-Gate Transisto*
Concept	**Fully depleted SOI**	**SiGe or Strained Si channel; bulk Si or SOI**	**Double-gate or surround-gate structure (No specific temporal sequence for these three structures is intended)**		
Application/driver	**Higher performance, Higher transistor density, Lower power dissipation**				
Advantages	**-Improved subthreshold slope –V_t controllability**	**-Higher drive current -Compatible with bulk and SOI CMOS**	**-Higher drive current Lithography independent L_g**	**-Higher drive current -Improved subthreshold slope -Improved short channel effect -Stacked NAND**	**-Higher drive current -Improved subthreshold slope -Improved short channel effect -Stacked NAND**
Scaling Issues	**-Si film thickness -Gate stack -Worse short channel effect than bulk CMOS**	**-High mobility film thickness, in case of SOI -Gate stack -Integration**	**-Si film thickness -Gate stack -Integrability -Process complexity -Accurate TCAD including QM**	**-Si film thickness -Gate stack -Process complexity -Accurate TCAD including QM effect**	**-Gate alignment -Si film thickness -Gate stack -Integrability -Process complexity -Accurate TCAD including QM effect**
Design Challenges	**-Device characterization -Compact model and parameter extraction**	**-Device characterization**	**-Device characterization -PD versus FD -Compact model and parameter extraction -Applicability to mixed signal applications**		
Maturity	**Development**				
Timing	**Near Future** →				

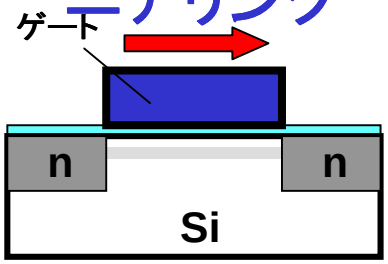
ノンクラシカルCMOS

デバイス

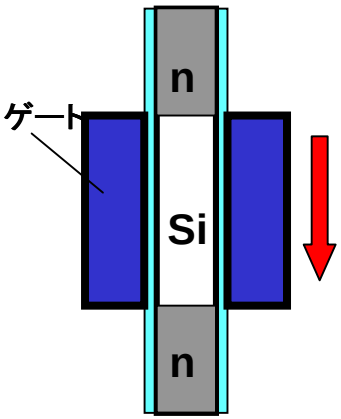
極薄膜SOI



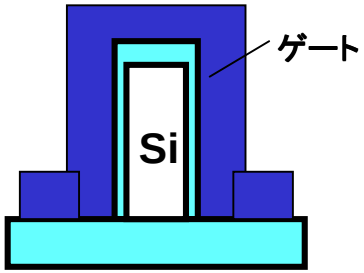
バンドエンジニアリング



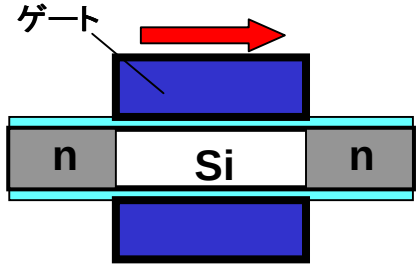
縦型



FinFET



ダブルゲート

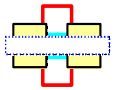
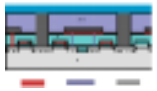
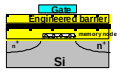


コンセプト

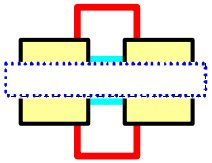
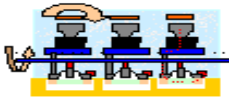
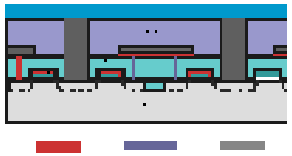
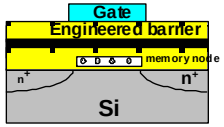
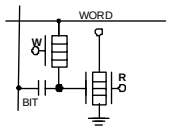
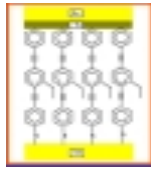
完全空乏型SOI	SiGe, ひずみSi (バルク，SOI)	ダブルゲートまたはサラウンドゲート		
利点	S値	電流駆動力 CMOS互換プロセス	電流駆動力 リソに依存しないLg	電流駆動力 S値 短チャネル効果	電流駆動力 S値 短チャネル効果
課題	SOI膜厚 ゲート電極	薄膜の膜厚 ゲート電極	ゲート電極 複雑なプロセス	ゲート電極 複雑なプロセス	上下ゲート整合 SOI膜厚など

→ 電子の流れ

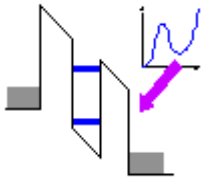
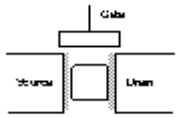
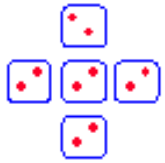
Emerging Research Memory Devices

Storage Mechanism	Baseline 2002 Technologies		Magnetic RAM		Phase Change Memory	Nano Floating Gate Memory	Single/Few Electron Memories	Molecular Memories
								
Device Types	DRAM	NOR Flash	Pseudo-Spin-Valve	Magnetic Tunnel Junction	OUM	-Engineered Tunnel Barrier -Nanocrystal	SET	-Bistable switch -Molecular NEMS -Spin based molecular devices
Availability	2002		~2004	~2004	~2004	>2005	>2007	>2010
Initial F Value	130 nm	150 nm	350 nm	130 nm	100 nm	80 nm	65 nm	45 nm
Cell Size	$8F^2$ 0.14 μm^2 1T	$10F^2$ 0.19 μm^2 1T	~$40F^2$ 4.9 μm^2 2T	$20–40F^2$ 0.68 μm^2 2T	$6F^2$ 0.06 μm^2 1T	$4–10F^2$ 0.04 μm^2	$4–9F^2$ ~0.04 μm^2	~$2F^2$ 0.004 μm^2
Access Time	<20 ns	~80 ns	<25 ns	<10 ns	<100 ns	<10 ns	<10ns	~10 ns
Store Time	<20 ns	~1 ms	<25 ns	<10 ns	<100ns	<10 ns	<100 ns	~10 ns
Retention	64 ms	>10 yrs	>10 yrs	>10 yrs	>10 yrs	>10 yrs	Seconds to minutes[1]	Days
E/W Cycles	Infinite	>1E5	>1E15	>1E13	>1E13	>1E6	>1E9	>1E15
General Advantages	Density Economy	Non-volatile	Non-volatile, High endurance, Fast read and write, Radiation hard, NDRO		Non-volatile, Low power, NDRO, Radiation hard	Non-volatile, Fast read and write	Density Power	Density, Power Identical Switches, Larger I/O difference, Opportunities for 3D easier to interconnect defect tolerant circuitry
Challenges	Scaling	Scaling	Integration issues, Material quality, Control magnetic properties for write operations		New materials and integration	Material Quality	Dimensional Control (Room temperature operation), Background Charge	Volatile Thermal Stability
Maturity	Production		Development		Development	Demonstrated	Demonstrated	Demonstrated

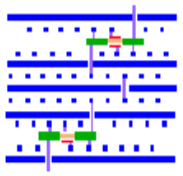
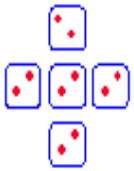
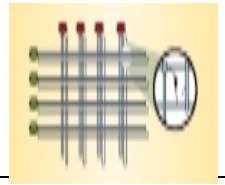
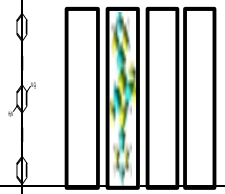
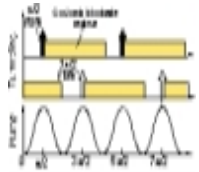
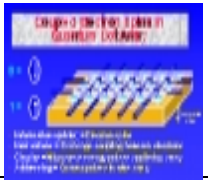
新メモリデバイス

記憶メカニズム	MRAM		相変化メモリ	ナノ浮遊ゲートメモリ	単電子・少数電子メモリ	分子メモリ
						
デバイスタイプ	巨大磁気抵抗	磁気トンネル接合	OUM	トンネルバリア ナノクリスタル	SET	分子MEMS 双安定スイッチ
導入時期	- 2004		- 2004	> 2005	> 2007	> 2010
導入時期	不揮発性 高速 Endurance 非破壊読出し		不揮発性 低消費電力 非破壊読出し	不揮発性 高速	高集積 消費電力	高集積，電力 3D集積, Defect Tolerannt

Emerging Logic Devices

						
Device	*Resonant Tunneling Diode – FET*	*Single Electron Transistor*	*Rapid Single Quantum Flux Logic*	*Quantum Cellular Automata*	*Nanotube Devices*	*Molecular Devices*
Types	**3-terminal**	**3-terminal**	**Josephson Junction +inductance loop**	**-Electronic QCA -Magnetic QCA**	**FET**	**2-terminal and 3-terminal**
Advantages	**Density, Performance, RF**	**Density, Power, Function**	**High speed, Potentially robust, (insensitive to timing error)**	**High functional density, No interconnect in signal path, Fast and low power**	**Density, Power**	**Identity of individual switches (e.g., size, properties) on sub-nm level. Potential solution to interconnect problem**
Challenges	**Matching of device properties across wafer**	**New device and system, Dimensional control (e.g., room temp operation), Noise (offset charge), Lack of drive current**	**Low temperatures, Fabrication of complex, dense circuitry**	**Limited fan out, Dimensional control (room temperature operation), Architecture, Feedback from devices, Background charge**	**New device and system, Difficult route for fabricating complex circuitry**	**Thermal and environmental stability, Two terminal devices, Need for new architectures**
Maturity	**Demonstrated**	**Demonstrated**	**Demonstrated**	**Demonstrated**	**Demonstrated**	**Demonstrated**

Emerging Research Architecture

						
Architecture	*3-D Integration*	*Quantum Cellular Automata*	*Defect Tolerant Architecture*	*Molecular Architecture*	*Cellular Nonlinear Networks*	*Quantum Computing*
Device Implementation	**CMOS with dissimilar material systems**	**Arrays of quantum dots**	**Intelligently assembles nanodevices**	**Molecular switches and memories**	**Single electron array architectures**	**Spin resonance transistors, NMR devices, Single flux quantum devices**
Advantages	**Less interconnect delay, Enables mixed technology solutions**	**High functional density. No interconnects in signal path**	**Supports hardware with defect densities >50%**	**Supports memory based computing**	**Enables utilization of single electron devices at room temperature**	**Exponential performance scaling, Enables unbreakable cryptography**
Challenges	**Heat removal, No design tools, Difficult test and measurement**	**Limited fan out, Dimensional control (low temperature operation), Sensitive to background charge**	**Requires pre-computing test**	**Limited functionality**	**Subject to background noise, Tight tolerances**	**Extreme application limitation, Extreme technology**
Maturity	**Demonstration**	**Demonstration**	**Demonstration**	**Concept**	**Demonstration**	**Concept**

新ロジックデバイスとアーキテクチャ

新ロジックデバイス

共鳴トンネルFET，単電子トランジスタ，単一量子磁束，

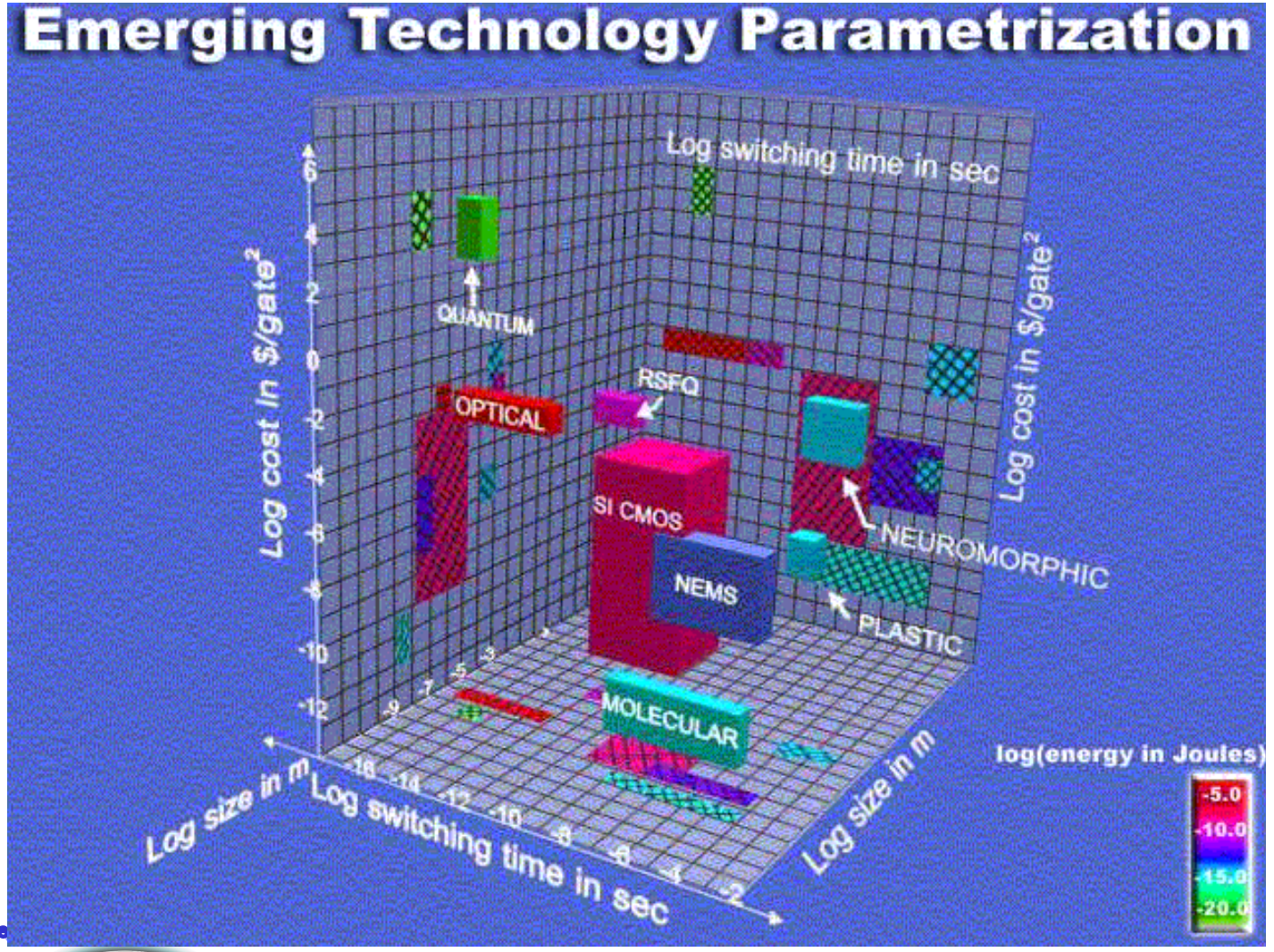
量子セルオートマトン，分子デバイス

新アーキテクチャ

三次元集積，量子セルラオートマタ，Defect Tolerant，

分子アーキテクチャ，非線形セルラネットワーク，量子計算

新探究技術パラメータ分析



Work-In-Progress

新探究デバイスのまとめ

1．ロードマップの延長線上で性能向上を加速させる技術

・ノンクラシカルCMOS

・新メモリデバイス

2．ロードマップを越える新しい技術・概念

・新ロジックデバイス

・新アーキテクチャ