65nmを実現するための新計測技術

Metrology WG (WG11)

・三菱電機　池野昌彦

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Metrology Roadmap 2001 Update

Europe	**Alain Deleporte (ST)**	**4/01**
	Alec Reader (Philips Analytical)	
	Vincent Vachellerie (ST)	**4/01**
	Mauro Vascone (ST)	
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	Bob Scace (Klaros Corporation)	
	Jack Martinez (NIST)	
	Alain Diebold (Int. SEMATECH)	

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SCOPE

- Microscopy
- Control of Statistical Processes
- Lithography Metrology
- FEP Metrology
- Interconnect Metrology
- Materials and Contamination Metrology
- Integrated Metrology
- Standards and Reference Materials

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GAPS in FAB Ready Metrology

- **3D CD for Mask and Wafer for lines and contact/via and long term capability for CD**
- **Optical and Electrical Metrology that controls high k plus interface**
- **Void detection in copper Lines**
- **Killer Pores in low k**
- **Sidewall barrier layer control below seed Cu**

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Difficult Challenges before 65 nm / 2007

- **Factory level and company-wide metrology integration**
- **Impurity detection (especially particles) at levels of interest for starting materials & reduced edge exclusion for metrology tools.**
- **Control of high-aspect ratio technologies such as Damascene challenges all metrology methods. *Key requirements are void detection in copper lines and pore size distribution in patterned low k.***

Add

- **Measurement of complex material stacks and interfacial properties including physical and electrical properties.**
- ***Measurement test structures and reference materials.***

New

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Difficult Challenges after 65 nm / 2007

- **Nondestructive, production worthy wafer and mask level microscopy for critical dimension measurement for 3-D structures, overlay, defect detection, and analysis.**

- **Standard electrical test methods for reliability of new materials, such as ultra-thin gate and capacitor dielectric materials, are not available.**

- **Statistical limits of sub-65 nm process control.**

- **3D dopant profiling.**

- ***Determination of manufacturing Metrology when device and interconnect technology remain undefined.***

New

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GAPS in Litho Metrology

Technology Node	*130 nm*	*90nm*	*65 nm*	*45 nm*	*32 nm*	*22 nm*	*Driver*
Lithography Metrology							
Wafer Gate CD nm post-etch contol	**6.5**	**3.7**	**2.5**	**1.8**	**1.3**	**0.9**	**MPU**
Wafer CD Tool 3σ Precision P/T=0.2 Isolated Lines	**1.3**	**0.75**	**0.5**	**0.36**	**0.26**	**0.18**	**MPU**
Line Edge Roughness (nm)	**4.5**	**2.7**	**1.8**	**1.3**	**0.9**	**0.65**	**MPU**
Overlay Control (nm) (mean +3σ)	**45**	**31**	**26**	**18**	**13**	**9**	**MPU**
Overlay Metrology Precision (nm) P/T=0.1	**4.5**	**3.1**	**2.6**	**1.8**	**1.3**	**0.9**	**MPU**

- **Precision of CD-SEM**
- **Proof of 3D CD for Tilt Beam CD-SEM**
- **Commercialization of 3D software for top-down CD-SEM**
- **Depth of Field Issues for CD-SEM**
- **Reference Materials for 65 nm node and below**
- **Standard method for Precision of Discrete CD Library**
- **Probe Tip Technology for CD-AFM**

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Changes to Lithography Metrology

- **Accelerated MPU Gate Length dilutes advances in CD Measurement**
  - **Will 15% Process 3σ be adopted??**
- **Addition of Line Edge Roughness Metrics**
- **Overlay may face difficulties associated with mixing exposure tools**
  - **e.g., 2 different 157 nm exposure tools for via & metal trench (or 157 nm for lines & Electron Projection for Via)**

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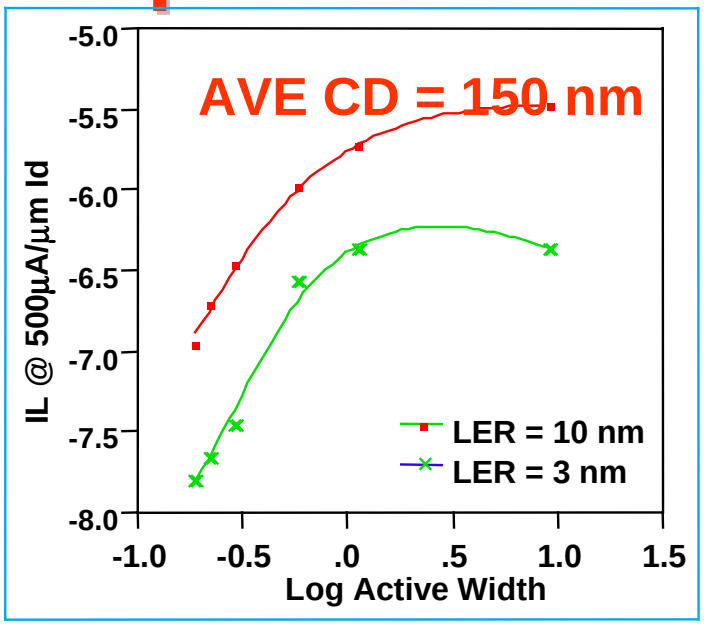
Line Edge Roughness Requirements

Line Edge Roughness Correlated to Leakage Current Increase

Patterson, et. al., SPIE 2001



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Lithography Metrology							
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Line Edge Roughness (nm)	**4.5**	**2.7**	**1.8**	**1.3**	**0.9**	**0.65**	**MPU**
Line Edge Roughness Precision 3σ (nm)	**0.9**	**0.54**	**0.36**	**0.26**	**0.18**	**0.13**	**MPU**

Thanks to ITRS Litho TWG - Harry Levinson / Mauro Vasconi

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Why are CD Measurement Requirements RED?

- **There is no universal metrology solution for all CD measurements.**
  - **e.g., Scatterometry meets Focus-Exposure precision needs to (70 nm node?) for resist lines but not for contacts (yet).**
  - **Can Scatterometry measure LER ?**
- **3D info needed for undercut gate, contact, and other structures.**
- **Precision includes tool matching and near + long term measurement variation.**

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Gaps in FEP Metrology

Technology Node	*130 nm*	*90nm*	*65 nm*	*45 nm*	*32 nm*	*22 nm*	*Driver*
Front End Processes Metrology							
Logic Dielectric Thick Precision 3σ (nm)	0.005	0.004	0.0024	0.0024	0.0016	0.0016	MPU
Metrology for Ultra-Shallow Junctions at Channel Xj (nm)	26	14.8	10	7.2	5.2	3.6	MPU

- **Physical Metrology for high k gate stack**
  - **Optical Models for next High k (beyond ZrO2 and HfO2)**
  - **Commercial availability of high k optical model in software**
  - **Interfacial control for interface between high k and silicon**
- **Electrical Metrology for high k gate stack**
  - **Application of Non-contact C-V to next High k (beyond ZrO2 and HfO2)**
  - **Comparison of non-contact electrical to C-V**
  - **USJ Metrology**
- **Ultra Shallow Junction Metrology (USJ)**
  - **Dose/Junction Control**
  - **2D Dopant Profiling with spatial resolution**
- **Metrology for post CMOS**
  - **SOI ; SiGe ; Vertical Transistors**

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FEP Metrology

- **Optical and Electrical measurement of High κ can be done for development but needs to be robust for manufacturing**
- **Metrology for interface below High κ needs R&D**
- **USJ Metrology needs development for < 65 nm**
- **FERAM needs fatigue testing for 10^{16} read/write cycles**

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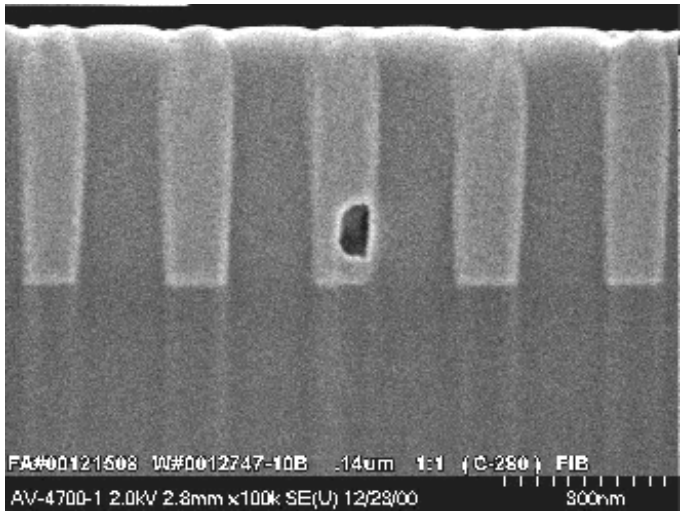
Gaps in Interconnect Metrology

Technology Node	*130 nm*	*90nm*	*65 nm*	*45 nm*	*32 nm*	*22 nm*	*Driver*
Interconnect Metrology							
Barrier layer thick (nm) process range (±3 ϑ Precision 1σ (nm)	18 10% 0.06	11 10% 0.04	8 10% 0.03	7 10% 0.02	5 10% 0.017	4 10% 0.013	MPU
Void Size for 1% Voiding in Cu Lines	32.5	22.5	16.25	11.25	8	5.5	MPU
Detection of Killer Pores at (nm) size	6.5	4.5	3.25	2.25	1.6	1.1	MPU

- **VOID Detection in Copper lines**
- **Killer Pore Detection in Low κ**
- **Barrier / Seed Cu on sidewalls**
- **Control of each new Low κ**



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Interconnect Metrology

- **Random isolated void detection (size of 25% of line width) at < 1% in copper lines may not be measurable in-line**
- **Max Low κ Pore size of 5% of line width**
- **Metrology for electrochemical deposition will be included in Metrology Roadmap**

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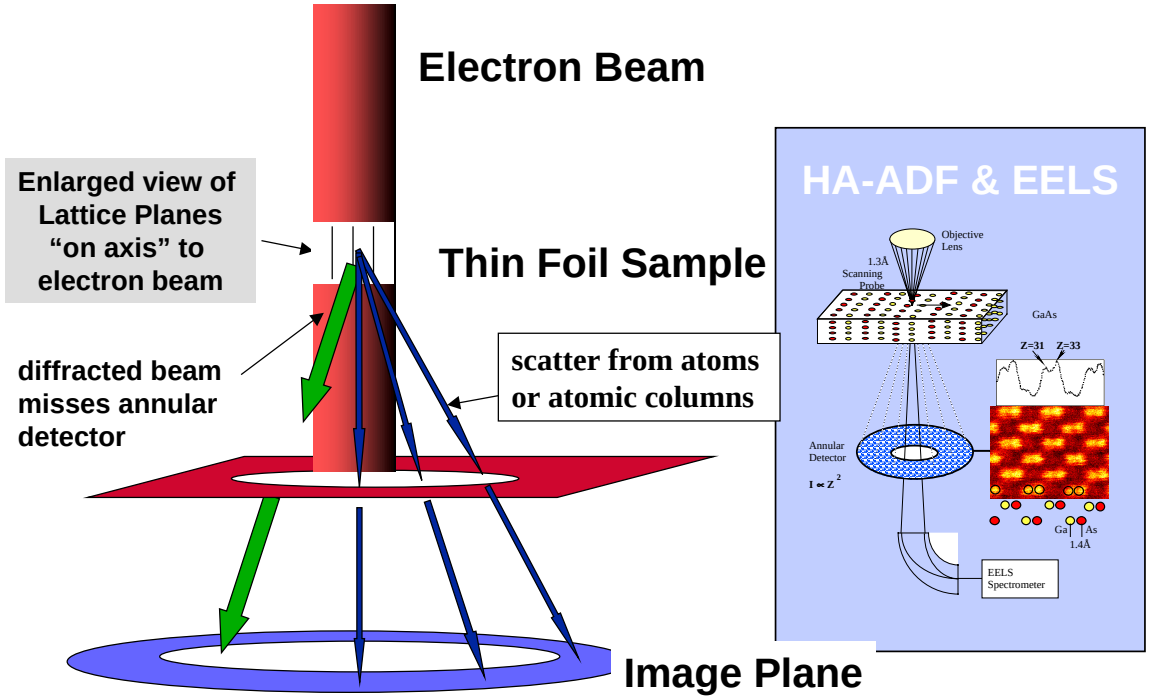
Materials Characterization Enables Process and Metrology Development

Short term: New Aberration Corrected Lens for STEM/TEM
Long Term: Atom Probe

High Angle - Annular Dark Field STEM



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2001 Grand Challenges

- **Development of Metrology tools in time.**
- **Rapid non-destructive metrology for CD, overlay, defect detection and line edge roughness that meets ITRS timing and technology requirements.**

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