2002年度WG4/Interconnect ITWG活動

1．2002年度の活動概要（ITRS関連）
2．トピックス：　ITRS2002update
3．2003年度の課題

WG4（配線技術）主査
（株）半導体先端テクノロジーズ
小川　真一

2002年度の活動概要（ITRS関連）

ITWG	WG4
4/16-17　Erlangen 検討項目 ・k低減加速なし（合意） ・信頼性見直し（Japan） ・ｸﾞﾛｰﾊﾞﾙ見直し（Infineon） ・新性能指標（IMEC） **7/23-24　San-Francisco** ・2002年度は大きな見直しなし ・ｸﾞﾛｰﾊﾞﾙ配線のﾋﾟｯﾁに範囲追加 ・RCdelayの指標追加 ・Jmax値の見直し ・Cu/Low-kの信頼性課題を強調 **12/3-4　Tokyo** ・2003年度へ向けた課題等	事前ミーティング（3/27） 国内検討 電流密度 リーク電流etc

ITWG Regional Chairs

Japan
- Shinichi Ogawa
- Akihiko Ohsaki

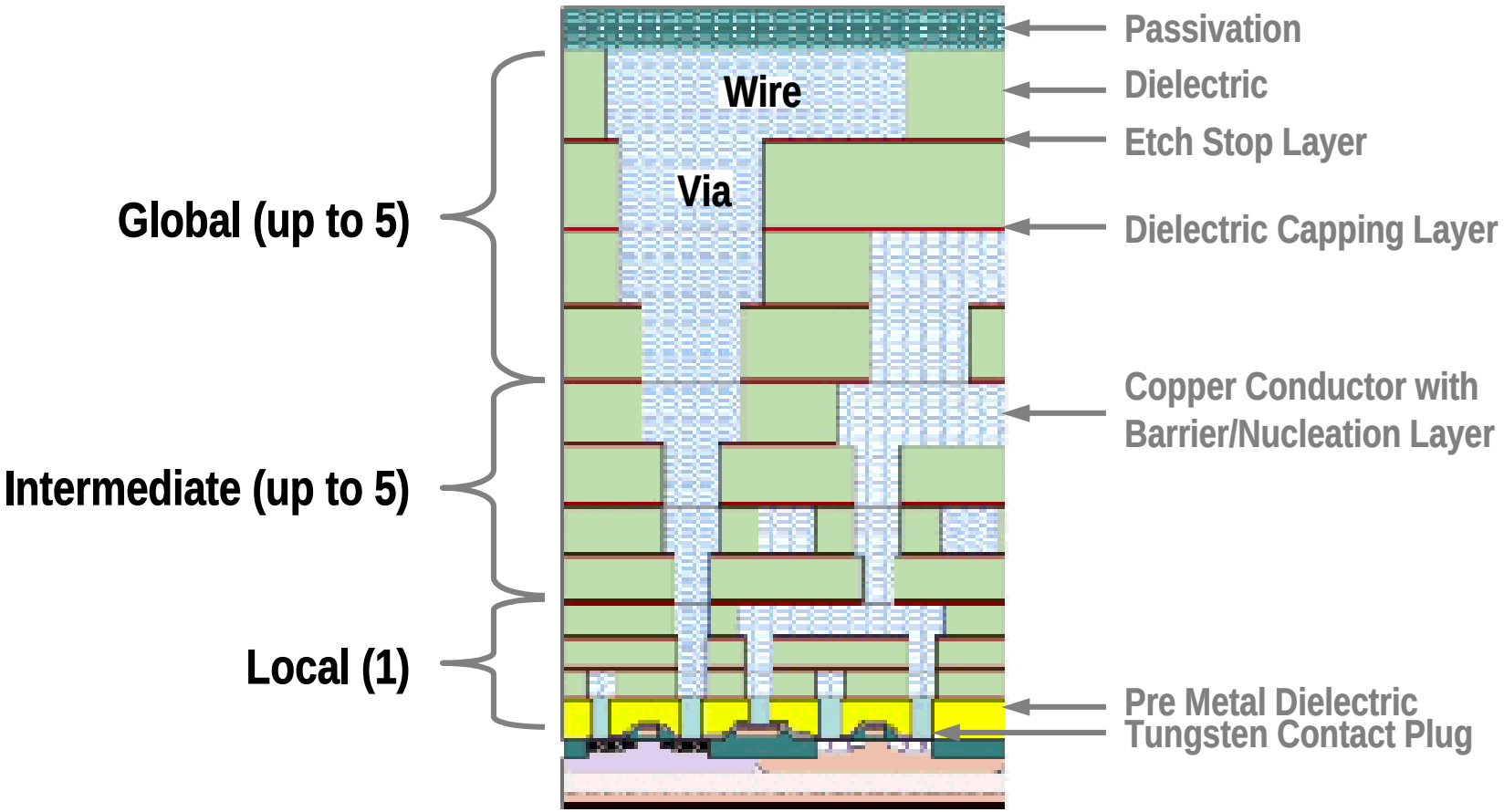
Taiwan
- Calvin Hsueh
- Shin-Puu Jeng

Korea
- Hyeon-Deok Lee
- Hyun Chul Sohn

US
- Robert Geffken
- Christopher Case

Europe
- Hans Joachim-Barth
- Joachim Torres

Typical chip cross-section illustrating hierarchical scaling methodology



2002 highlights

- No significant changes
  - No changes to timing
  - No changes to number of metal levels
  - No changes to low k dielectric roadmap
- New wiring performance metrics
- Updated Jmax/Imax
- Clarification of global wiring pitch
- Increased emphasis on reliability issues associated with Cu/low k integration

MPU HP Near Term Years

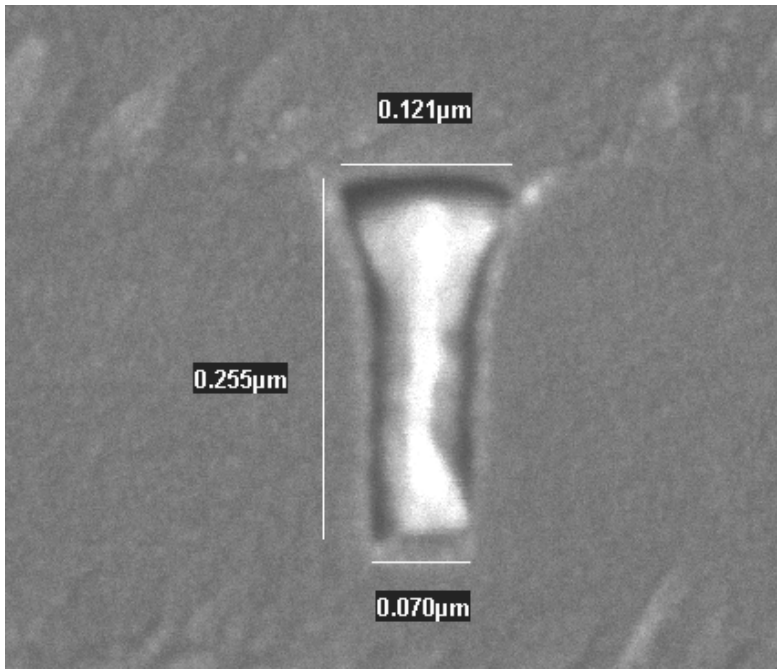
YEAR / *TECHNOLOGY NODE*	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM ½ PITCH (nm) (SC. 2.0)	*130*	*115*	*100*	*90*	*80*	*70*	*65*
MPU/ASIC ½ PITCH (nm) (SC. 3.7)	*150*	*130*	*107*	*90*	*80*	*70*	*65*
MPU PRINTED GATE LENGTH (nm) (SC. 3.7)	*90*	*75*	*65*	*53*	*45*	*40*	*35*
MPU PHYSICAL GATE LENGTH (nm) (SC. 3.7)	*65*	*53*	*45*	*37*	*32*	*28*	*25*
Conductor effective resistivity (μΩ-cm) Cu intermediate wiring*	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**	**2.2**
Barrier/cladding thickness (for Cu intermediate wiring) (nm)	**16**	**14**	**12**	**10**	**9**	**8**	**7**
Interlevel metal insulator —effective dielectric constant (κ)	**3.0-3.6**	**3.0–3.6**	**3.0-3.6**	**2.6–3.1**	**2.6–3.1**	**2.6–3.1**	**2.3–2.7**
Interlevel metal insulator (minimum expected) —bulk dielectric constant (κ)	**<2.7**	**<2.7**	**<2.7**	**<2.4**	**<2.4**	**<2.4**	**<2.1**

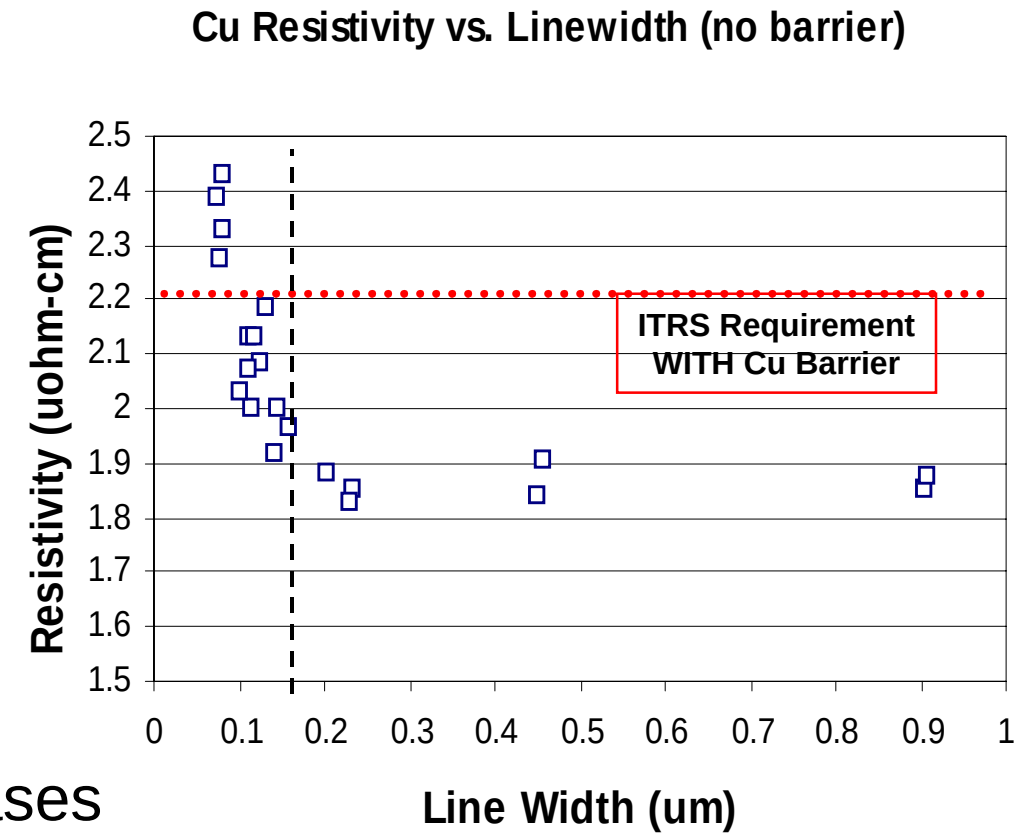
Bulk and effective dielectric constants described

Unchanged from 2001 – differing views

Cu at all nodes - conformal barriers

Effect Of Line Width On Cu Resistivity





Conductor resistivity increases

expected to appear around 100 nm linewidth -

will impact intermediate wiring first - ~ 2006

Courtesy of SEMATECH

MPU HP Near Term Years

YEAR TECHNOLOGY NODE	2001	2002	2003	2004	2005	2006	2007
DRAM ½ PITCH (nm) (SC. 2.0)	130	115	100	90	80	70	65
MPU/ASIC ½ PITCH (nm) (SC. 3.7)	150	130	107	90	80	70	65
Local wiring pitch (nm)	350	295	245	210	185	170	150
*Interconnect RC delay 1 mm line (ps) [3]	86	121	176	198	256	303	342
*Line length where τ = RC delay (μm)	137	106	80	70	57	50	44
Minimum global wiring pitch (nm)	670	565	475	460	360	320	290
Ratio (global wiring pitch/intermediate wiring pitch)	1.5 - 5.0	1.5 - 5.0	1.5 - 5.0	1.5- 6.7	1.5 - 6.7	1.5 - 6.7	1.5 - 8.0

New RC delay metric for a 1 mm line (level dependent)

Ratio of global wiring pitch to semi-global wiring pitch

Reliability Challenges

- Short term
  - Electrical, thermal and mechanical exposure
  - New failure mechanisms with Cu/low k present significant challenges before volume production
    - interface diffusion
    - interface delamination
  - Higher intrinsic and interface leakage in low k
  - Need for new failure detection methodology to establish predictive models

Dimensional Control

- 3D CD of features
  - performance and reliability implications
- Void detection in Cu wires
- Multiple levels
  - reduced feature size, new materials and pattern dependent processes
  - process interactions
    - CMP and deposition - dishing/erosion - thinning
    - Deposition and etch - to pattern multi-layer dielectrics
- Aspect ratios for etch and fill
  - particularly DRAM contacts and dual damascene

Process Integration

- Combinations and interactions of new materials and technologies
  - interfaces, contamination, adhesion, diffusion, leakage concerns, thermal budget, ESH, CoO
- Structural complexity
  - levels - interconnect, ground planes, decoupling caps
  - passive elements
  - mechanical integrity
  - other SOC interconnect design needs (RF)
  - cycle time

Solutions beyond Cu and low κ

- Material innovation combined with traditional scaling will no longer satisfy performance requirements
  - Design, packaging and interconnect innovation needed
  - Alternate signal transmission media
    - optical, RF
  - Emerging devices (3D or multi-level) in the interconnect

Last words

- Continued rapid changes in materials
- Develop solutions for emerging devices
- Must manage 3D CD
- System level solutions must be accelerated to address the global wiring grand challenge
  - Cu resistivity increase impact appears ~2006
  - materials solutions alone cannot deliver performance - end of traditional scaling
  - integrated approach with design and packaging

2003年度の課題/予定

● 2003 ITRSでの検討予定課題

- Low-kの今後についてどうするか？
  - ・現実のデバイスでのEffective k 値の再調査
  - ・信頼性上の問題による困難さと、要求値との整合をどう取るか？

- Emerging Devicesにおける配線
  - ・Emerging Devicesにおける配線への要求は？
  - ・Cu/Low-kの限界を超える方策は？