2002年度YE（歩留改善）STRJ 活動報告

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内容

- 装置許容欠陥数
- Invisible Defect
- 2002 ITRS Update
- In-line FA
- まとめ

セマッテクの新しい装置欠陥モデルソフト

RDLY 100 nm Model.lnk

area[iii]. This derivation assumes long parallel lines (runners) of minimum width and spacing. It also assumes the $1/x^3$ defect size distribution (See the next section.)

$$Ac = \frac{LHx_d^2}{2w(H+w)}$$

If we assume that the total area of the integrated circuit is covered by lines of equal width and space, the above expression simplifies to:

$$Ac = A\frac{Xd^2}{2L\min(L\min + P\min)}$$

Tool Group List

Define Tool List | **Geometries & Critical Areas** | PWP Data | PID Data | Elec Data

Minimum Device Geometry (nm) *

Tool	Xd Calc.	Xd	L min	P min Calc.	P min	Ac Calc.	Ac, Critical Area (cm2)	Kr, Kill Ratio	Tc, Trans.
(5) Starting Wafer Quality	☑	35.0	70.0	☐	260.0	☑	0.04932	1.000	0.830
(10) CD Metrology	☑	35.0	70.0	☐	260.0	☑	0.04932	1.000	0.830
(20) CMP Clean	☑	65.0	130.0	☐	265.0	☑	0.07652	1.000	0.830
(30) CMP Dielectric	☑	70.0	140.0	☑	280.0	☑	0.07750	1.000	0.830
(40) CMP Metal	☑	65.0	130.0	☐	265.0	☑	0.07652	1.000	0.830
(50) CVD Dielectric	☑	70.0	140.0	☑	280.0	☑	0.07750	1.000	0.830
(60) Dielectric SOG	☑	65.0	130.0	☐	265.0	☑	0.07652	1.000	0.830
(70) Electrical Test	☑	65.0	130.0	☐	265.0	☑	0.07652	1.000	0.830
(80) Film Thickness Metrology	☑	35.0	70.0	☐	260.0	☑	0.04932	1.000	0.830
(90) Furnace CVD	☑	65.0	130.0	☐	265.0	☑	0.07652	1.000	0.830
(100) Furnace Oxide/Anneal	☑	35.0	70.0	☐	260.0	☑	0.04932	1.000	0.830
(110) Implant High Current	☑	35.0	70.0	☐	260.0	☑	0.04932	1.000	0.830
(120) Implant Low/Med Current	☑	230.0	460.0	☑	920.0	☑	0.07750	1.000	0.830
(130) Litho Cell	☑	35.0	70.0	☐	260.0	☑	0.04932	1.000	0.830
(140) Metal CVD	☑	65.0	130.0	☐	265.0	☑	0.07652	1.000	0.830
(150) Metal Electroplate	☑	65.0	130.0	☐	265.0	☑	0.07652	1.000	0.830
(160) Metal Etch	☑	230.0	460.0	☑	920.0	☑	0.07750	1.000	0.830
(170) Metal PVD	☑	55.0	110.0	☐	265.0	☑	0.06820	1.000	0.830
(180) Optical Inspection	☑	35.0	70.0	☐	260.0	☑	0.04932	1.000	0.830
(190) Overlay Metrology	☑	35.0	70.0	☐	260.0	☑	0.04932	1.000	0.830
(200) Plasma Etch	☑	35.0	70.0	☐	260.0	☑	0.04932	1.000	0.830
(210) Plasma Resist Strip	☑	35.0	70.0	☐	260.0	☑	0.04932	1.000	0.830
(220) RTP Anneal	☑	35.0	70.0	☐	260.0	☑	0.04932	1.000	0.830
(230) SEM Inspection	☑	65.0	130.0	☐	265.0	☑	0.07652	1.000	0.830
(240) Wafer Read/Sort/Sleuth	☑	35.0	70.0	☐	265.0	☑	0.04858	1.000	0.830
(250) Wafer Transport and Stock	☑	35.0	70.0	☐	265.0	☑	0.04858	1.000	0.830
(260) Wet Bench	☑	35.0	70.0	☐	260.0	☑	0.04932	1.000	0.830

* Xd = min. critical defect size, L min = min. line or space width, P min = mininum pitch

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ISSM'02

Defect Budget Trend Model for Future Device Manufacturing

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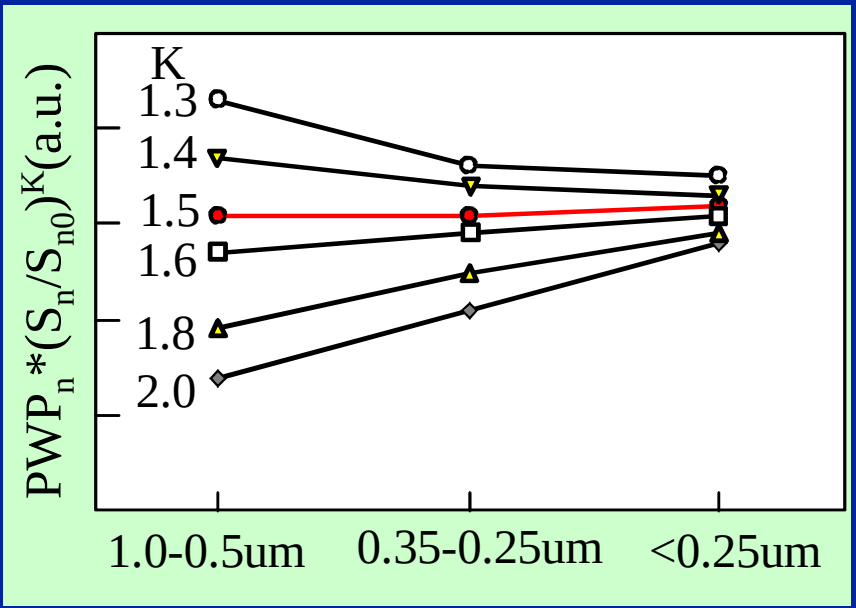
Average Defect Budget Number

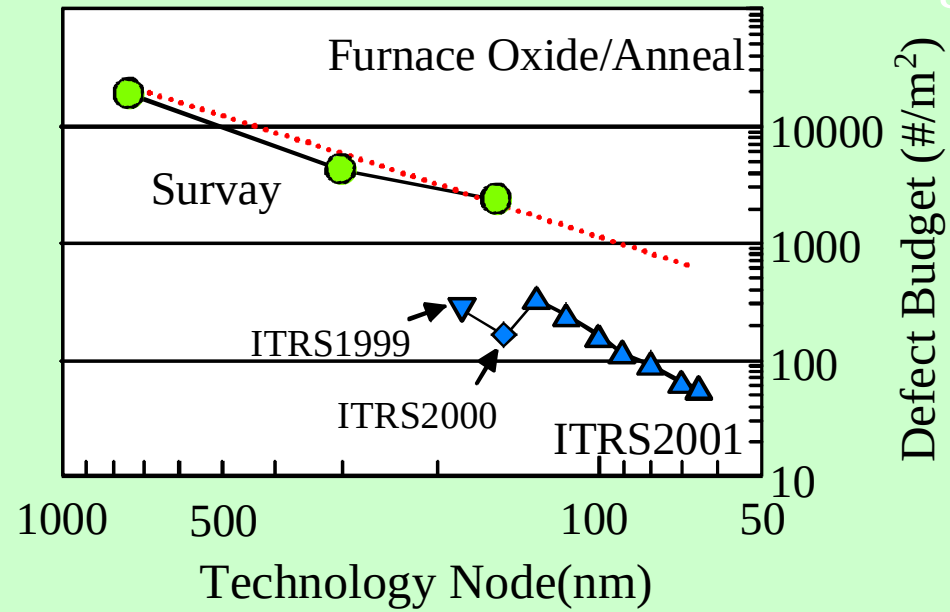
Design rule	750nm (1.0-0.5um)	300nm (0.35-0.25um)	155nm (0.18-0.13um)
Defect budget(m^{-2})	24121	4771	1988
Ratio to ITRS	1.4	1.8	2.1

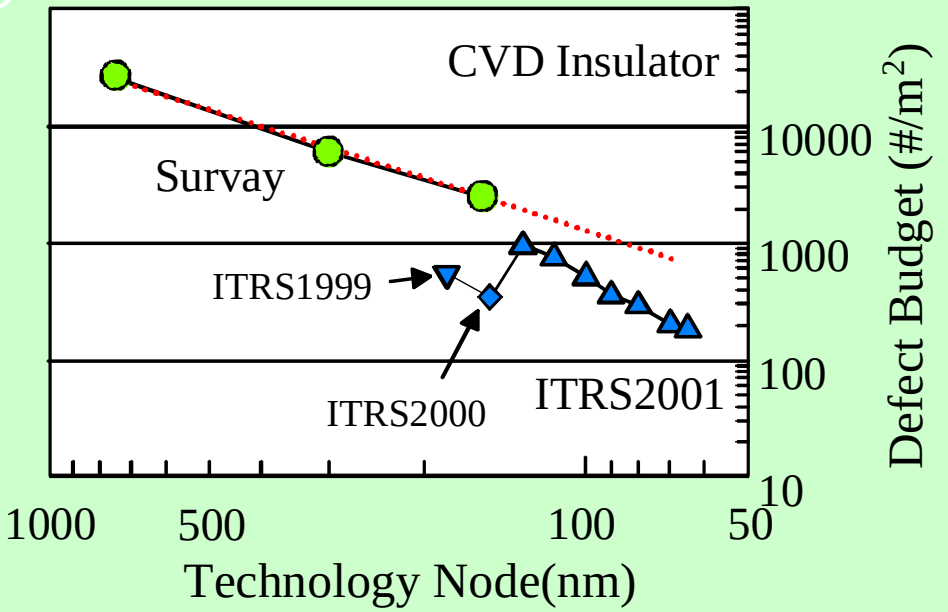
Modification using K value

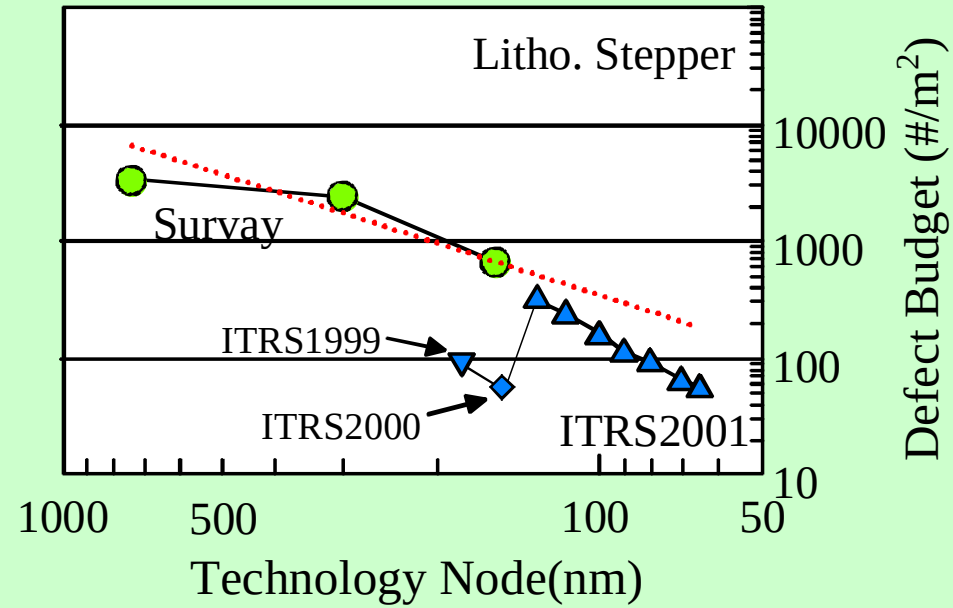
$$PWP_n = PWP_{n0} * \frac{F_n}{F_{n0}\left(S_n / S_{n0}\right)^K}$$

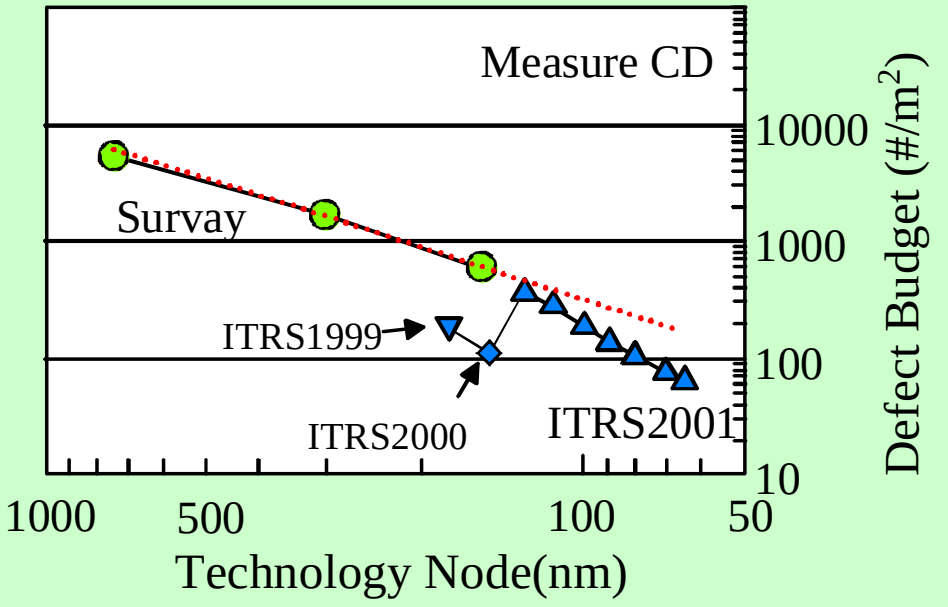


Defect Budget Trend









Invisible Defect

Type of Defect	Phenomena	Module	Probable cause
DRAM Data retention	Leak	Many area	Capacity Leak, Sub leak, TR leak
Silicide Abnormality	High resistivity	Transistor	Thinning?
High dose Extension Defect	High resistivity /Opening	Transistor	Over etching/washout
Gate Leak	Leak	Transistor	Gate Oxide cause /edge cause
SRAM Data retention	High Resistivity Data inversion	Transistor	Load TR Ids decrease, or Load high-R
FLASH Data retention	Leak	Transistor	Charge Recombination
FLASH deplete error	Characteristic	Transistor	Vth over decrease
Kink	Characteristic	Transistor	Vg-Ids characteristic Abnormality
Halo profile Abnormality	Characteristic	Transistor	Short Channel effect appears
Vth shift	Vth shift	Transistor	ESD, or Plasma damage
Worm hole Defect	High resistivity /Opening	Wiring	Substrate damage owing to WF6 reaction
Via Peeling	High resistivity /Opening	Wiring	Excess Stress
Short in Porous ILD	Short/Leak	Wiring	Excess Coverage of Barrier Metal
TDDB Defect in Porous ILD	Leak	Wiring	Poor Coverage of Barrier Metal
Memory Disturb	Data inversion	Wiring	EMI,electro-magnetic interference
Void	Open	Wiring	Void migration/creation

ITRS Conference
December 3 - 4, 2002
Tokyo, Japan

ITRS 2002 Yield Enhancement (YE) Update

Presenters: Toshihiko Osada (Fujitsu) and
Fred Lakhani (International Sematech)

International Technology Roadmap for Semiconductors ITRS

2002 ITRS YE ITWG Co-chairs

- **Europe**
  - Ines Thurner
    - Infineon
- **Japan**
  - Toshihiko Osada
    - Fujitsu
  - Hiroshi Kitajima
    - Selete
- **Korea**
  - TBD
- **Taiwan**
  - Len Mei
    - Promos Technologies
- **United States**
  - Christopher Long
    - IBM
  - Fred Lakhani
    - International Sematech

YE Difficult Challenges

- ***High-Aspect-Ratio Inspection*.**
  - High-speed, cost-effective tools are needed to rapidly detect defects at 1/2 X ground rule (GR) associated with high-aspect-ratio contacts, vias, and trenches and especially defects near or at the bottoms of these features.
- ***Non-visual Defect Detection***
  - In-line and end-of-line tools and techniques are needed to detect non-visual defects.
- ***Data Management for Rapid Yield Learning.***
  - Automated, intelligent analysis and reduction algorithms that correlate facility, design, process, test, and work-in-process (WIP) data must be developed to enable the rapid root-cause analysis of yield-limiting conditions.

YE Difficult Challenges (continue)

- ***Design for Manufacture & Test (DFM & DFT) and Systematic Mechanisms Limited Yield (SMLY)***
  - IC designs must be optimized for a given process capability and must be testable and diagnosable. Understanding SMLY is mandatory for achieving historic yield ramps in the future.
- ***Yield Models***
  - Random, systematic, parametric, and memory redundancy models must be developed and validated to correlate process-induced defects (PID), particle counts per wafer pass (PWP), and *in-situ* tool/process measurements to yield.
- ***Correlation of Impurity Level to Yield.***
  - Test structures and methods are needed for correlating fluid/gas contamination types and levels to yield.

Key Changes in 2002 Electronic Update

- For the Defect Detection & Characterization (DDC) section, table changes were made to either correct typing errors or make technology requirements consistent with the rest of the roadmap.
- For the Yield Learning (YL) section, table changes were made to reflect the following assumption changes:
  - **The inspection sampling rate during yield ramp was changed from 20% to 10%**
  - **The cycle time per mask level was changed from 1 day to 1.5 days**
  - **Time to source new yield detractors was changed from 0.5X cycle time to 1X cycle time**
  - **Appearance of new defects/faults during yield ramp was changed from 1 per month to 4 per year**

Key Changes in 2002 Electronic Update…continue

- For the Yield Model and Defect Budget (YMDB) section, the ITWG members recommended using the cluster coefficient of 2 instead of 5. This revision will be made in 2003.

- For the Wafer Environment Contamination Control (WECC) section, besides clarifying the notes associated with the technology requirements table, the particle size distribution for fluids/gases of interest has been specified as $f(x)=K*1/X^{2.2}$ based on a reference cited in the notes.

Changes and Additions for 2003

- Limit scope to wafer sort yield.
- Look at the relationship between yield enhancement and manufacturing process control. Also connect the yield learning section to other TWGs.
- **Add new difficult challenges and new topics:**
  - **Line edge roughness, ACLV, subtle process variation**
  - **Where does process variation stop and defect start?**
  - **Contamination transferred from wafer edge and backside**
  - **Unified definition of defects based on yield impact**
- Must come up with creative solutions to improve yield learning rate because of increasing complexity and cycle time.
- Expand on new material coverage extending classical CMOS (i.e. high κ, Low κ, and Cu in all 4 focus topics).
- Drive the roadmap based on 300mm wafer size and issues critical to making high yielding 300mm fabs.
- Include commonality and uniqueness beyond classical CMOS i.e. SOI, SiGe, strained silicon, etc. in all 4 focus topics (DDC, YL, YMDB, WECC).

Overall future challenges

Key challenges

- high aspect ratio inspection and review possibility
- Integration of in-line physical failure analysis to improve root cause identification
- signal/noise : sorting of defects of interest vs nuisance defects
- cycle time / yield learning challenges

Cross functional challenges with design subgroup

- design for yield
  automation for recommended rules, implementation of DFM in productive environment (tools). For e.g. minimize critical area, add redundant rows, columns & vias and metal extensions.
- design for test/analysis

Other challenges

- structural test (bitfail map with pattern recognition for logic), procedures to extract fault densities
- non visual defect source
- cost of yield
- yield vs throughput (production needs limit useable sensitivity)

Table 95a Technology Requirements for WECC - Near-term

	Year of Production	2001	2002	2003	2004	2005	2006	2007
	DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
	MPU / ASIC ½ Pitch (nm)	150	130	107	90	80	70	65
	MPU Printed Gate Length (nm)	90	75	65	53	45	40	35
	MPU Physical Gate Length (nm)	65	53	45	37	32	28	25
Was	Wafer Environment Control							
Is	SAME							
Was	Critical particle size (nm) [A]	65	58	52	45	38	35	33
Is	SAME							
Was	# Particles > critical size (/m^3) [B]	5	4	3	2	2	1	1
Is	SAME							
Was	Airborne Molecular Contaminants (ppt)) [C]							
Is	Airborne Molecular Contaminants (pptM)) [C]							
Was	Lithography—bases (as amine, amide, or NH_3)	750	750	750	750	750	<750	<750
Is	SAME							
Was	Gate—metals (as Cu, E=2 $\times 10^{-5}$) [C]	0.2	0.2	0.15	0.1	0.1	0.07	<0.07
Is	Gate—metals (as Cu, E=2 $\times 10^{-5}$)	0.2	0.2	0.15	0.1	0.1	0.07	<0.07
Was	Gate—organics (as molecular weight greater than or equal to 250, E=1 ´ 10-3) [D] Organics (as CH_4)	100 1800	90 1620	80 1440	70 1260	60 1100	60 900	50 <900
Is	Gate—organics (as molecular weight greater than or equal to 250, E=1 $\times 10^{-3}$) [D] Organics (as CH_4)	100 1800	90 1620	80 1440	70 1260	60 1100	60 900	50 <900
Was	Salicidation contact—acids (as Cl-, E=1 $\times 10^{-5}$)	10	10	10	10	10	<10	<10
Is	Salicidation contact—acids (as Cl-, E=1 $\times 10^{-5}$)	10	10	10	10	10	<10	<10
Was	Salicidation contact—bases (as NH_3, E=1 $\times 10^{-6}$)	20	16	12	10	8	4	<4
Is	Salicidation contact—bases (as NH_3, E=1 $\times 10^{-6}$)	20	16	12	10	8	4	<4
Was	Dopants (P or B) [E]	<10	<10	<10	<10	<10	<10	<10

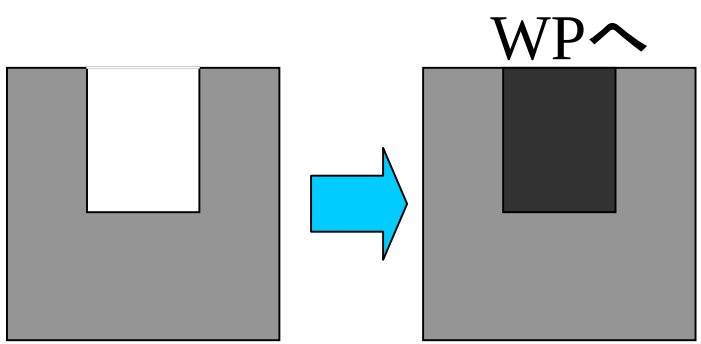
プローブ測定を工程途中で行う

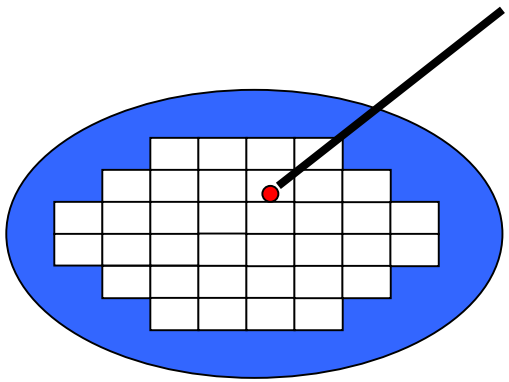
M1	206	CL_BAR1	Clean	Clean prior to Barrier Dep
M1	207	BARR_DEP	Dep Barrier Layer for Cu	Dep CVD Metal Nitride Barrier; A.R.= 1.7, Thk=11+/-1.25nm
M1	208	DEP_MET1	Deposit CVD Cu Seed	Deposit CVD Cu; 20nm
M1	209	DEP_MET1	Electroplate Cu	Electroplate Cu, 240 nm
M1	210	POLISH_MET1	Polish Cu; 260 nm	CMP -Polish 260 nm Cu Metal &11 nm barrier metal; Stop on oxide Hard Mask
M1	211	CL_MET1	Post CMP Clean	Clean, Post CMP
M1	212	FCD_M1	Measure Metal Final CD	Measure Metal Final CDs(3 wfrs 20 sites / wafer)= 130+/-13 nm
M1	213	FINSP_M1	Inspect	Inspect, PLY(2 wfrs 100%)
M1	214	ANN_MET1	Anneal, Metal	Anneal, Metal; H2/N2, 100-325C(40m)/30m/N2 325-100C(40m). Note that the adequacy of 325C to anneal the process-induced damage is unclear.
M1	215	PARM_TEST	Parametric Electrical Test	Parametric Electrical Test, OPTIONAL Wafer Testing, 1 or 2 wafers/lot
M2	216	CL_DPNIT HM	Clean, Dep Nitride Etch Stop	Wet Clean
M2	217	DEP_NIT HM	Deposit Nitride Etch Stop	Deposit Plasma CVD Nitride, Blanket Etch Stop, 325C, 20 -25 nm
M2	218		Measure Nitride	Measure Nitride, THK/SDEV (2 wafers, 5 sites)
M2	219	COAT_701	Coat Low K Dielectric	Spin Coat Low K Dielectric, 430+/-30nm

セマテックの100nm工程シート

In-line Sampling

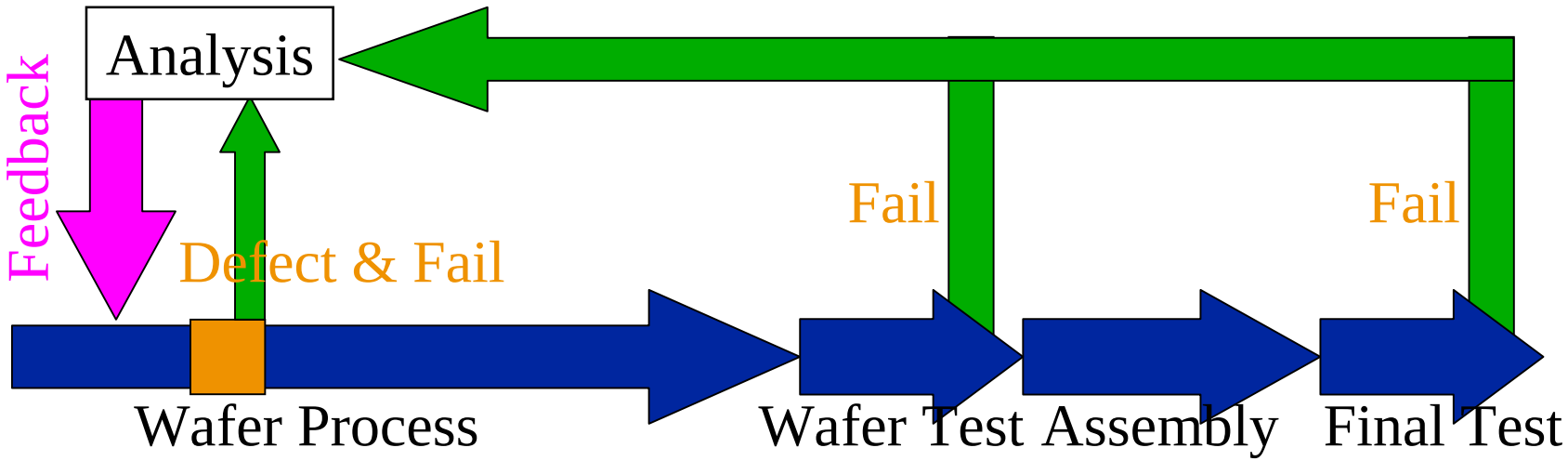
- **Wafer : FIB Cut & Capping(Micro-Surgery)**
  - Return to Process after Review(Dual Beam), or Sample Cut and Capping
- **Wafer TEM Sample: Micro-Sampling**
  - TEM obsevation for SEM-difficult Location





Quick Turn Around Time Failure Analysis

- **In-line Failure Analysis Capability Establishment**
  - In-line Fault Sourcing
  - Wafer Review/Analysis
  - In-line Sampling by Micro-Surgery



まとめ

- 装置許容欠陥数はStapperの計算式で、PWPまたはPIDを提示する。
- ISSM2002の発表を通じてPWP vs PIDの議論。PWPでPIDを代用する。
- Invisible欠陥を例示した。セマテックもMember companyで問題としているInvisible Defectをアンケート調査中。
- In-Line FA, DFM, DFTを提案した。