How can we share the pain?

ー新材料開発がもたらすものー

＜FEP WG＞

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*:国際対応

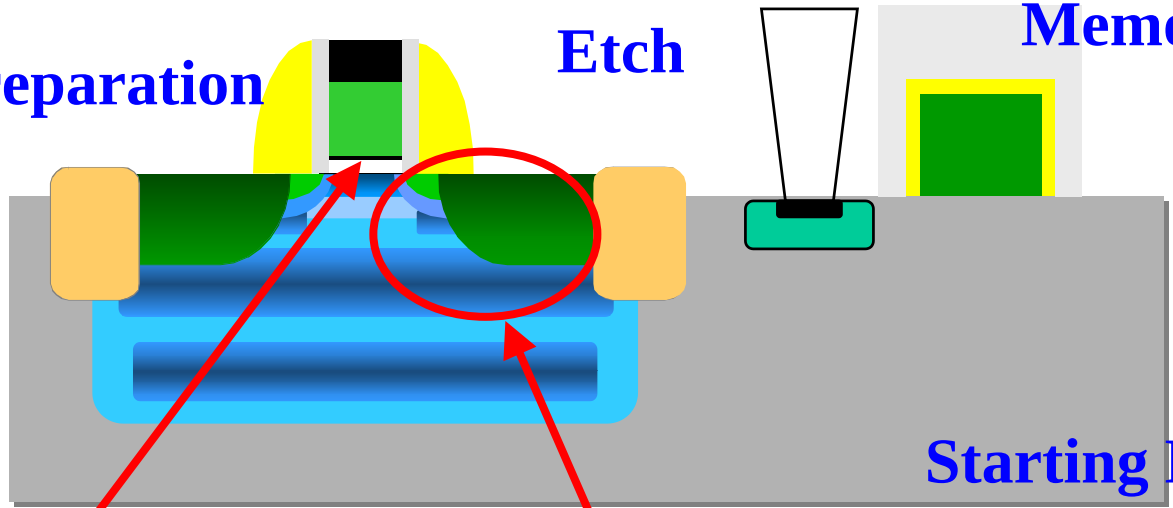
OUTLINE

- FEPの取り扱う技術分野
- FEPと“*Share the Pain*”
- ITRS2003の変化点と課題
  - 各技術分野
  - Memories
- まとめ

FEPの取り扱う範囲

--- Starting MaterialsからSilicidationまで＋Memory

（STRJ担当：DRAMとFeRAM）



Surface Preparation

Etch

Memory

DRAM
Flash
FeRAM

Starting Materials

SOI
SON
Strained-Si/SiGe
Si on X

Thermal/Thin Films

High-k
Poly-SiGe
Metal Gate

Doping

Heavy Metals
Elevated S/D (SiGe)

ITRS2003: "Share the Pain"

複数の解決策にリスク分散。
FEPの新材料導入への期待が大きい。

In the chapters on PIDS and FEP, …it is observed that careful optimization of device parameters by "sharing the pain" has been proven to still enable continuing performance improvement in MOSFETs.

FEP- The Grand Challenges

デバイス構造・プロセスの工夫だけでなく、新材料導入が不可欠な時代に

- **Introduction of many new materials into the CMOS Logic and DRAM process flows (2003-2007)**
  - **High k gate dielectric layers**
  - **Dual metal gates**
  - **New DRAM storage capacitor structures and materials**
  - **New substrate materials such as SOI and strained silicon**
  - **Alternate memory devices and materials, e.g. MRAM, FeRAM**
- **Beyond 2007, the probable introduction and CMOS integration of non-standard, dual-gate MOSFET's e.g. FINFET**

CMOSプロセスにおける新材料(元素)

その大部分はFEPで使用される

I a	II a	III a	IV a	V a	VI a	VII a	VIII			I b	II b	III b	IV b	V b	VI b	VII b	0
1	2	3	4	5	6	7	8			9	10	11	12	13	14	15	16
H																	He
Li	Be											B	C	N	O	F	Ne
Na	Mg											Al	Si	P	S	Cl	Ar
K	Ca	Sc	Ti	V	Cr	Mn	Fe	Co	Ni	Cu	Zn	Ga	Ge	As	Se	Br	Kr
Rb	Sr	Y	Zr	Nb	Mo	Tc	Ru	Rh	Pd	Ag	Cd	In	Sn	Sb	Te	I	Xe
Cs	Ba	La	Hf	Ta	W	Re	Os	Ir	Pt	Au	Hg	Tl	Pb	Bi	Po	At	Rn
Fr	Ra	Ac															

使用中 (FeRAM等を含む)

導入を検討中 (MRAM等を含む)

Starting Materials

Starting Materials Technology Requirements

Metrology capability limit (e.g. by extra-reflection) is emphasized.

General: Targeted particle size, Nanotopography, Site flatness.

New substrate: Particle(120-150nm: on SOI), Film thickness, Defects.

Technology requirements for SOI are raised to CZ wafer level(99% yield).

PD/FD-SOI thickness are for starting materials instead of final device.

BOX thickness is doubled in the ITRS2003 (2 x MPU Lg)

Year of Production		2004	2007	2010	2013	2016	*Driver*
DRAM 1/2 Pitch (nm)		90	65	45	32	22	D ½
Front surface particle size (nm)	2001	≥ 45	≥ 35	≥ 23	≥ 16	≥ 11	D ½
	2003	≥ 90	≥ 90	≥ 90	≥ 65	≥ 45	D ½,M
Nanotopography *New*	2003	≤ 23	≤ 16	≤ 11	≤ 8	≤ 6	M
Silicon-On-Insulator Wafer (99% Chip Yield)*							
FD-SOI thickness (nm) *Final*	2001	11 - 19	8 - 13	5 - 9	4 - 7	3 - 5	M
Starting	2003	21 - 39	18 - 33	15 - 19	14 - 16	13 - 14	M
Large defects (DRAM) (cm^{-2})	2001	≤ 0.055	≤ 0.028	≤ 0.028	≤ 0.021	≤ 0.022	D ½
	2003	≤ 0.009	≤ 0.010	≤ 0.012	≤ 0.012	≤ 0.007	D ½
Large defects (MPU) (cm^{-2})	2001	≤ 0.017	≤ 0.017	≤ 0.017	≤ 0.017	≤ 0.017	M
	2003	≤ 0.003	≤ 0.003	≤ 0.003	≤ 0.003	≤ 0.003	M

Supplier Metrology

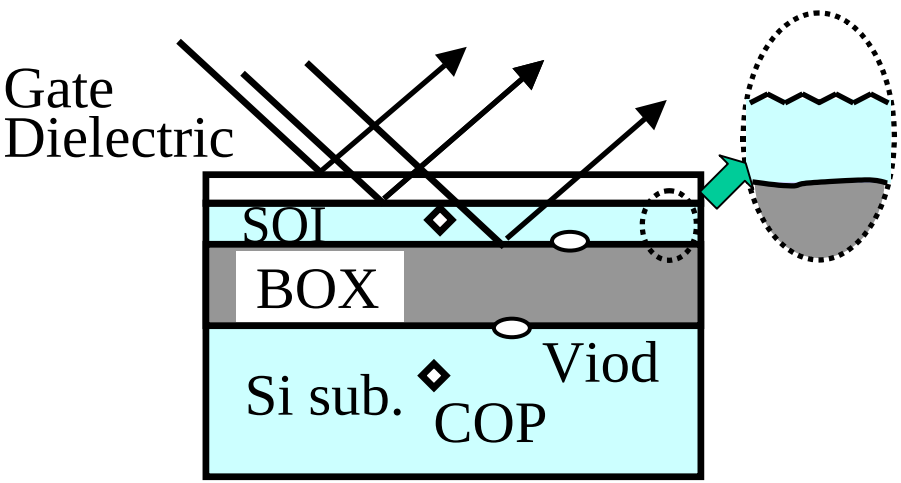
Work in Progress - Do not publish

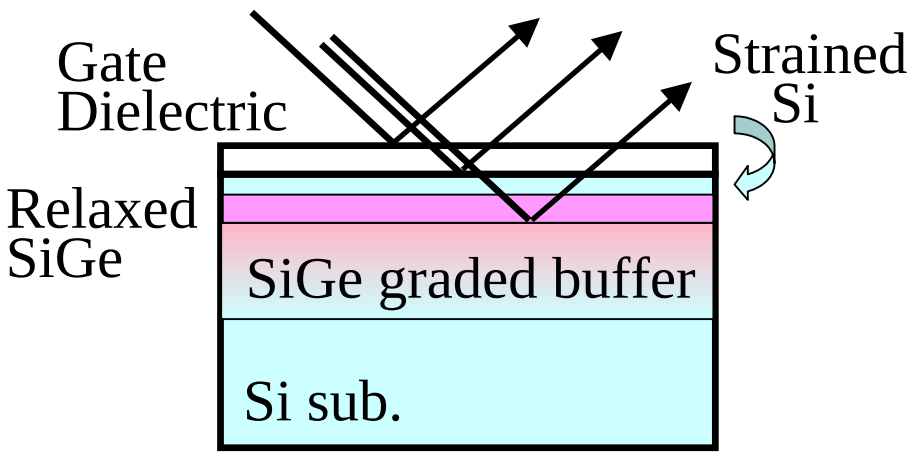
New Metrology Requirement

Optical measurements (ex. computed multilayed model fitting) of
Film thickness, Particles, Nanotopography, Defects, •••

Extra-reflection by
(Specific) Layered structure, COPs, Voids, Roughness(Haze), ••

Optical constants (ex. ε) modified by
Stress, Local strress distribution?, Ge conc., Ge profile, ••



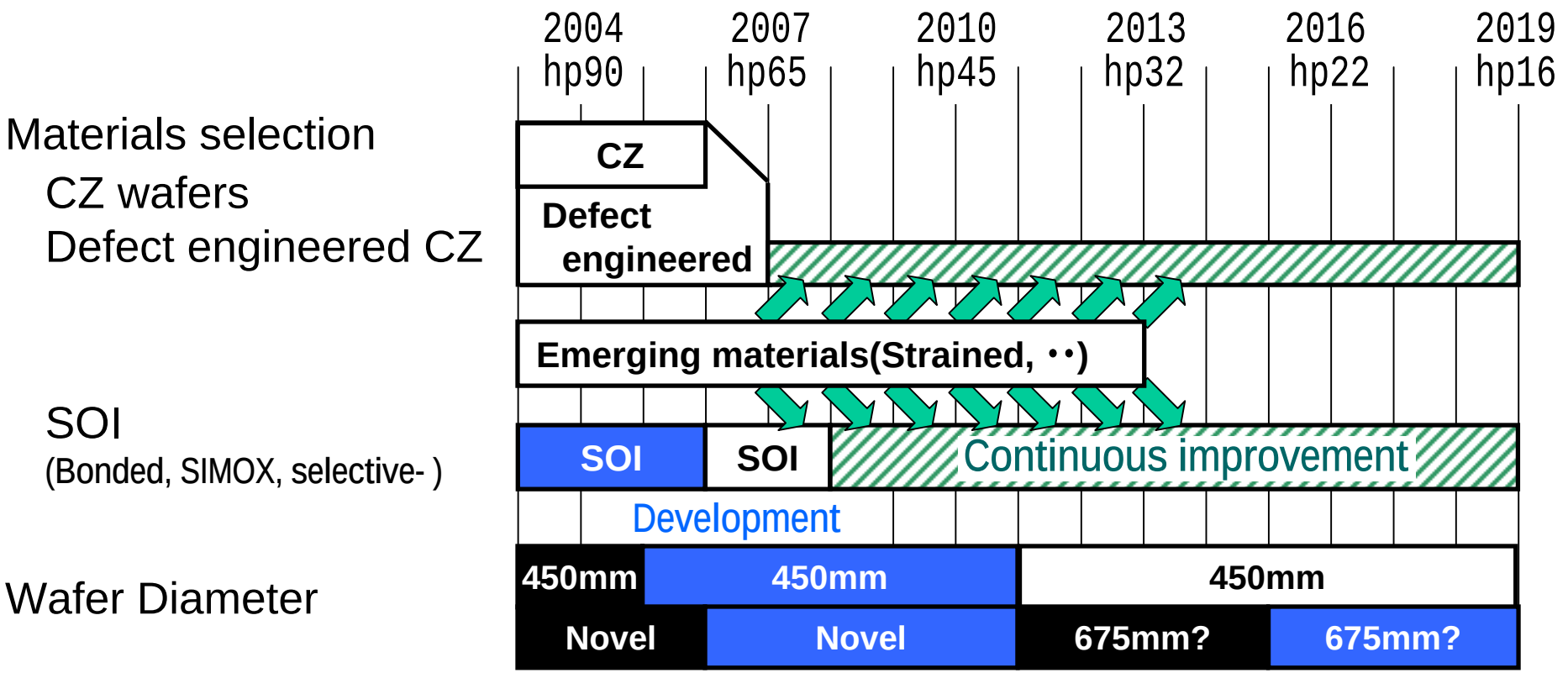


Potential Solutions

***SOI may become the dominant wafer type*, even for non-classical CMOS.**

Materials selection scenario (emerging materials, large diameter, •••)

- ***Near term: Defect-engineered CZ, SSOI, SGOI, PD-SOI***
- ***Long term: FD-SOI, 450mm or alternate structure***



Surface Preparation

Changed requirements in 2003

1. Watermarks were removed from metrics table because it is widely understood that no watermarks can be tolerated.

2. Back surface particles were removed from metrics because of no data or available models.

3. Residual carbon metrics have not changed significantly.

4. Metallic contamination metrics are unchanged.

The metals are empirically grouped into three classes :

(a) Mobile metals such as Na and K (b) metals which dissolve in silicon or form silicides such as Ni, Cu, Cr, Co, Hf and Pt and (c) major gate-oxide-integrity (GOI) killers such as Ca, Ba, Sr and Fe

5. New requirements for silicon and oxide loss were added.

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*	*Driver*
DRAM 1/2 Pitch (nm)	*100*	*90*	*80*	*70*	*65*	*57*	*50*	*D 1/2*
Silicon Loss (A) per cleaning step	1.2	1.0	0.8	0.7	0.5	0.4	0.4	*M*
Oxide Loss (A) per cleaning step	1.2	1.0	0.8	0.7	0.5	0.4	0.4	*M*

Contamination issues and cleaning technology for high-k

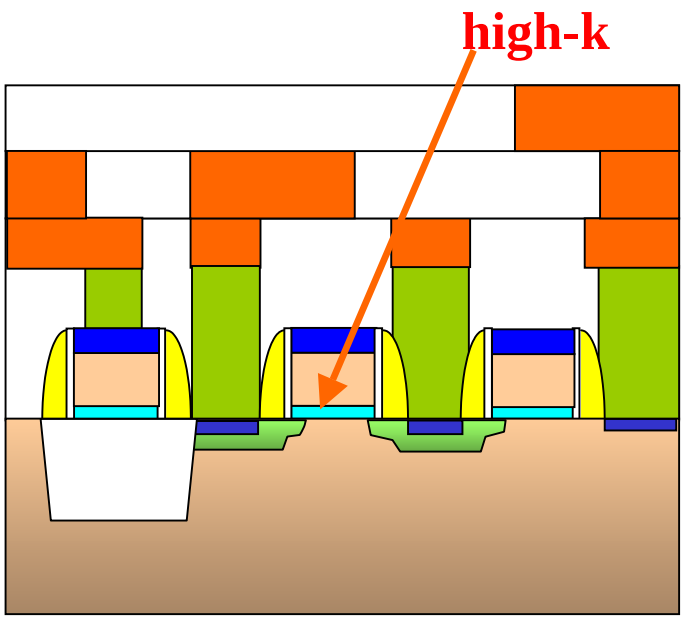
1. Issues of high-k related contamination

Contamination *from* high-k

→ **Clarification of acceptable contamination level**

Contamination *to* high-k

→ **Control of interfacial oxide and residual carbon**



2. Cleaning Technology Development

Chemically compatible high-k removal after gate definition

H-terminated cleaning and surface roughness control

Atmospheric control among cleaning, deposition, annealing and oxidation

↓

Integrated surface preparation techniques

Etch

Critical Dimension Etch

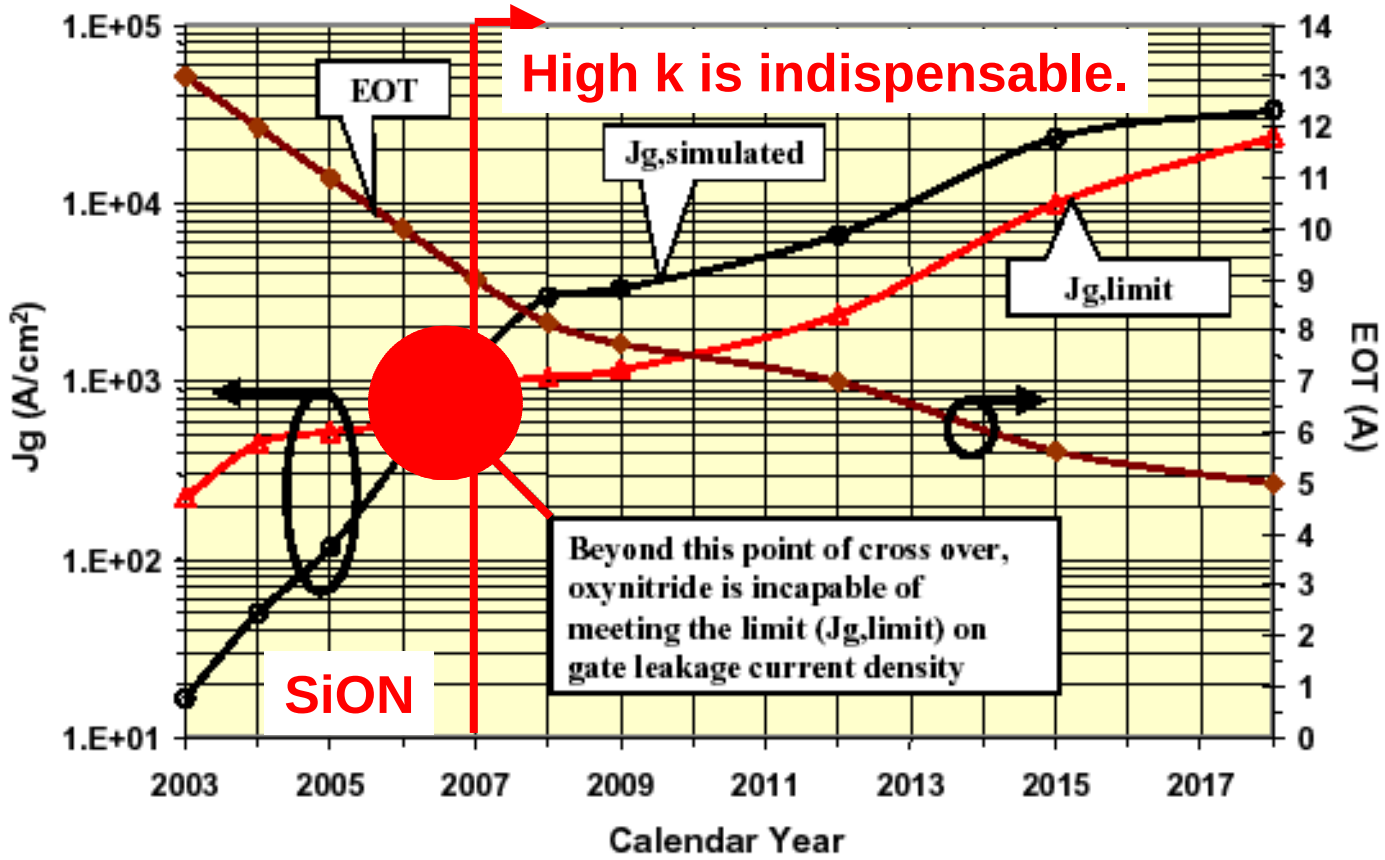
- **Upgrade resist trim and etch CD requirements**
  - **The allowable etch variance σ^2_{etch} is limited to 1/5 of the total variance, σ^2_T of the combined lithography and etch processes**

$$\frac{(\sigma_{etch})^2}{(\sigma_{total})^2} = \begin{matrix}\text{ITRS2001}\\ \frac{1}{3}\end{matrix} \Rightarrow \begin{matrix}\text{ITRS2003}\\ \frac{1}{5}\end{matrix}$$

		2003	2004	2005	2006	2007	2010	2013	2016
L_{gate} 3σ variation (nm)	ITRS2001	4.46	3.75	3.15	2.81	2.50	1.77	1.25	0.88
	ITRS2003	4.46	3.75	3.15	2.81	2.50	1.80	1.30	0.90
Total maximum allowable lithography 3σ (nm)	ITRS2001	3.7	3.0	2.6	2.4	2.0	1.5	1.1	0.7
	ITRS2003	◆4.0	3.3	2.9	2.5	2.2	2.0	1.4	1.0
Total maximum allowable etch 3σ (nm)	ITRS2001	2.57	2.17	1.82	1.62	1.44	1.02	0.72	0.51
	ITRS2003	◆1.99	◆1.68	1.41	1.26	1.12	0.80	0.58	0.40
Resist trim maximum allowable 3σ(nm)	ITRS2001	1.49	1.25	1.05	0.94	0.83	0.59	0.42	0.29
	ITRS2003	◆1.16	◆0.97	0.82	0.73	0.65	0.46	0.34	0.23
Gate etch maximum allowable 3σ(nm)	ITRS2001	1.77	1.48	1.32	1.18	1.05	0.83	0.59	0.41
	ITRS2003	1.62	◆1.37	1.15	1.02	0.91	0.66	0.47	0.33

Thermal/Thin Films

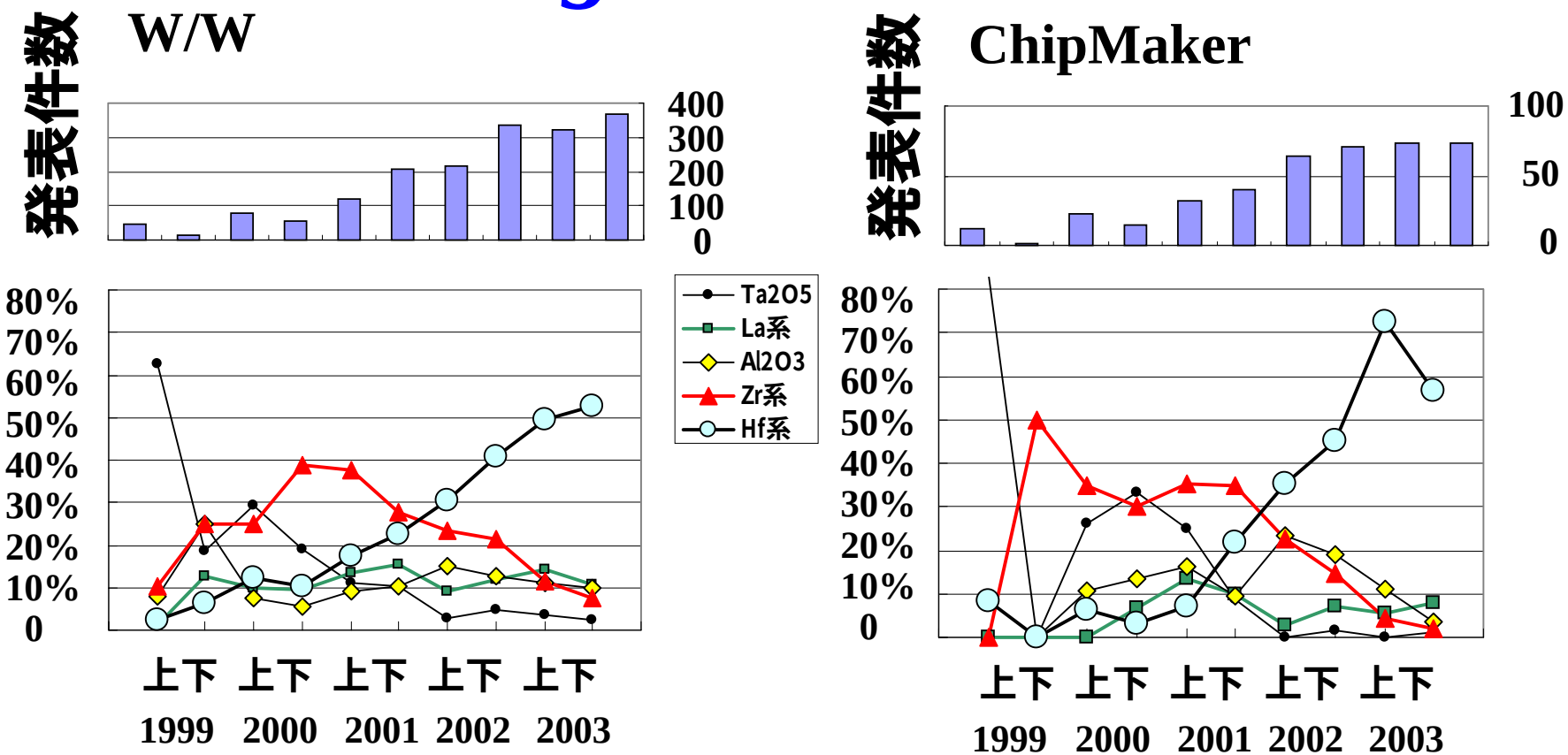
Intolerable pain from PIDS



High-performance Logic Scaling-up of Gate Leakage Current Density Limit and of Simulated Gate Leakage due to Direct Tunneling

***Based on More Conservative Estimate of Oxynitride Leakage: 1/30 of Oxide Leakage in 2003 ITRS vs 1/100 in 2001 ITRS**

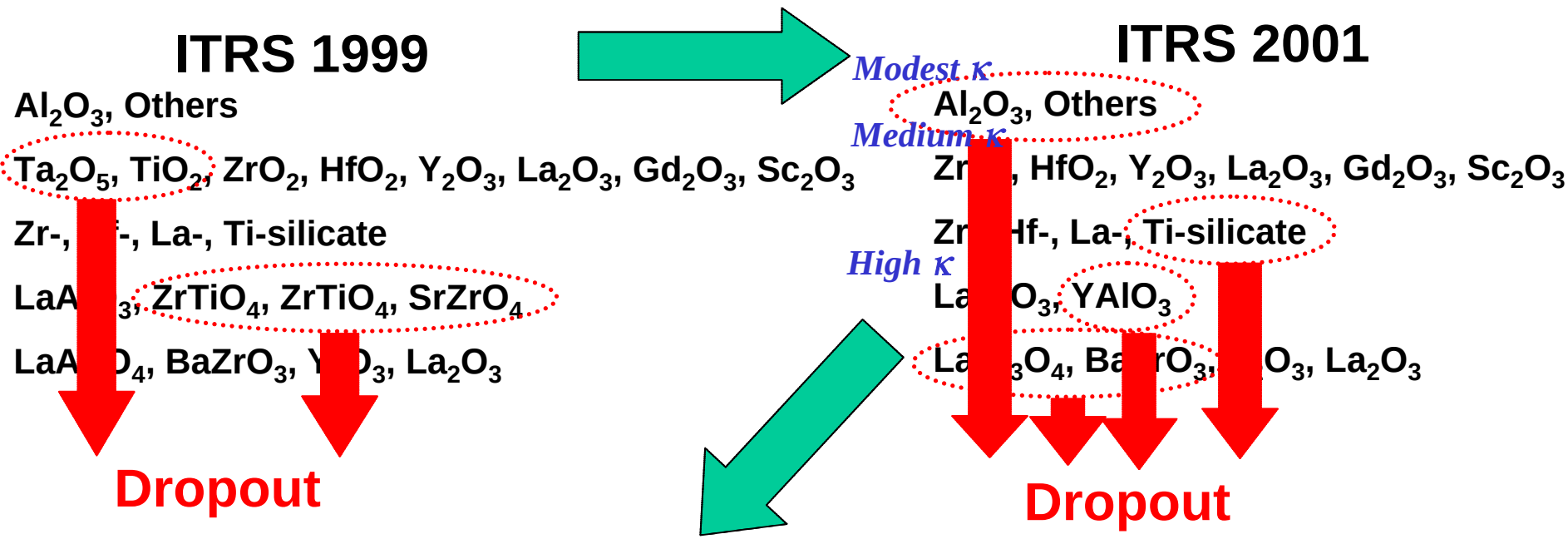
Publication number of high-k materials



Ta_2O_5 and ZrO_2 drastically decreased. The Hf-based family of high-k gate dielectrics has been significantly studied.

*北島、シリコンテクノロジ分科会研究会

Potential solution of high-k materials



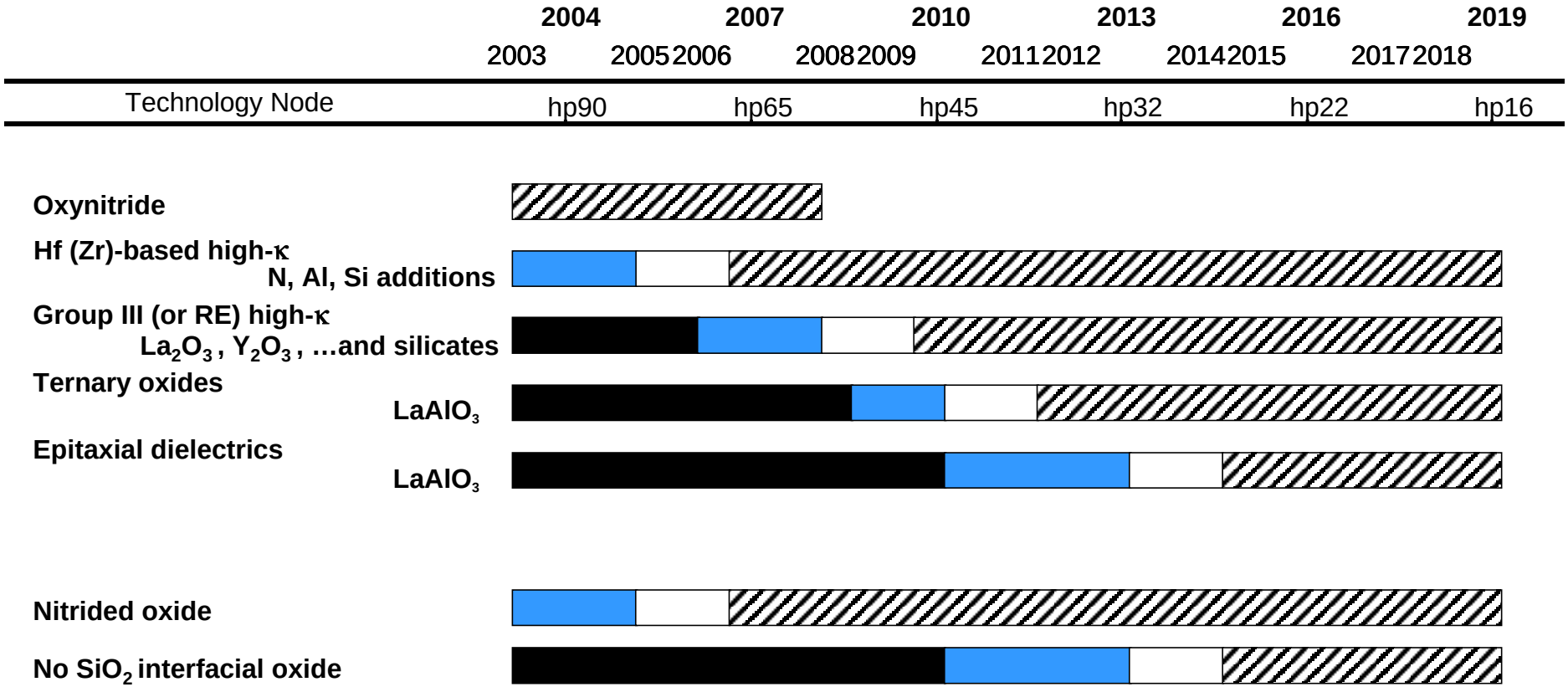
ITRS 2003

Hf (Zr)-based high-k
N, Al, Si additions
Group III (or RE) high-k
La_2O_3 , Y_2O_3 , …and silicates
Ternary oxides
$LaAlO_3$
Epitaxial dielectrics
$LaAlO_3$

Requirements

- $\kappa > 10$ (20 for long term)
- Band gap = 4 ~ 5 eV
- Barrier height > 1 eV
- Negligible PF current
- Thermal budget > 1000℃
- μ is comparable to SiON.

Introduction of high-k materials



Near-term requires ultra-thin silicon oxynitride films.
Hf-based family of high-k gate dielectrics has high potential.
Nevertheless, there will be severe restraints on surface preparation, pre-and post-process ambient control, silicon compatible materials development, and post-processing thermal budgets.

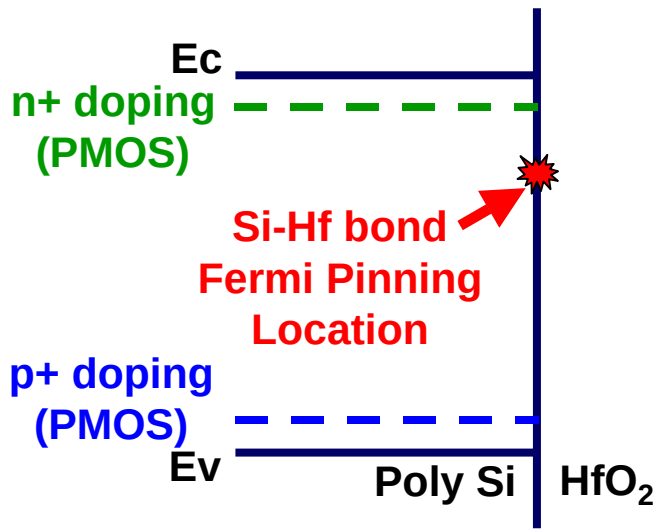
HP Logic, Metal Gate Delays Need for High-k Gate Dielectric

Year of Production	2003	2004	2005	2006	2007	2008	2009	Driver
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20	MPU
Gate Electrode Depletion Effect- Required Gate Dielectric EOT (in nm) to meet device EIT based on Gate Material Choice								
For the Case of 1E20/cm^3 poly doping	1.42	1.32	1.09	0.97	0.88	0.41	0.41	MPU/ASIC
For the Case of 2E20/cm^3 poly doping	1.69	1.59	1.38	1.25	1.15	0.74	0.74	MPU/ASIC
For the Case of Metal Gate:	2.04	1.94	1.74	1.64	1.54	1.15	1.15	MPU/ASIC

0.3nm improvement

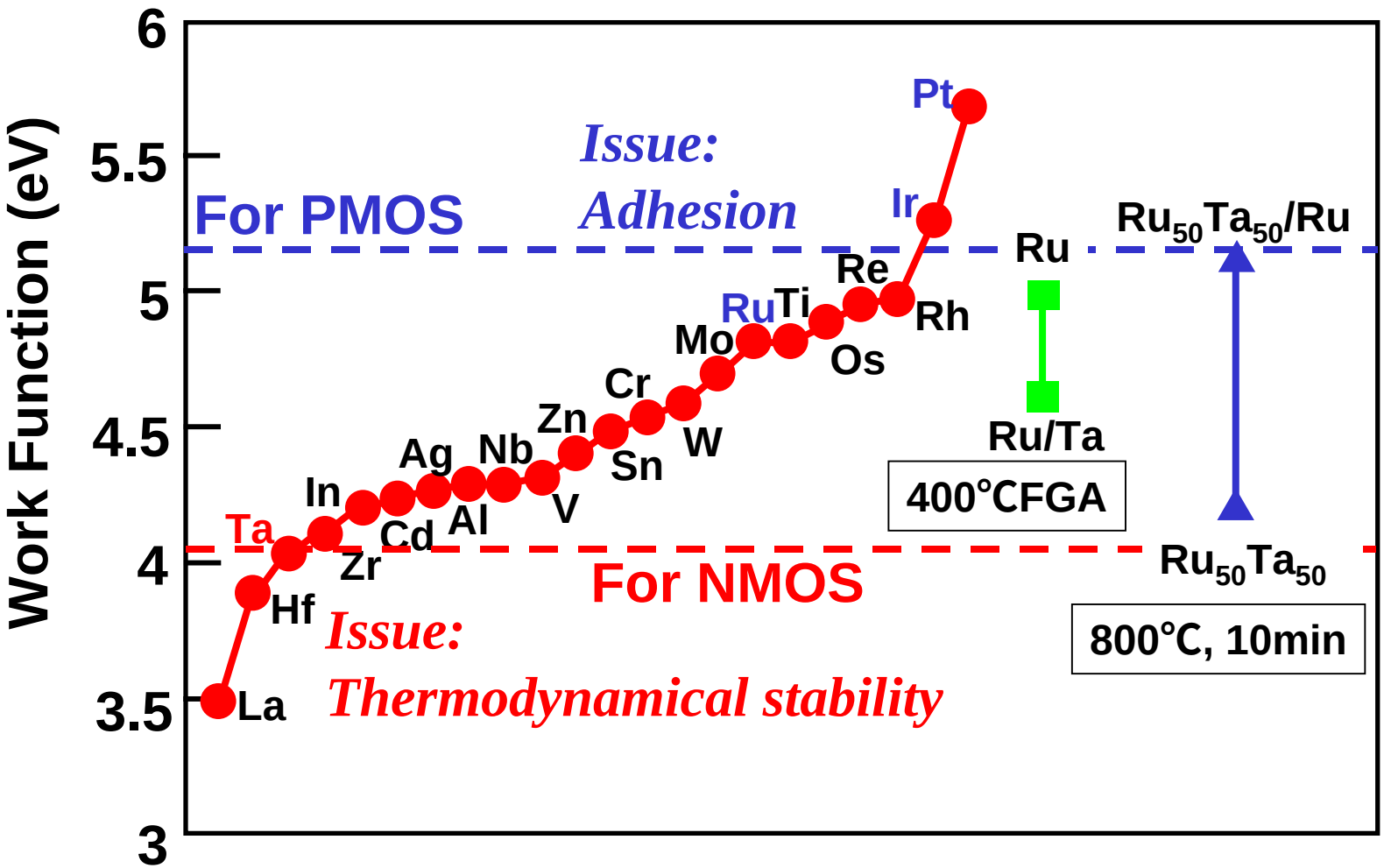
***Based on Modeling done by H. Gossmann, Axcelis Technologies Inc.**

Enhanced means of activating the doped polysilicon is very tough.
Fermi level pinning causes poly gate depletion and V_{th} shift with high k materials.
So high-K / metal gates transistors will have excellent characteristics.



***Hobbs, Symposium on VLSI Tech, 2003**

Work function engineering

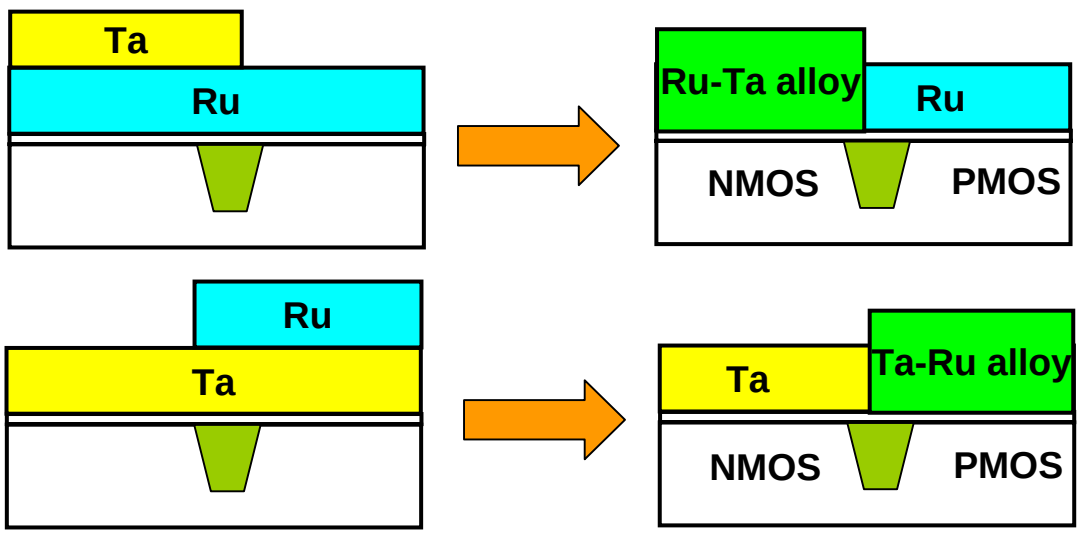


*Misra, 6th Annual Topical Research Conference on Reliability

Introduction of metal gate

	2004	2007	2010	2013	2016	2019
	2003 2005	2006 2008	2009 2011	2012 2014	2015 2017	2018
Technology Node	hp90	hp65	hp45	hp32	hp22	hp16
Poly Si or poly Si- Ge						
Metal 1for NMOS Ta/Ru, $Ta_xSi_yN_z$						
Metal 2 for PMOS Ru, Ru/Ta, Pt, Ir, Ni						
Tools and methods for electrodes CVD, ALE, PVD; clustered with dielectric; inorganic and organic sources						

One candidate of dual work function



*Lee, IEDM 2003

The introduction of FD SOI will need the gate work functions near mid-gap.

Choice of "replacement gate" or gate-last processes depends on surface preparation, doping or etching.

Mobility enhancement: ITRS2003

HP: High Performance

Years of Production	2001	2004	2007	2010	2013	2016
DRAM 1/2 Pitch(nm)	130	90	65	45	32	22
HP Phys. Lg(nm)	65	37	25	18	13	9
EOT(nm)	1.45	1.2	**0.9**	**0.7**	**0.6**	**0.5**
Depletion(nm)	0.8	0.8	**0.4**	**0.4**	**0.4**	**0.4**
Vdd(V)	1.2	1.2	1.1	1.0	0.9	0.8
Ion(uA/um)	900	1100	**1510**	**1900**	**2050**	**2400**
HP C*V/I(ps)	1.6	0.95	**0.64**	**0.39**	**0.26**	**0.15**
Mobility Imp. Factor	0%	30%	**100%**	**100%**	**100%**	**100%**

CV/I Improvement: 17% / year

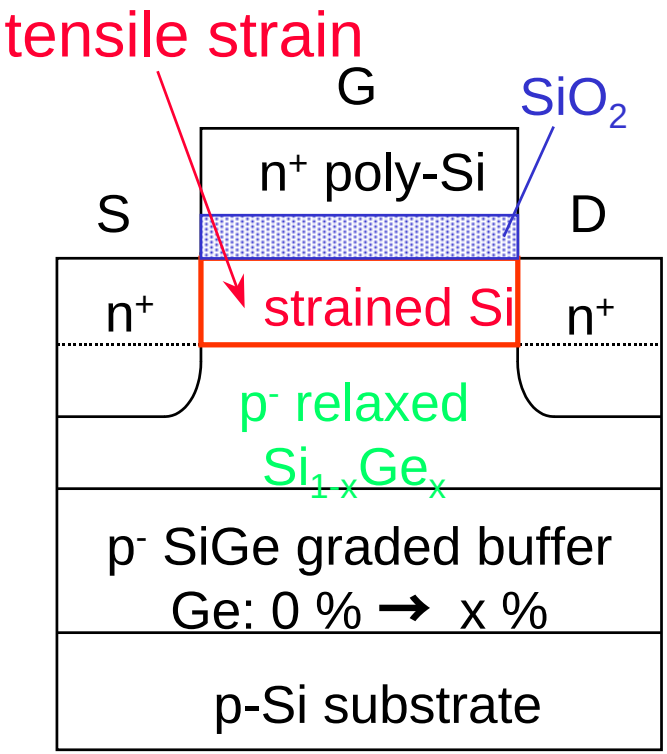
Mobility enhancement: ITRS2002 update

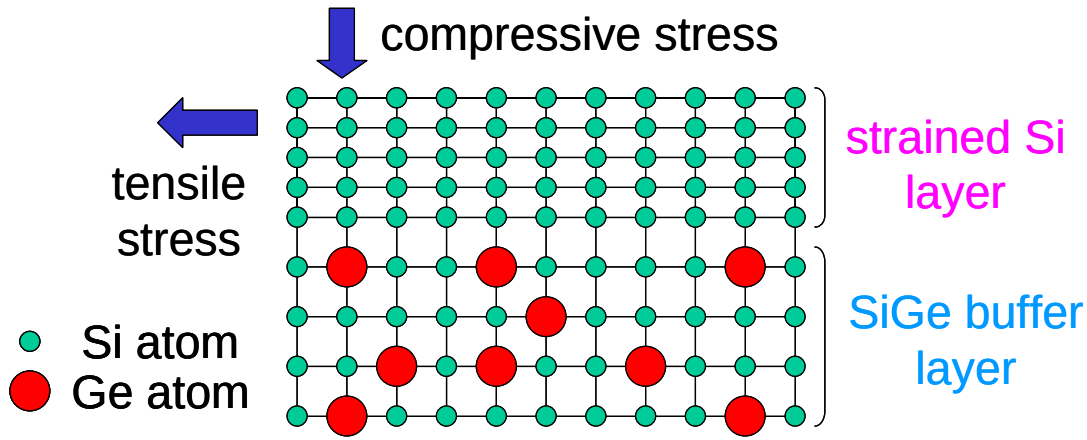
HP: High Performance

Years of Production	2001	2004	2007	2010	2013	2016
DRAM 1/2 Pitch(nm)	130	90	65	45	32	22
HP Phys. Lg(nm)	65	37	25	18	13	9
EOT(nm)	1.3-1.6	0.9-1.4	**0.6-1.1**	**0.5-0.8**	**0.4-0.6**	**0.4-0.5**
Depletion(nm)	0.8	0.8	**0.5**	**0.5**	**0.5**	**0.5**
Vdd(V)	1.2	1	0.7	0.6	0.5	0.4
Ion(uA/um)	900	900	900	1200	**1500**	**1500**
HP C*V/I(ps)	1.6	0.99	0.68	0.39	**0.22**	**0.15**
Mobility Imp. Factor	0%	0%	0%	30%	**70%**	**100%**

CV/I Improvement: 17% / year

High mobility by strain Si



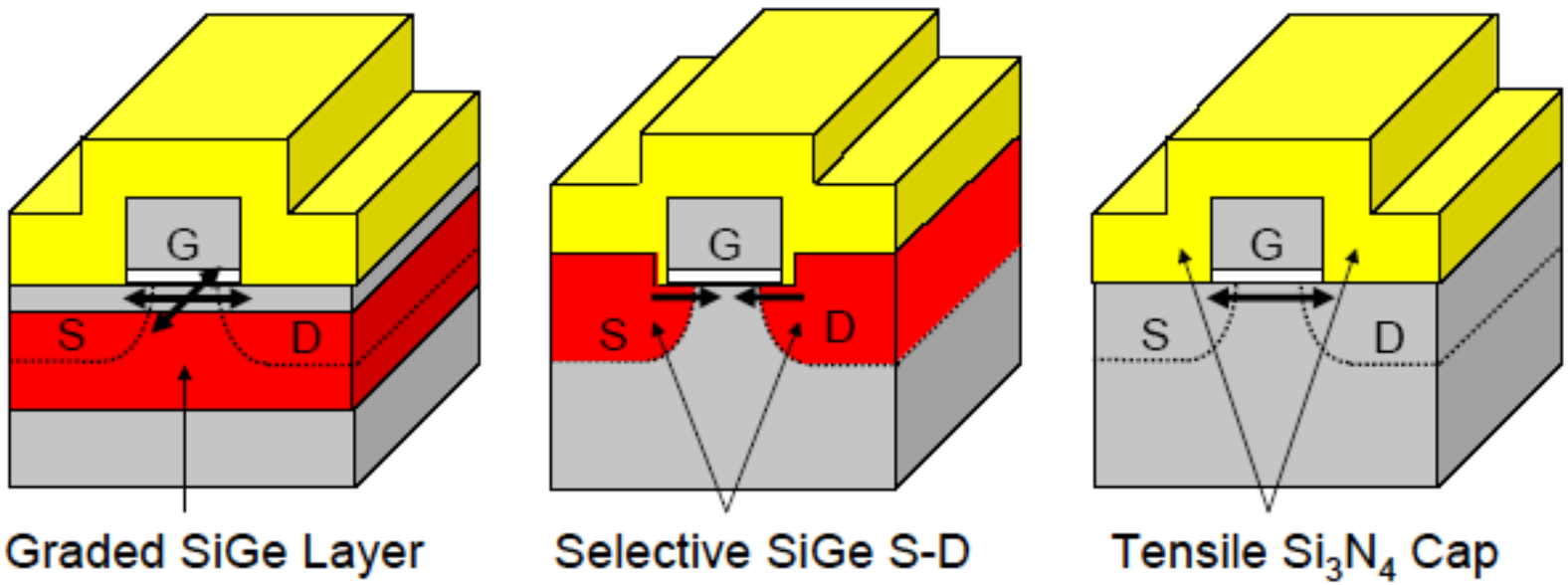


(J. Welser et al., IEDM'92, p.1000)

Mobility enhancement (Intel's case)

Transistor Strain Techniques

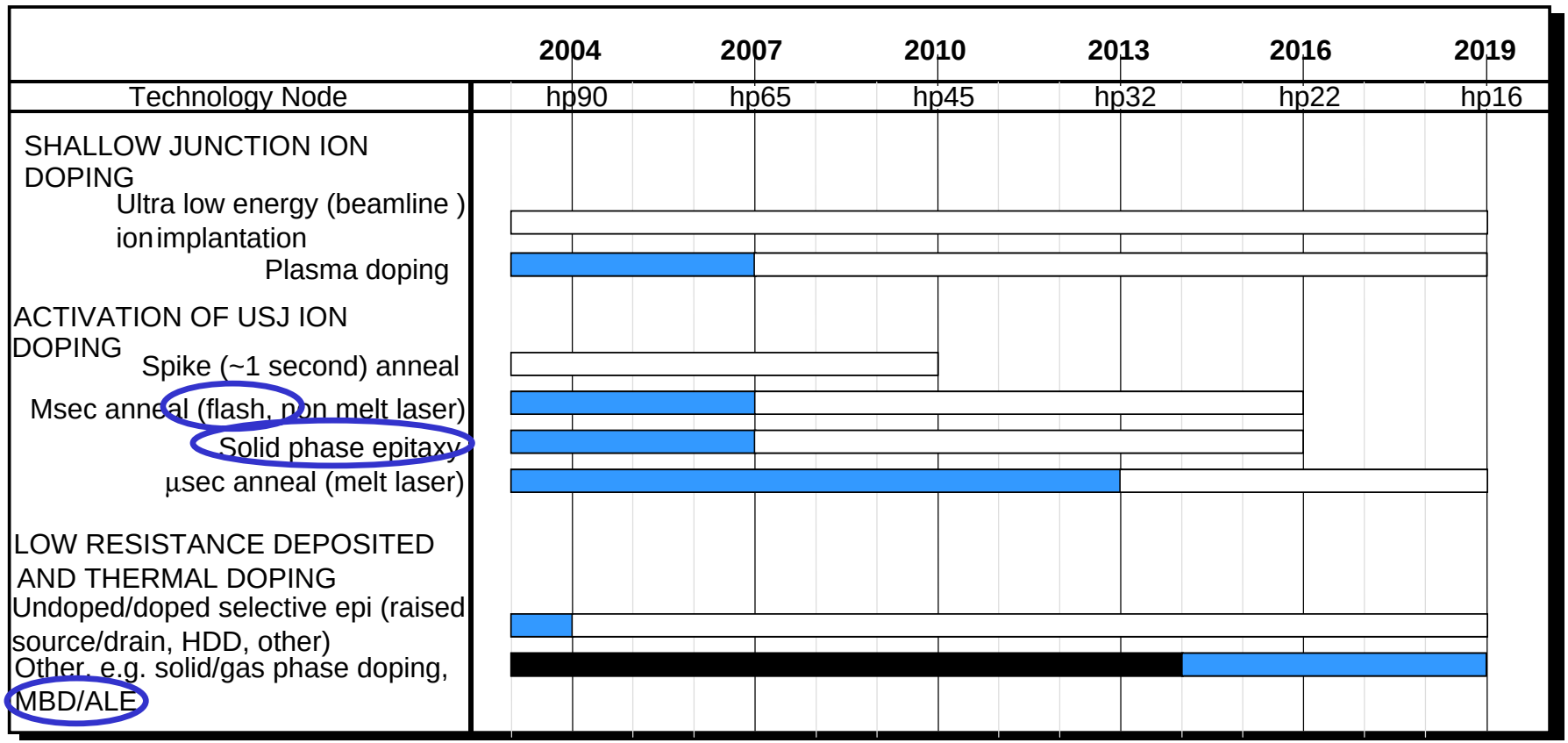
(Intel: Mass production since 2004)



Doping

Doping Potential Solutions

- **Major challenges continue to surround the achievement of ultra-shallow, abrupt, highly activated drain extensions.**
  - **Drives innovation in ion implantation processes & equipments**
  - **Drives R&D for very rapid activation processes**

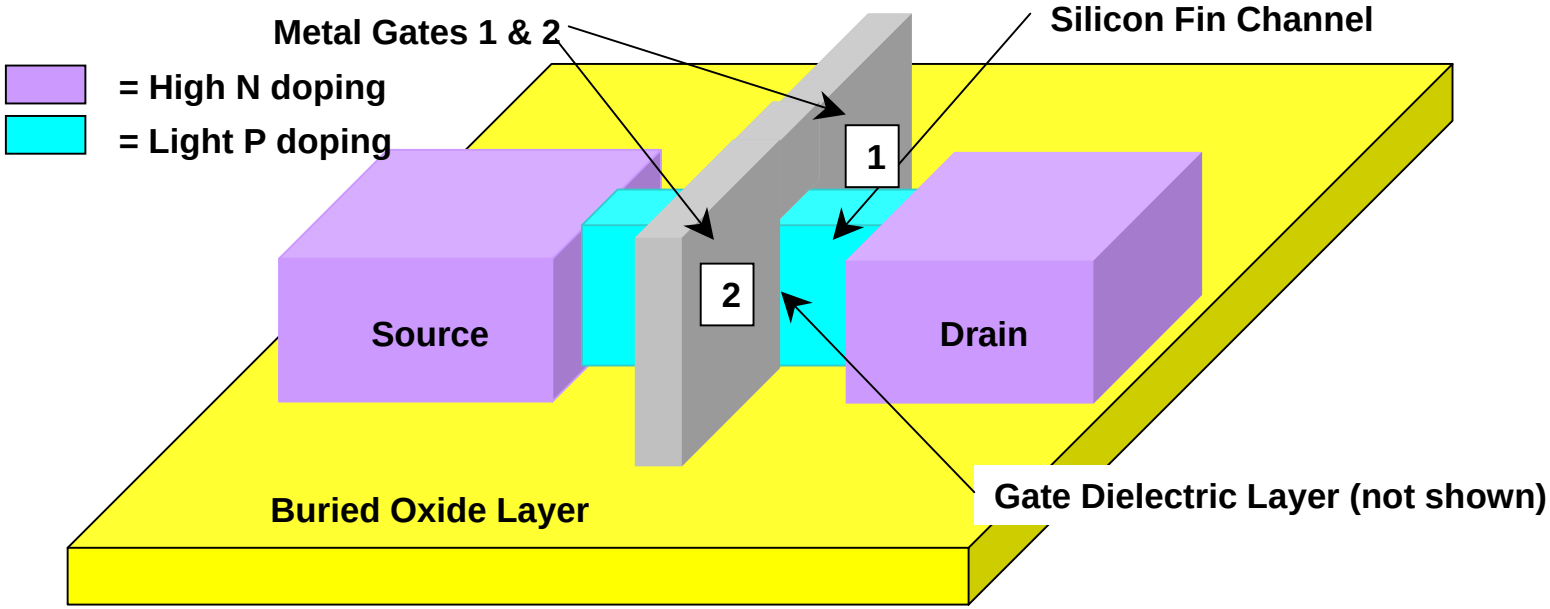


Junction Design

- **Attempts at more sophisticated model-based forecasting of Source/Drain requirements have not yet yielded conclusive results**
  - **S/D requirements highly interactive with overall transistor design**
  - **S/D requirements for bulk devices are different from SOI and future non-planar double gate devices**
  - **Drain Extension requirements are listed as target values**

Year of Production	*2003*	*2004*	*2005*	*2006*	*2007*	*2008*	*2009*	*Driver*
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20	MPU
PIDS Assumed Device Structure	Enhanced Planar Bulk CMOS					FDSOI, Elevated Contact		MPU/ASIC
Drain Extension Xj (nm)	24.8	20.4	17.6	15.4	13.8	8.8	8.0	MPU/ASIC
Maximum Drain Extension Sheet Resistance (Ohm/Sq) PMOS	545	663	767	833	884	1739	1800	MPU/ASIC
Maximum Drain Extension Sheet Resistance (Ohm/Sq) NMOS	255	310	358	389	412	811	840	MPU/ASIC
Extension Lateral Abruptness (nm/decade)	5	4.1	3.5	3.1	2.8	TBD	TBD	MPU/ASIC
Contact Xj (nm)	49.5	40.7	35.2	30.8	27.5	NA	NA	MPU/ASIC
Sidewall Spacer Thickness , Extension Structure (nm)	49.5	40.7	35.2	30.8	27.7	NA	NA	MPU/ASIC

Impact of Double- or Tri-Gate Device on Doping



	2004	2007	2010	2013	2016
Technology Node	hp90	hp65	hp45	hp32	hp22
DEVICE STRUCTURES					
Conventional planar channel/contact					
Re-engineer junction, channel doping with compatible contact for strain/SiGe					
Align annealing roadmap with high-κ gate material decisions					
High aspect ratio doping for 3D structures (plasma, angled implant, other)					

Memories

DRAM Technology Requirements

High-k dielectrics are changed.

BST and STO disappeared.

Ta_2O_5 and Al_2O_3 are extended to 2010 for DRAM stacked capacitor

– High aspect ratio of storage node for cell plate deposition is needed in 2010

– Aspect ratio of High Aspect Contact (HAC) increases over 50 in 2013

		03	04	05	06	07	10	13	16
Dielectric Constant	ITRS2001	50	50	250	300	450	800	1500	3000
	ITRS2003	22	22	40	50	50	50	60	80
A/R of SN(OUT) for cell plate depo.	ITRS2001	13.4	13.3	28.9	25.7	25.2	19.8	14.3	13.3
	ITRS2003	29.4	19.9	32.1	39.4	26.5	71.2	128.2	286.0
HAC A/R	ITRS2001	15.5	16.3	15.8	16.3	15.3	17.4	21.0	25.4
	ITRS2003	25.0	21.9	23.3	25.7	25.4	48.1	68.5	97.2

Flash Memory Technology Requirements

Clear Definition of the technology node for both NAND and NOR type Flash memories are given.

– The half-pitch of the memory cell (A) is the best definition of minimum feature size for NAND flash.

– Each of the half pitch parallel to the poly 2 word line (B), the poly 1 to poly 1 distance along the word line (C) and the minimum contact size (D) is the minimum feature size for NOR flash.

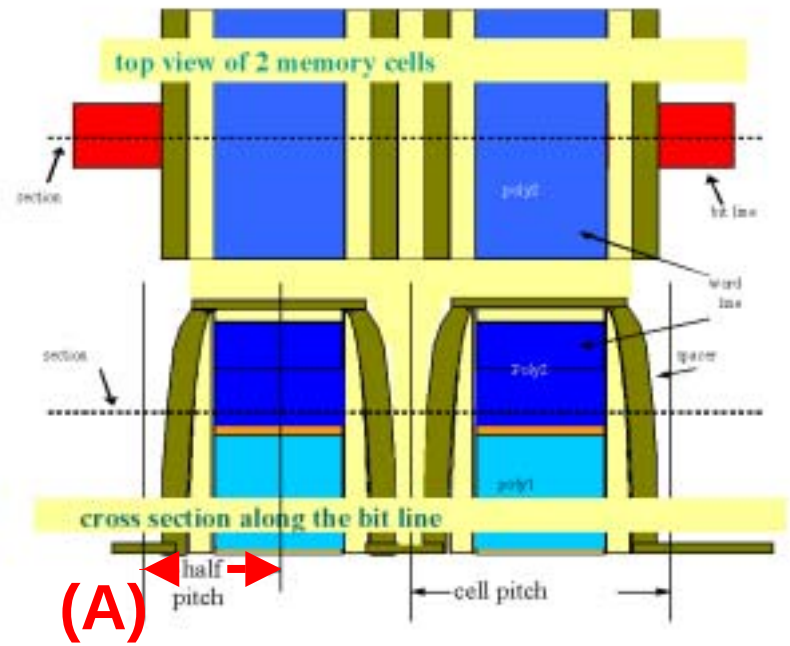


Figure 50 Minimum Feature Size of NAND Flash Memory

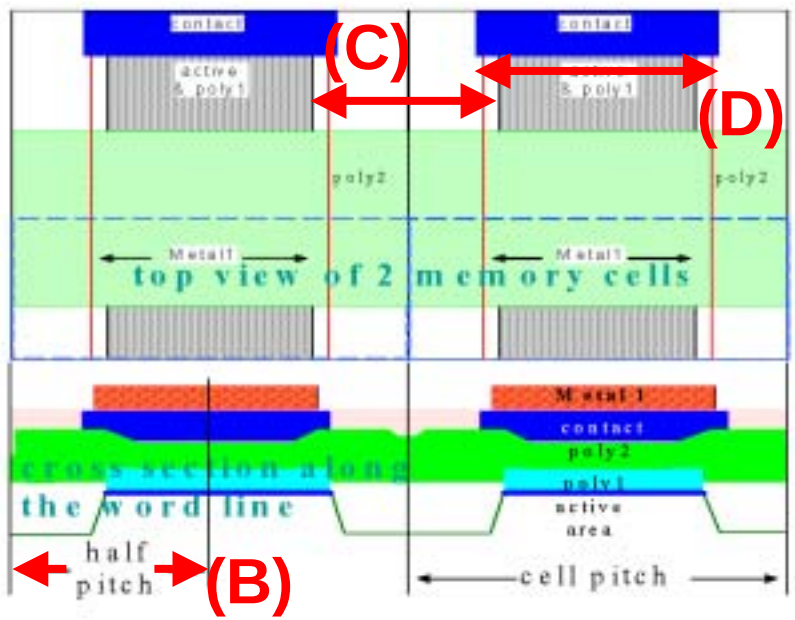


Figure 51 Minimum Feature Size of NOR Flash Memory

FeRAM

Feature Size & Cell Area Factor: Shown for Embedded as well as Standard since Embedded is dominant in the market

Memory Density:

"Demonstrator" Density to show the technology level

Year of First Product Shipment	2003	2004	2005	2006	2007	2010	2013	2016
Technology Node	100nm	hp90	80nm	70nm	hp65	hp45	hp32	hp22
ITRS2001 Feature Size (um): F1 (Standard Memory)	*0.25*	*0.18*	*0.18*	*0.18*	*0.13*	*0.1*	*0.07*	*0.05*
ITRS2003 Feature Size (um): F1 (Standard Memory)	0.25	0.18	0.15	0.13	0.12	0.09	0.065	0.045
ITRS2003 Demonstrator Density (Standard Memory)	32Mb	64Mb	128Mb	256Mb	256Mb	1Gb	4Gb	16Gb
ITRS2003 Feature Size (um): F2 (Embedded Memory)	0.18	0.13	0.12	0.11	0.10	0.07	0.05	0.035
ITRS2003 Cell Area Factor: a (Standard Memory)	15	15	12	12	12	8	8	8
ITRS2003 Cell Area Factor: b (Embedded Memory)	46	35	35	35	30	24	20	16

Summary

- FEP各分野のITRS2003に於ける変化点紹介
- 新材料導入：従来の課題解決と新たな課題
  - ◇SOI（ウェーハ）:
    需要は本格化、しかし測定に課題（*extra-reflection*）
  - ◇Strained-Si:
    一部で実用化、製法や移動度向上のモデル化が課題
  - ◇Gate Stack (High-k & メタルゲート)：
    High-k材料はHf系に絞られてきたが、Vth制御等課題
    メタルゲートとの一括実現が望まれる
- メモリ
  - ◇DRAM: キャパシタ誘電膜材料を見直し
  - ◇Flash: テクノロジーノードを定義
  - ◇FeRAM: Embeddedの記載追加