ITRS 2005 の概要

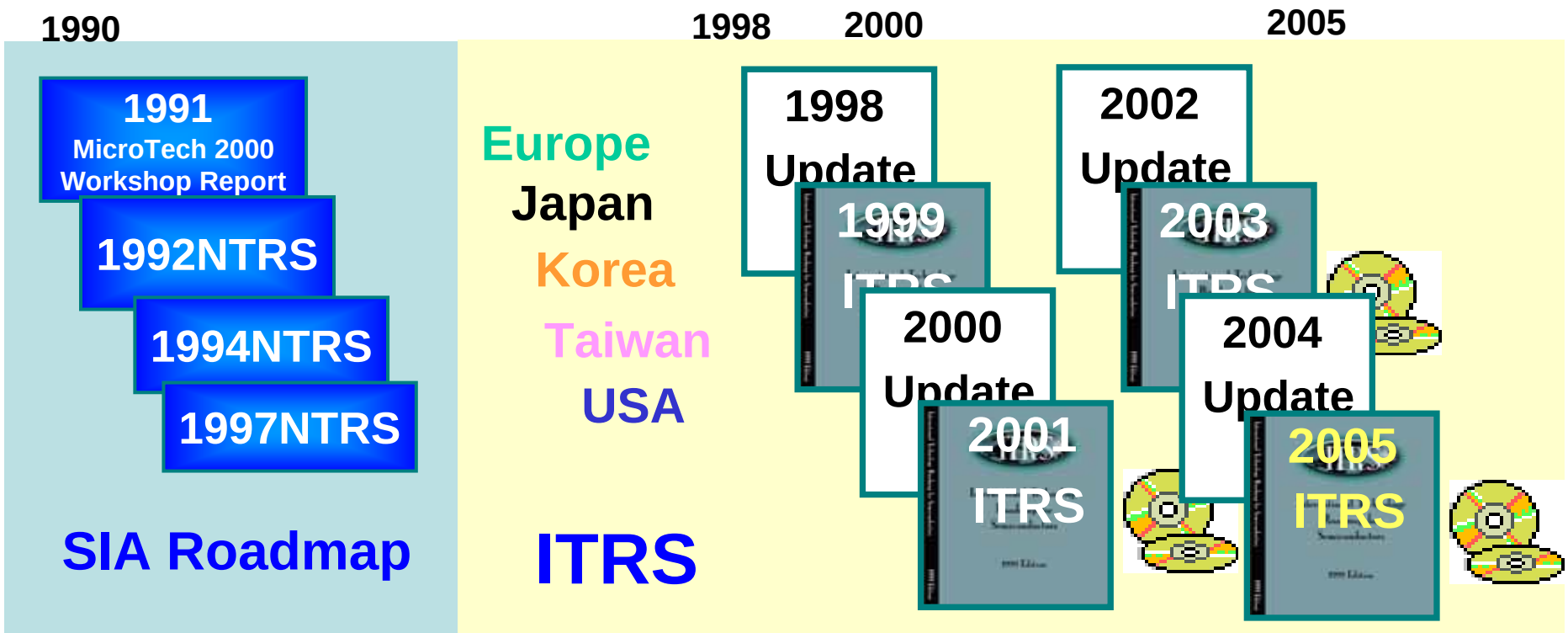
STRJ　委員長

石内　秀美　（(株) 東芝）

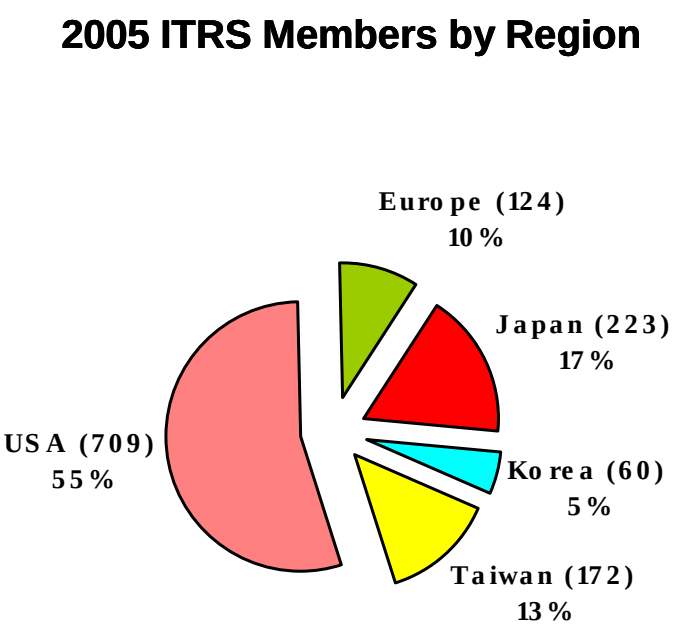
目次

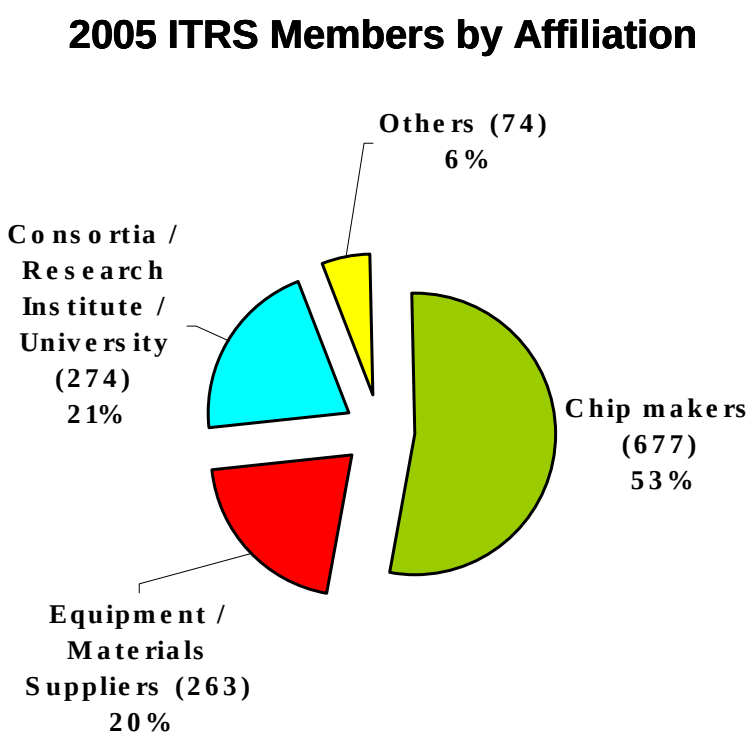
- **はじめに**
- ITRS 2005 Edition**の概要**
  - **主要トピックス**
  - **微細化トレンド**
  - **リソグラフィーツール**
  - High-k**ゲート絶縁膜導入時期**
  - MOS**トランジスタにおけるパラレルパス**
  - 450mm **ウェーハについて**
  - **多層配線技術**
  - **新探究デバイス** (Emerging Research Devices)
  - More Moore **と** More than Moore

NTRS/ ITRSの歴史と現状



ITRS 2005参加メンバーの統計





地域別

所属組織別

2005 ITRS Editionの主要トピックス

1　技術ノード

⑴ 技術ノード（Technology Node）を表のヘッダからはずす。

⑵ DRAM，NAND型Flashメモリ、MPU/ASICで別々のロードマップ

⑶ NAND型Flashメモリがもっとも厳しいルール（ハーフピッチ）を使う

2　リソグラフィー

ArF液浸リソグラフィーが次世代のツールとして最有力。その次はEUV 。

F2リソグラフィー、EPL、PEL は候補から外れる。

3　FEPとプロセスとデバイスインテグレーション（PIDS）

⑴ 用途別にプロセスの選択が多様化するという、“parallel path”の考え方を取り込む。同一のデザインルールでも複数の製造プロセスが共存する

⑵ High-k（高誘電率）ゲート絶縁膜材料の導入は2008年に延期

⑶ 450mmウェーハの導入は2012年

4　Emerging Research Devices (ERD、新探究デバイス)

独立の章となる。技術候補を入替。Non Classical CMOSはPIDS章で記述。

5　More MooreとMore than Moore

微細化（More Moore）とともに、多様化（More than Moore）の視点に言及

ITRS 2005の章構成

1. *Executive Summary*
   - *Introduction*
   - *Grand Challenges*
   - *What is New for 2005 --- the Working Group Summaries*
   - *Overall Roadmap Technology Characteristics*
   - *Glossary*
2. *System Drivers*
3. *Design*
4. *Test and Test Equipment*
5. *Process Integration, Devices, and Structures*
6. *RF and Analog/Mixed-Signal Technologies for Wireless Communications*
7. *Emerging Research Devices*
8. *Front End Processes*
9. *Lithography*
10. *Interconnect*
11. *Factory Integration*
12. *Assembly and Packaging*
13. *Environment, Safety, and Health*
14. *Yield Enhancement*
15. *Metrology*
16. *Modeling and Simulation*

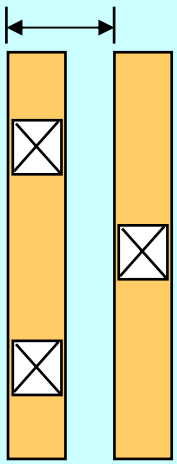
青字： 新しく独立した章

2003/2004 ITRS Definition of the Half Pitch - WAS

[DRAM half-pitch determines the 2003 ITRS "node"]

DRAM ½ Pitch
= DRAM Metal Pitch/2

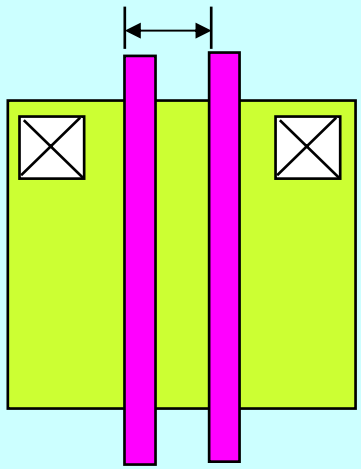
Metal Pitch



Typical DRAM
Metal Bit Line

MPU/ASIC Poly Silicon ½ Pitch
= MPU/ASIC Poly Pitch/2

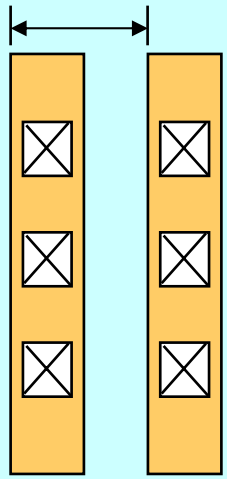
Poly Pitch



Typical MPU/ASIC
Un-contacted Poly

MPU/ASIC M1 ½ Pitch
= MPU/ASIC M1 Pitch/2

Metal 1 (M1) Pitch



Typical MPU/ASIC
Contacted Metal 1

Source: 2003 ITRS - Exec. Summary Fig 4

ITRS 2003年版:
DRAMのハーフピッチをTechnology Nodeの代表値とする。
各Tableのヘッダーにこの値を記載

Year of Production	2002 [Actual]	2003	2004	2006	2007	2009	2010	2012	2013	2015	2016	2018
Technology Node (nm)	hp130		hp90		hp65		hp45		hp32		hp22	

Source: 2003 ITRS - Exec. Summary

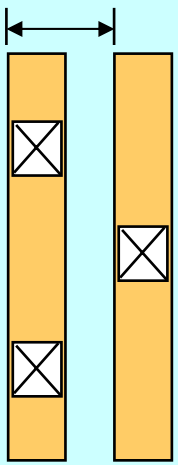
* Cycle Time = one-half of the time to reach a technology trend reduction to 0.5x

Half Pitchの定義 (ITRS 2005)

DRAM ½ Pitch
= DRAM Metal Pitch/2
MPU/ASIC M1 ½ Pitch
= MPU/ASIC M1 Pitch/2

Metal

Pitch

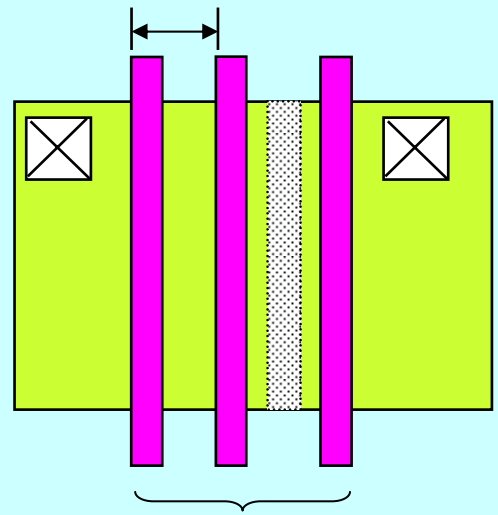


Typical DRAM/MPU/ASIC
Metal Bit Line

FLASH Poly Silicon ½ Pitch
= Flash Poly Pitch/2

Poly

Pitch



Typical flash
Un-contacted Poly

ITRS 2005年版：DRAM，Flash，MPUのハーフピッチを各Tableのヘッダーに記載

2005 ('05-'20) ITRS Technology Trends DRAM M1 Half-Pitch : 3-year cycle

Year of Production	2000 [Actual]	2001	2002 [Actual]	2003	2004	2005	2006	2007	2008	2009	2010	2012	2013	2015	2016	2018	2019	2020
Technology - Contacted M1 H-P (nm)	180	151	130	107	90	80	71	65	57	50	45		32		22		16	14

2-Year Technology Cycle ['98-'04]

3-Year Technology Cycle

2005 ITRS Flash Poly Half-Pitch Technology: 2.0-year cycle until 1yr ahead of DRAM @65nm/'06

Year of Production	2000 [Actual]	2001	2002 [Actual]	2003	2004	2005	2006		2008	2009	2010	2012	2013	2015	2016	2018	2019	2020
Technology - Uncontacted Poly H-P (nm)	180	151	130	107	90	76	65	57	50	45		32		22		16		13

2-Year Technology Cycle ['98-'06]

3-Year Technology Cycle

2005 ITRS MPU M1 Half-Pitch Technology: 2.5-year cycle; then equal DRAM @45nm/2010

Year of Production	2000	2001	2002 [July'02]	2003	2004	2005	2006	2007	2008 [July'08]	2009	2010	2012	2013	2015	2016	2018	2019	2020
Technology - Contacted M1 H-P (nm)	180	157	136 [130]	119	103	90	78	68	59 [65]	52	45		32		22		16	14

3-2-Yr Cycle]

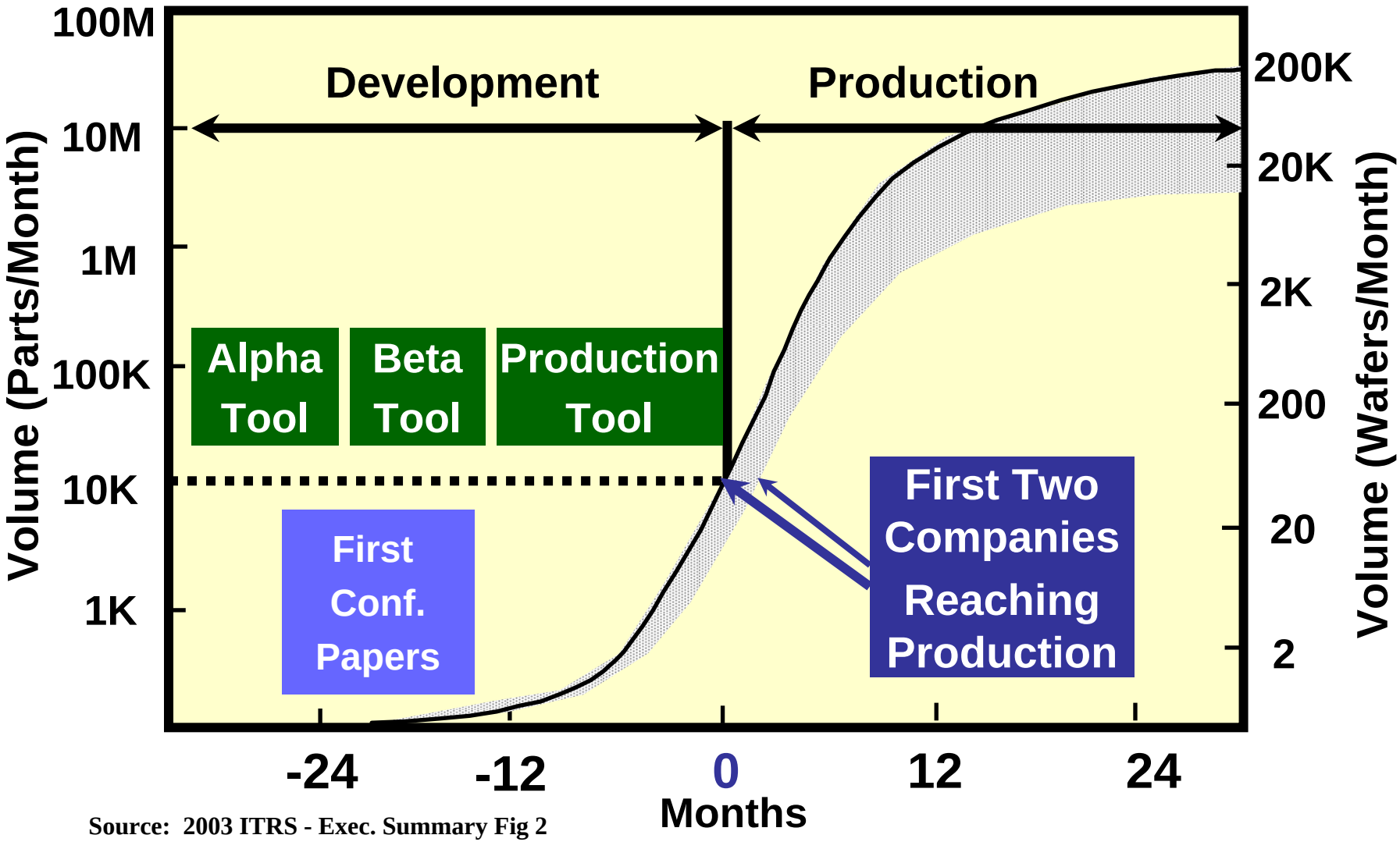
2.5-Year Technology Cycle

3-Year Technology Cycle

生産開始年の定義は２００３年版と同じ

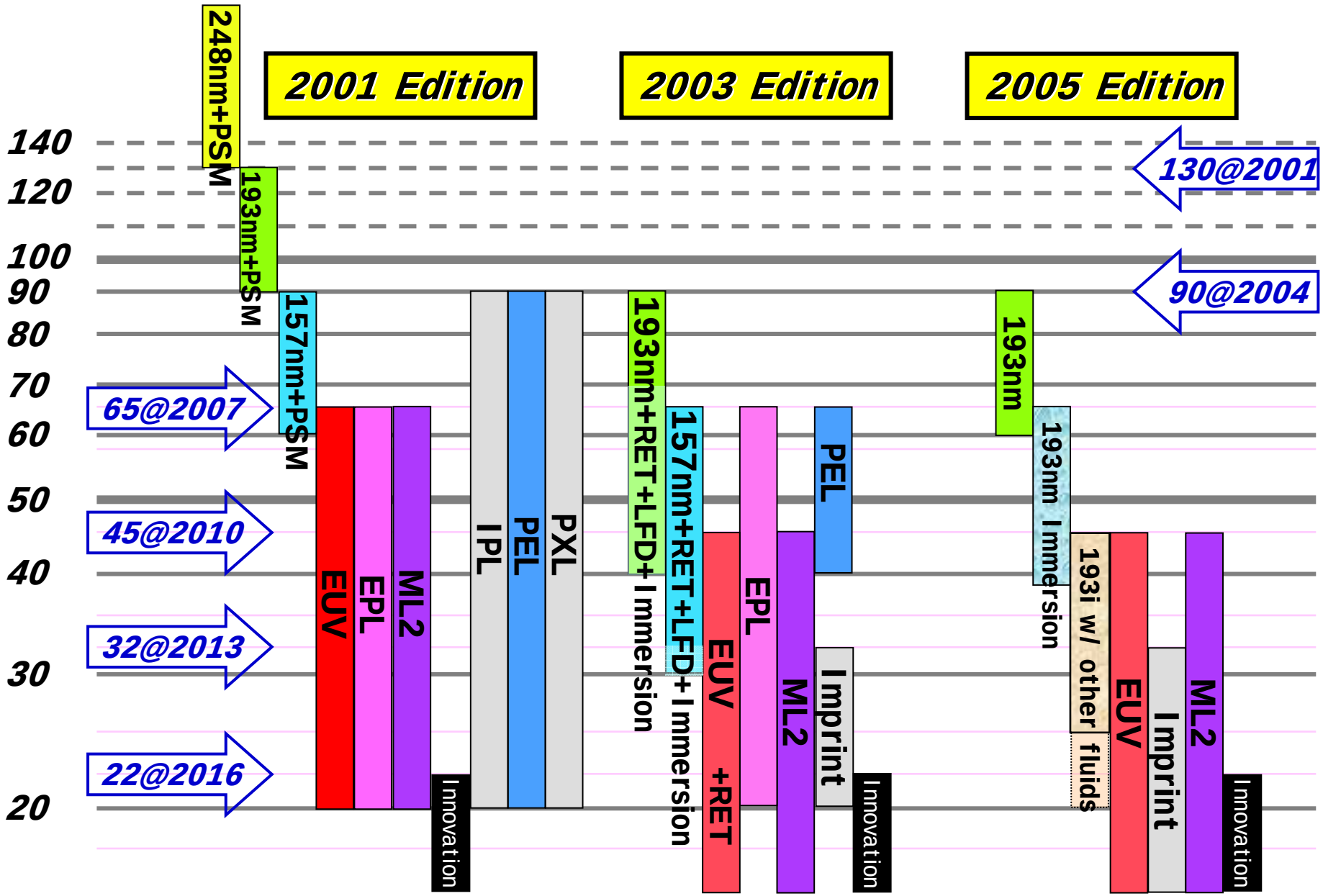
Cycle Timing

Production Ramp-up Model and Technology Node

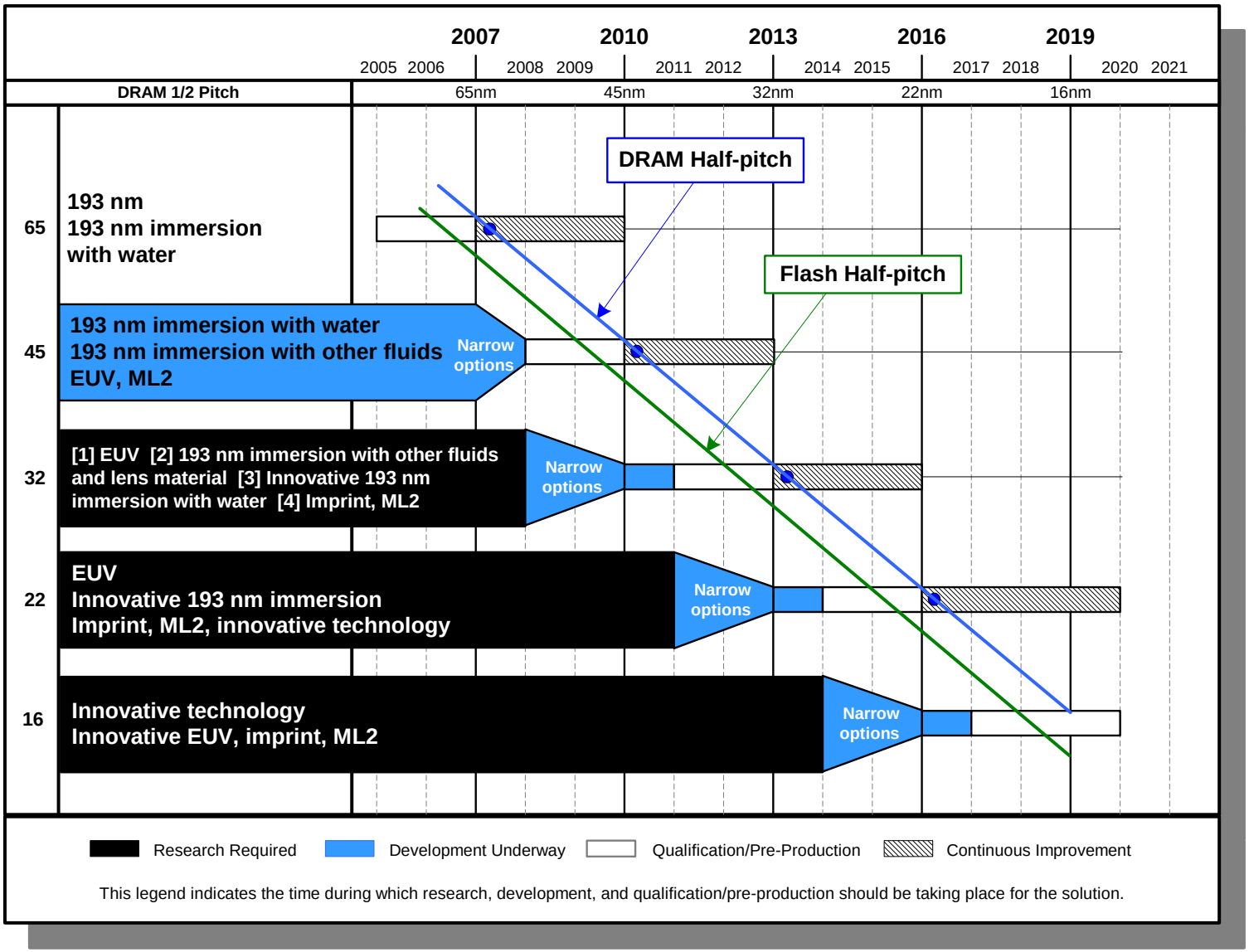


Source: 2003 ITRS - Exec. Summary Fig 2

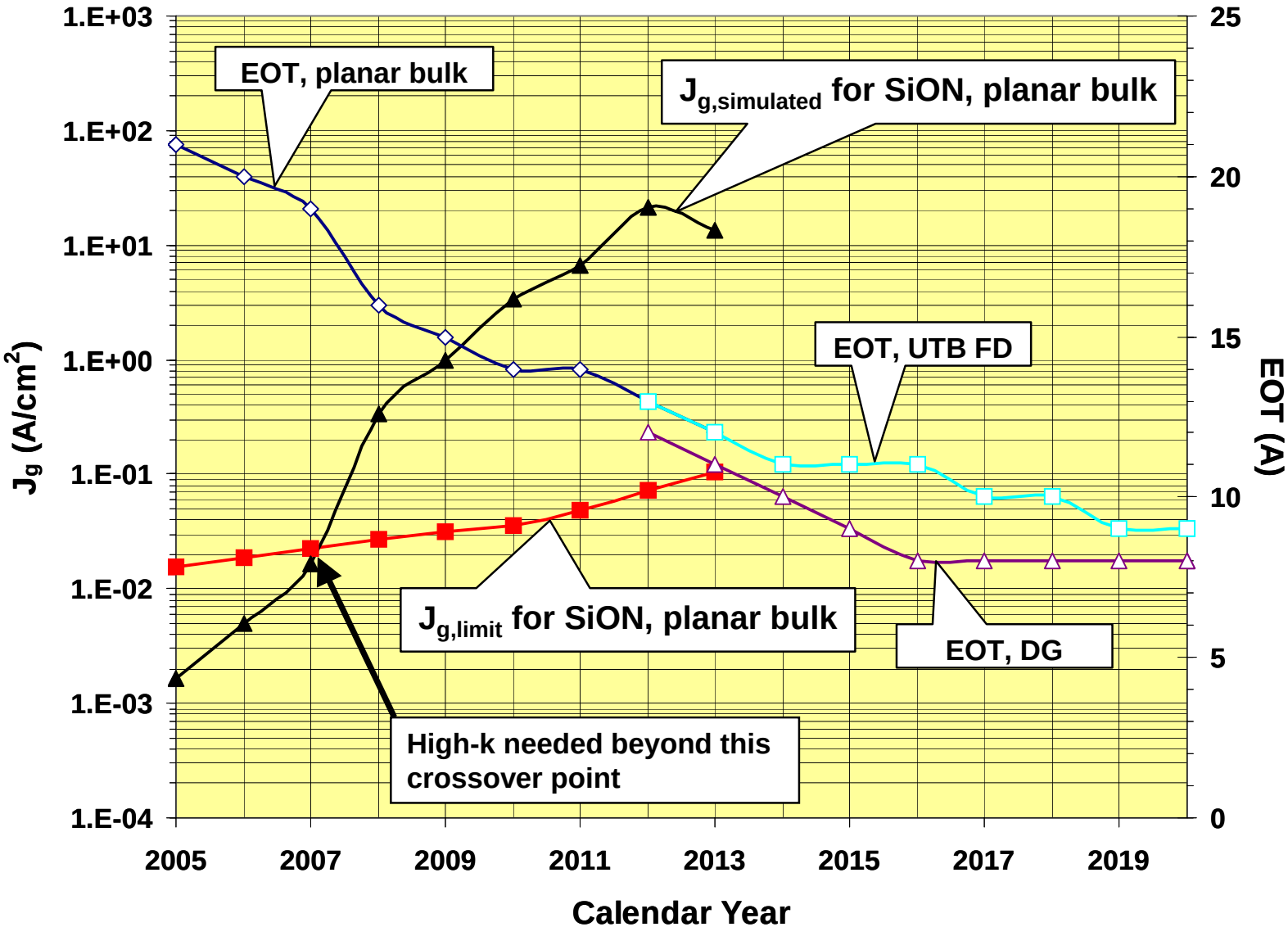
ITRSのリソグラフィーツールの変遷



リソグラフィーのロードマップ

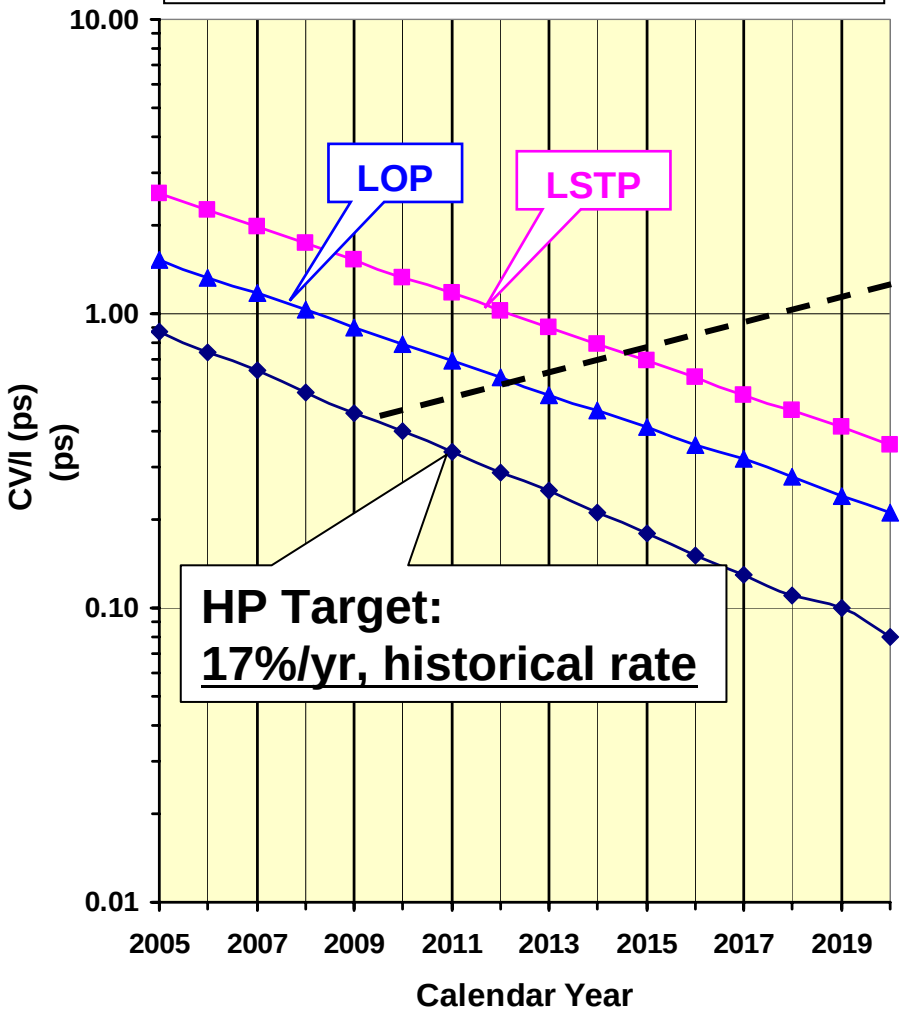


High-kゲート絶縁膜材料の導入時期は2008年以降
(LSTP: Low Standby Power)

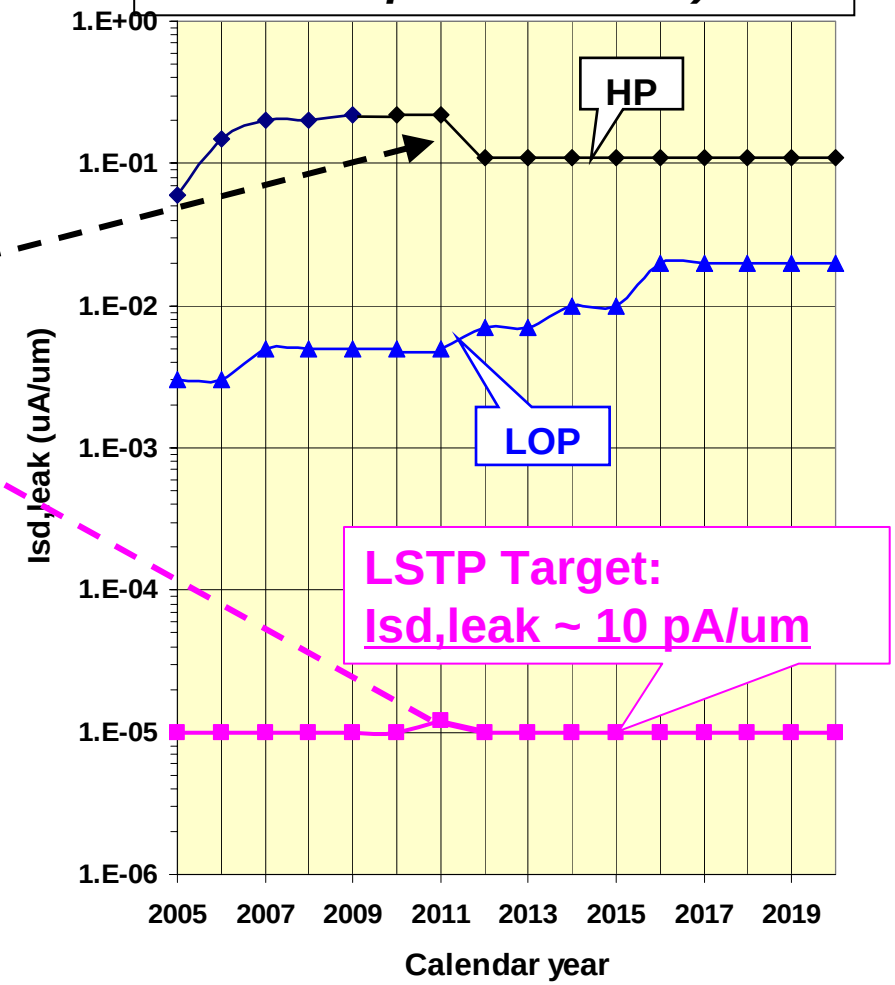


2005 ITRS: Low Power & High Performance (HP)

Intrinsic Transistor Delay,
$\tau = CV/I$
(lower delay = higher speed)

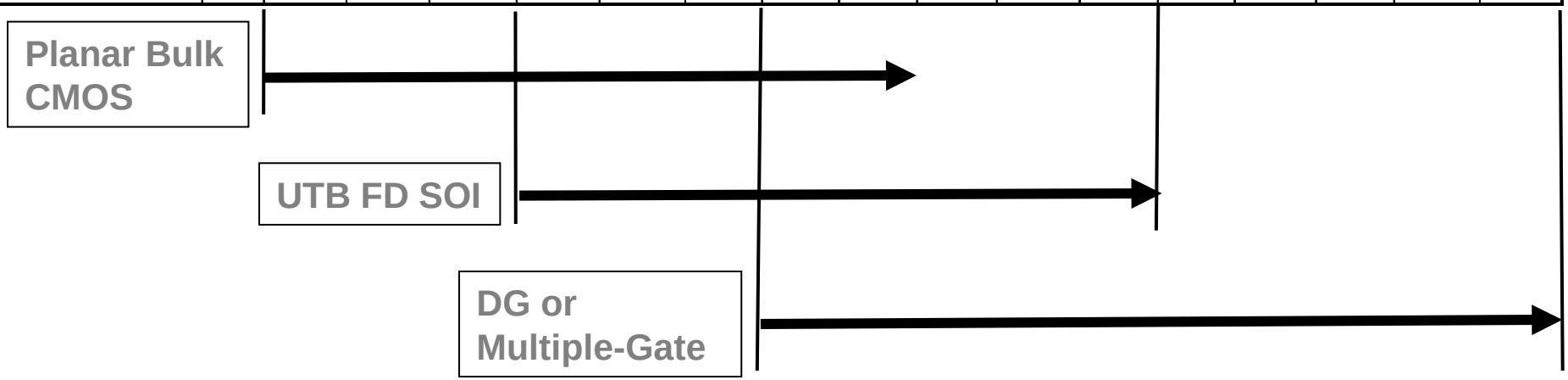


Leakage Current
(HP: standby power dissipation issues)



Multiple Parallel Paths (High Performance Logic)

Year in Production		2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
Physical Lgate (High Performance)	nm	32	28	25	22	20	18	16	14	13	11	10	9	8	7	6	5



Multiple parallel paths reflects most likely scenario:

- Some companies will extend planar bulk CMOS as long as possible
- Others will switch to FDSOI and/or multiple gate earlier
- Ultimate MOSFET is multiple gate
- Similar multiple paths for low-power logic

Multiple Parallel Paths (LSTP)

Year in Production	Units	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2017	2018	2019	2020
Technology Generation				lstp65			lstp45			lstp32			lstp22				lstp16	
# of years since 2005		0	1	2	3	4	5	6	7	8	9	10	11	12	12	13	14	15
Physical Lgate (Low-Standby-Power) (Bulk & DG)	nm	65	53	45	37	32	28	25	22	20	18	16	14	13	13	12	11	10
Physical Lgate (Low-Standby-Power) (FD)	nm								22	20	18	17	16	15	15	14	13	12

Planar Bulk

FDSOI and MG in parallel

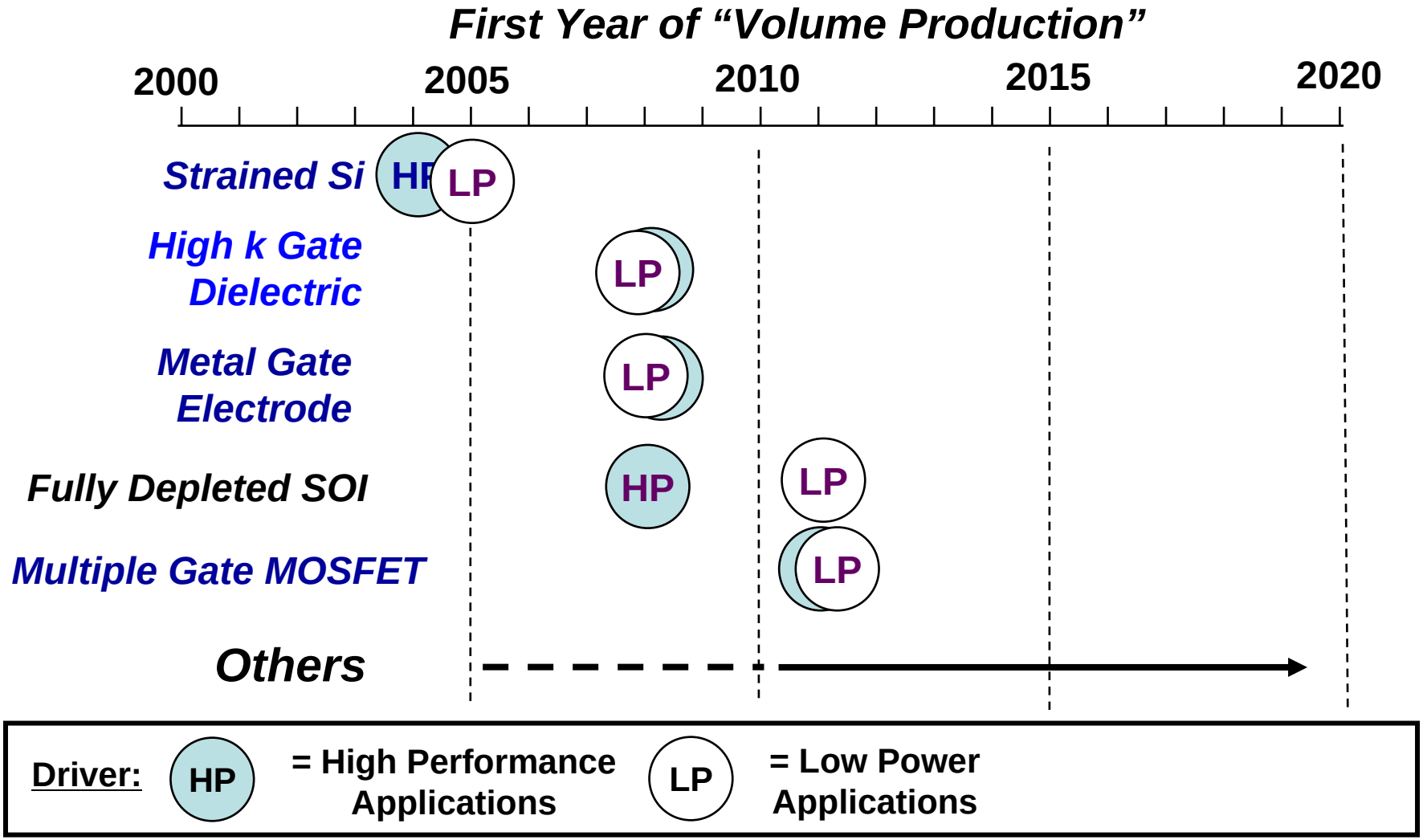
[FDSOI = Fully Depleted, Ultra-thin Body SOI]

[MG = Multiple Gate (e.g., FinFET)]

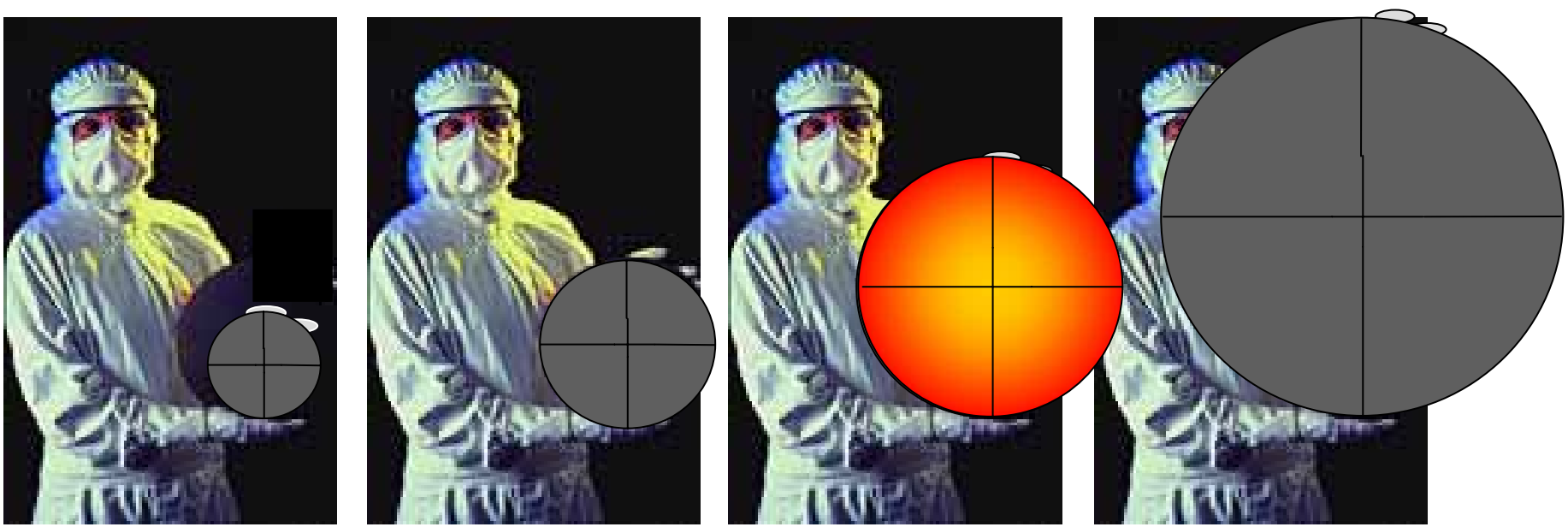
- **Approach**
  - **Extend planar bulk as long as possible**
  - **Implement FDSOI and MG in parallel**
  - **Slowed Lg scaling for FDSOI in latter years**

MOSトランジスタへの新技術導入: 2008年に複数の技術導入

The "CMOS Change Crunch" Multiple, Big Changes Over Next 7 Years



Wafer Size Conversion History



200mm/1990 | 300mm/2001 | **450mm/2012** | 675mm/2021?

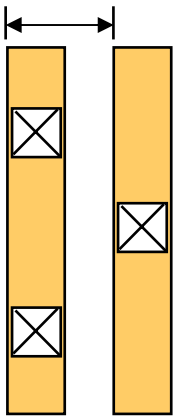
(125/150mm - 1981)

9 yrs + 2yrs delay* | **11 yrs + 0yrs delay** | **9 yrs + 0yrs delay**

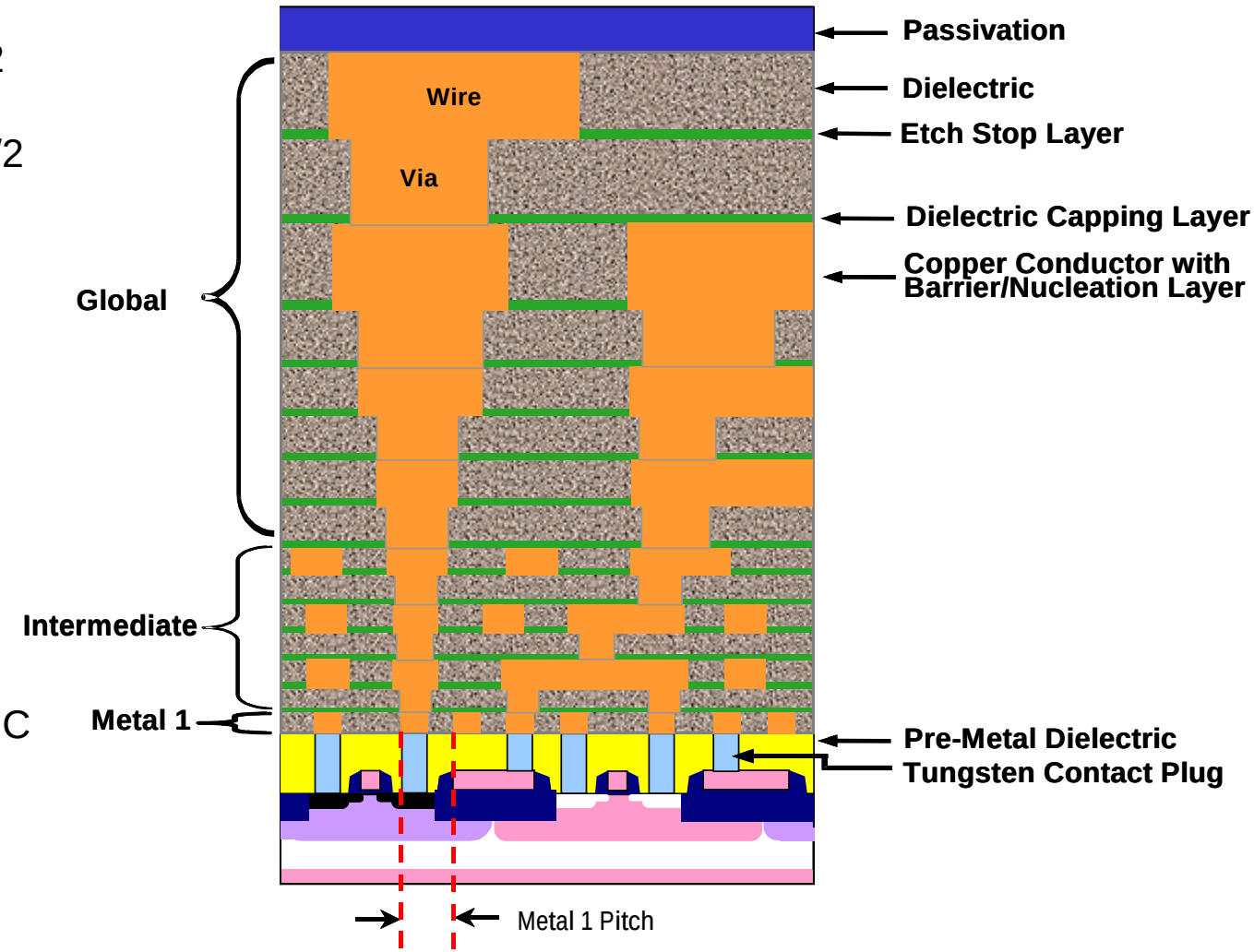
ロジックLSIの多層配線構造

DRAM ½ Pitch
= DRAM Metal Pitch/2
MPU/ASIC M1 ½ Pitch
= MPU/ASIC M1 Pitch/2

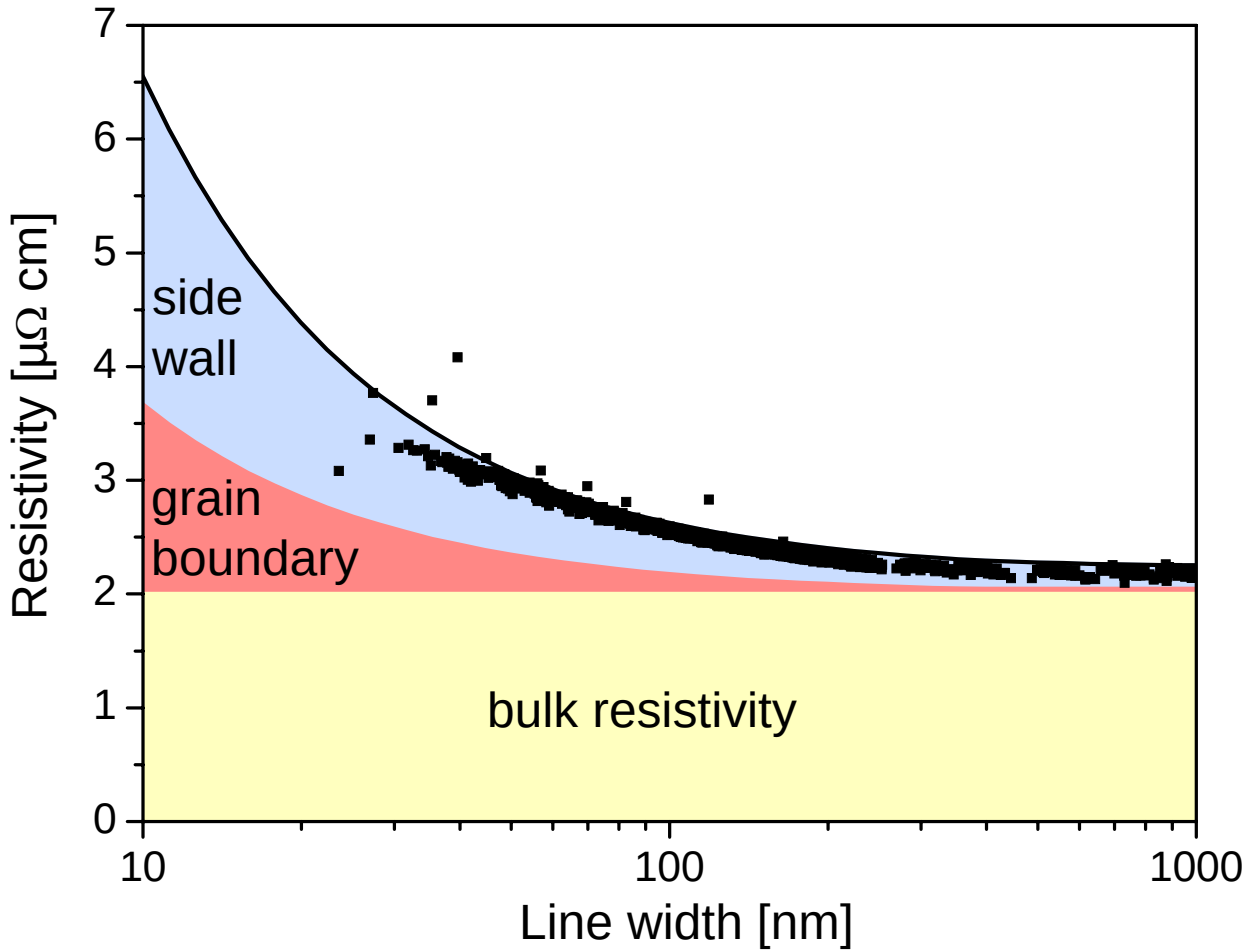
Metal Pitch



Typical DRAM/MPU/ASIC
Metal Bit Line



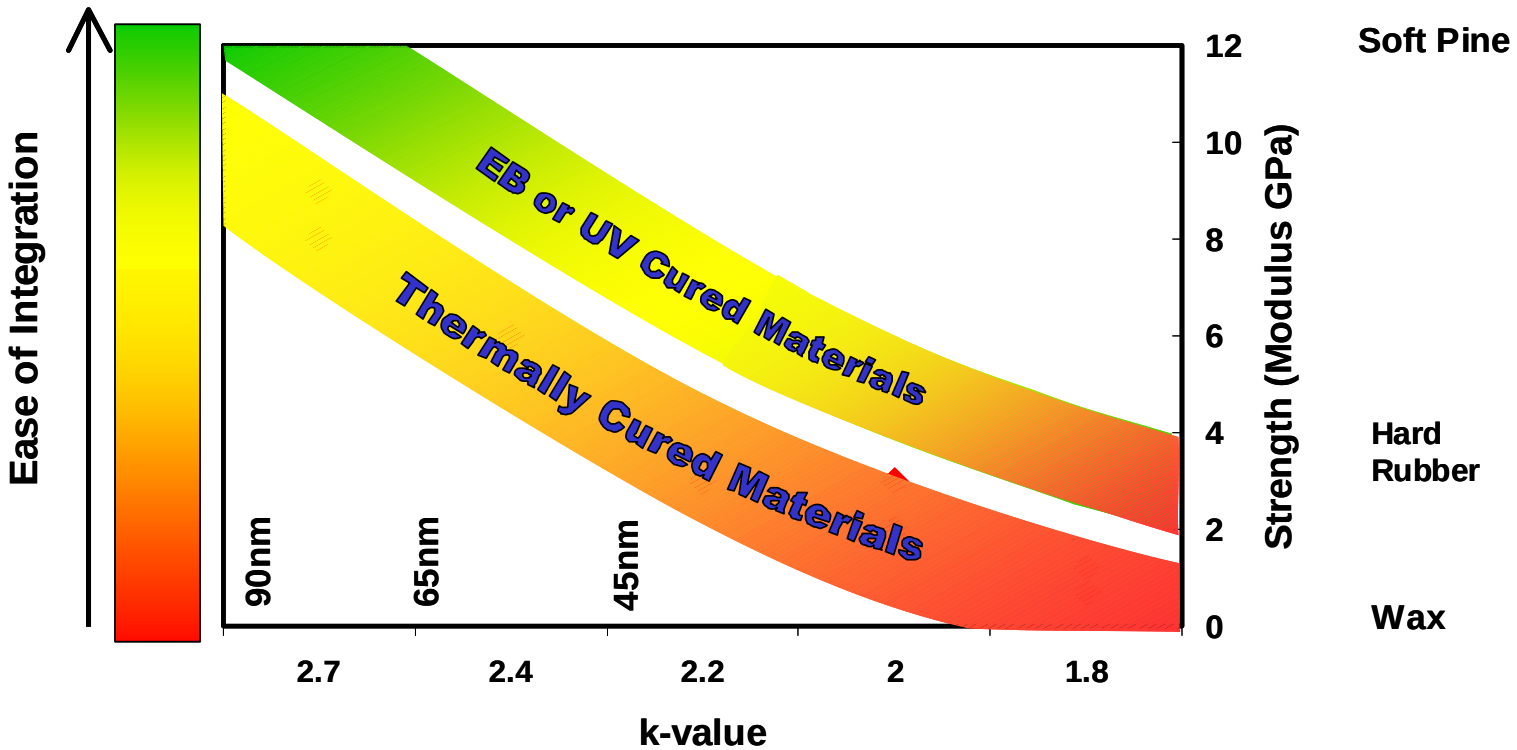
微細化に伴うCu配線抵抗の上昇



Source: Infineon Technologies

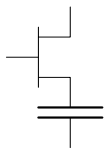
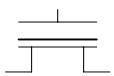
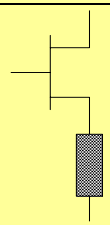
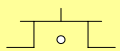
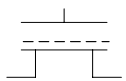
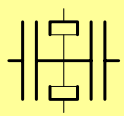
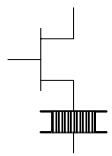
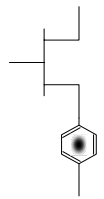
Low-k材料と機械的強度の両立

- Low k materials with k~2.7 are in manufacturing and materials with k~2.4 will be developed in 2~3 years.
- Securing mechanical properties of the Ultra Low k materials is a challenge.



Emerging Research Memory Devi

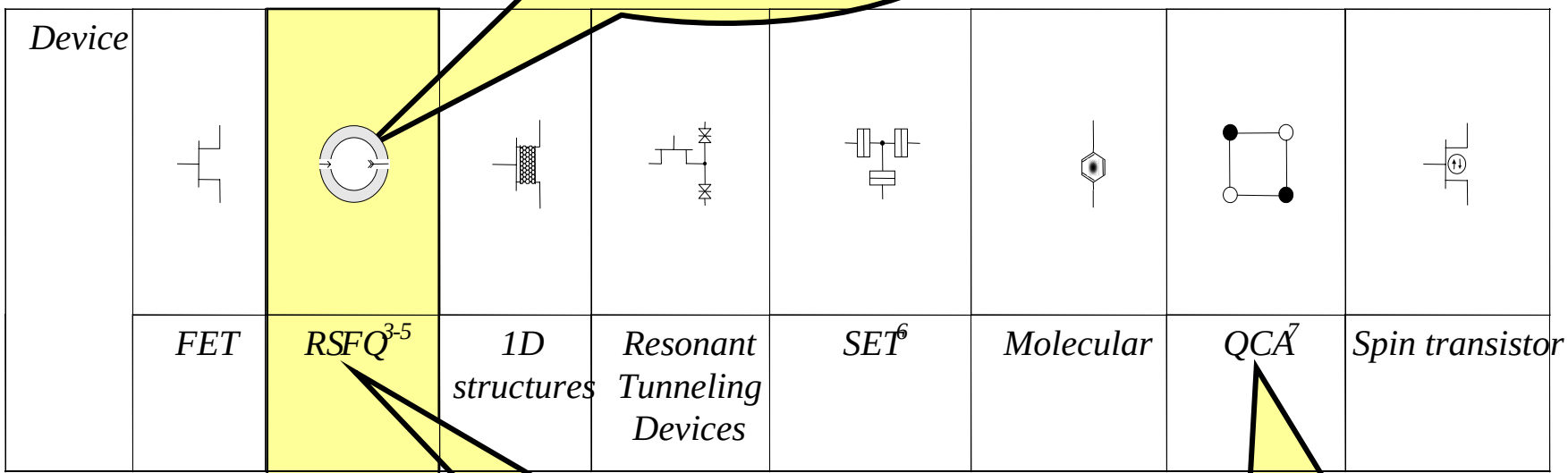
Remove SET Memory from 2005 ERD

Storage Mechanism	*Present Day Baseline Technologies*		*Phase Change Memory**	*Floating Body DRAM*	*Nano-floating Gate Memory***	*Single/F Electron Memories** *	*Insulator Resistance Change Memory***	*Molecular Memories***
								
Device Types	DRAM	NOR Flash	OUM	1TDRAM eDRAM	Engine… tu… ba… nano…			…ble
Availability	2004	2004	~2006	~2006		>2007	~2010	>2010
Cell Elements	1T1C	1T	1T1R	1T	1T	1T	1T1R	1T1R

Move to PIDS/FEP in 2005 ERD

Emerging Research Logic Devices

Replace with Ferromagnetic Logic



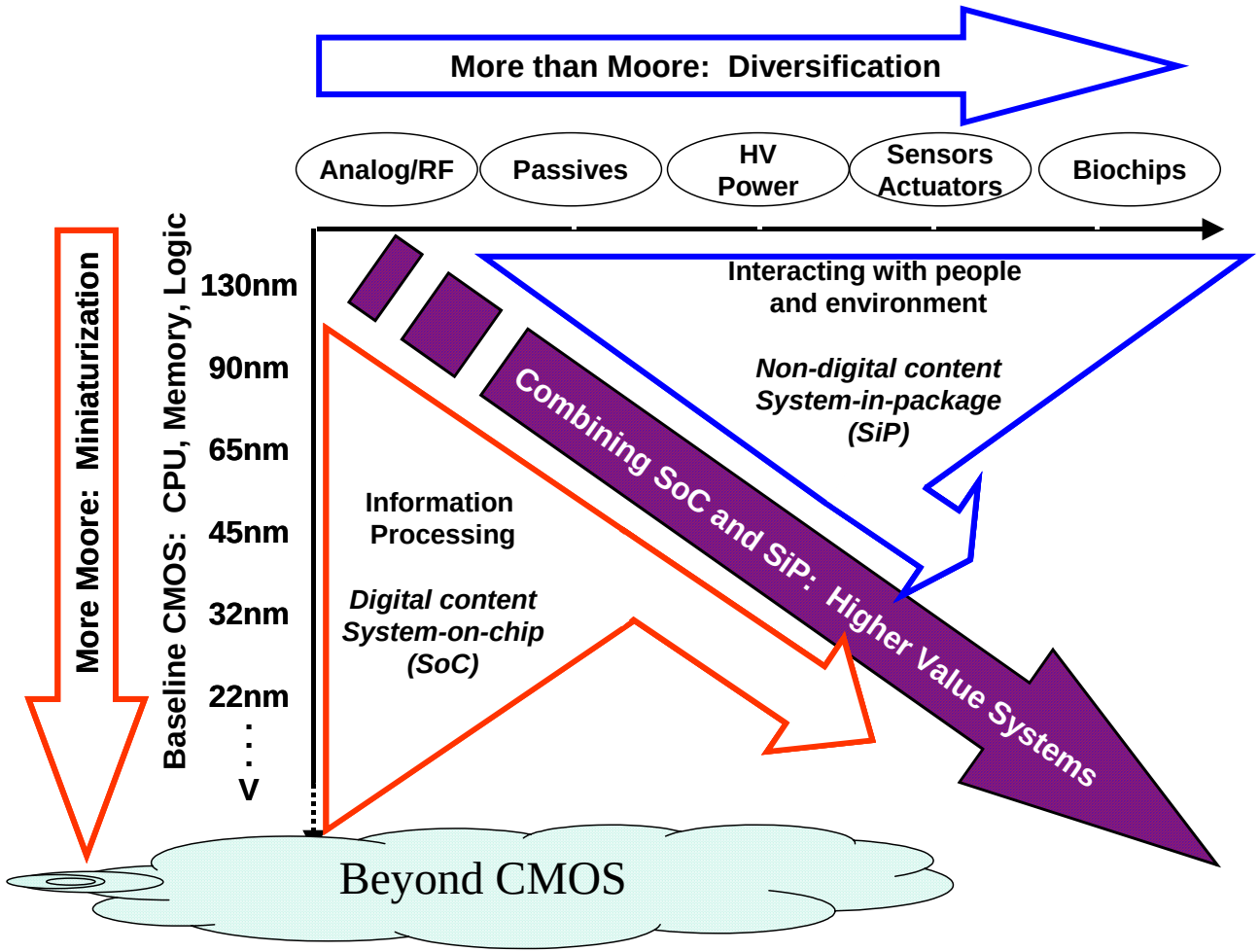
Device	FET	RSFQ[3-5]	1D structures	Resonant Tunneling Devices	SET[6]	Molecular	QCA[7]	Spin transistor

Remove RSFQ from 2005 ERD

Remove E:QCA from 2005 ERD

More Moore(微細化) と More than Moore (多様化)

Moore's Law & More



関連webサイトのURL

さらに詳しい資料については下記を参照願います

- **ITRSの公式ホームページ**
  - http://public.itrs.net/
  - ITRS 2005 Edition**はじめ、**ITRS**の最新情報**
- **JEITAのロードマップのホームページ**
  - http://strj-jeita.elisasp.net/strj/index.htm
  - ITRS 2003, 2001, 1999**の日本語訳**
  - ITRS**の過去の版 (英文)**
  - STRJ **(半導体技術ロードマップ専門委員会) の活動情報**