WG12: Emerging Research Devices (ERD)

新探究デバイス

－Beyond CMOS候補の位置付けと研究動向－

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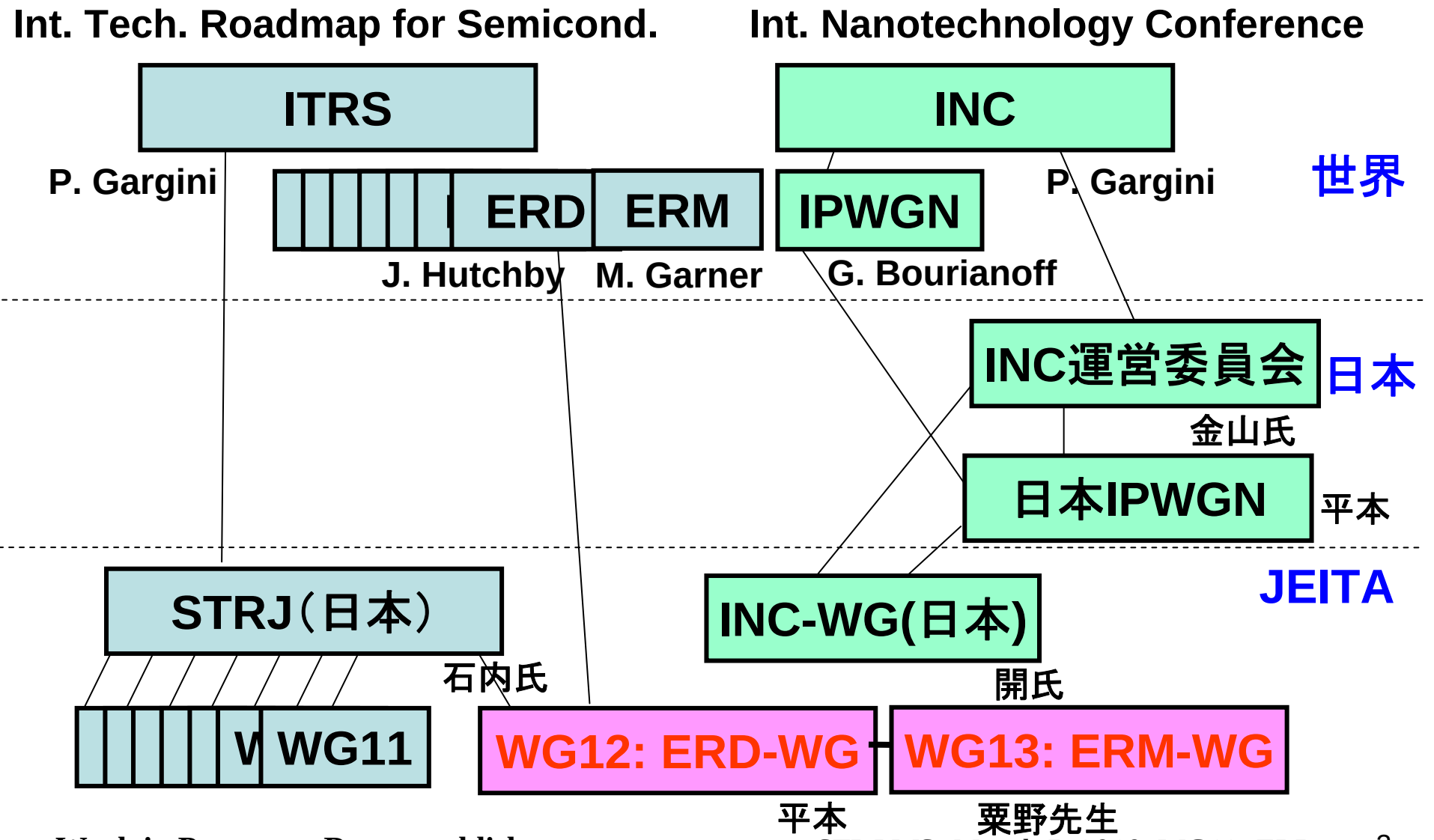
1. 日本のERD-WGの位置付け
2. ERDのスコープと目的
3. 2009年版の概要：ロジック，メモリ
4. ロジック・メモリデバイスの評価
5. カーボンベースナノエレクトロニクス
6. まとめ

用語集

BISFET	Bilayer PseudoSpin Field-Effect Transistor
CNT	Carbon Nanotube
ERD	Emerging Research Device
ERM	Emerging Research Material
FET	Field Effect Transistor
GNR	Graphene Nano Ribbon
INC	International Nanotechnology Conference
IPWGN	International Planning WG for Nanoelectronics
MRAM	Magnetic RAM
NEMS	Nano Electro Mechanical Systems
NW	Nano Wire
PCM	Phase Change Memory
QCA	Quantum Cellular Automata
SET	Single Electron Transistor
STT	Spin Torque Transfer

ERD-WGの位置付け


Int. Tech. Roadmap for Semicond.
Int. Nanotechnology Conference
ITRS
INC
P. Gargini
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世界
ERD
ERM
IPWGN
J. Hutchby
M. Garner
G. Bourianoff
INC運営委員会
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石内氏
開氏
WG11
WG12: ERD-WG
WG13: ERM-WG
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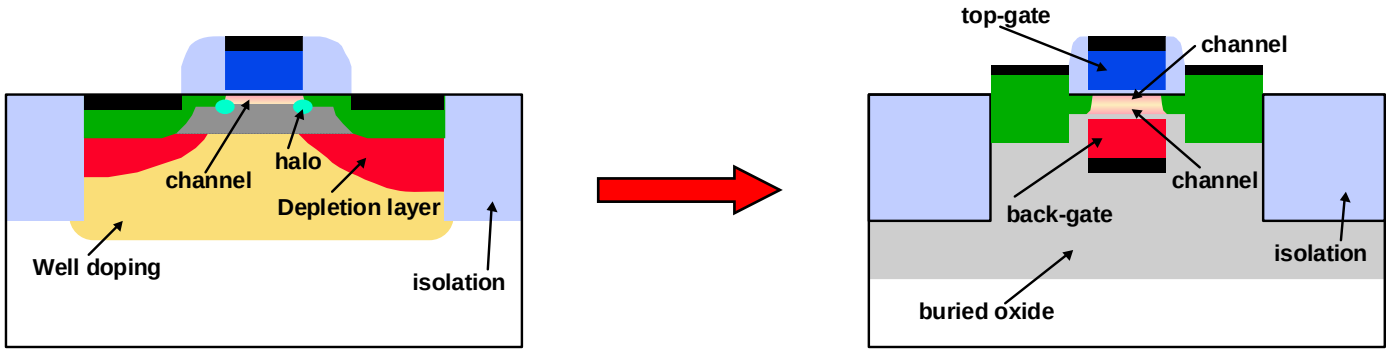
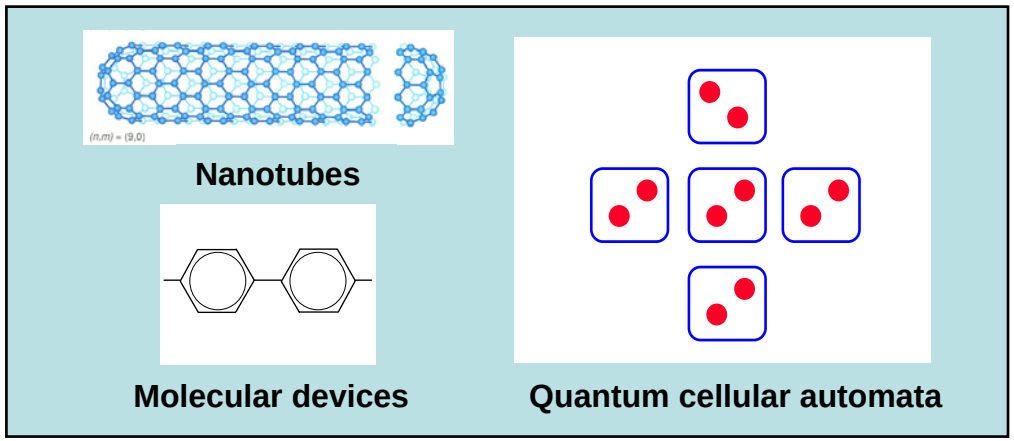
2003年版までのERDのスコープ



Bulk CMOS

Double-Gate CMOS

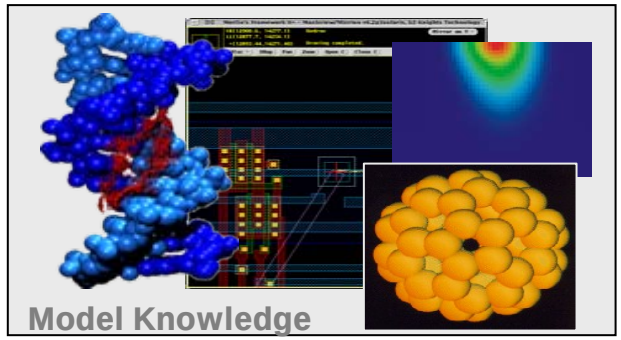
New Memory and Logic Technologies



New Architecture Technologies

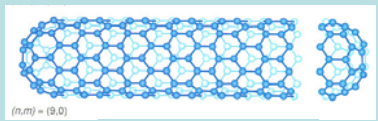
Emerging Information Processing Concepts

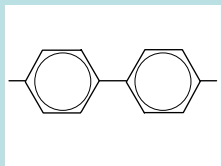
2005年版ERDのスコープ

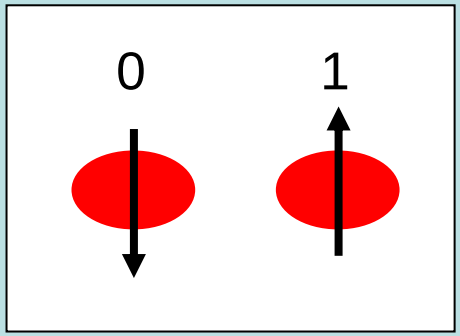


新材料

新メモリとロジック技術





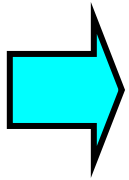


新アーキテクチャ技術

新情報処理のコンセプト「Beyond CMOS」

求められる機能

- 要求される特性:
  - スケーラビリティ
  - 性能
  - エネルギー効率
  - 利得
  - 信頼性
  - 室温動作
- 望まれる特性:
  - CMOSプロセスとの互換性
  - CMOSアーキテクチャとの互換性



他の状態変数
(電荷だけでなく)

- スピン状態
- 分子状態
- 強相関電子状態
- 位相状態
- 量子状態
- 磁気単一量子磁束
- 機械的変形
- ダイポール

ERDの目的

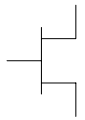
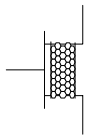
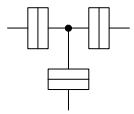
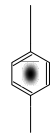
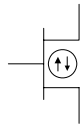
1. 新材料導入，異種デバイス集積化等によるCMOSプラットフォームの延長.
2. 原理の全く異なるデバイスによる情報処理技術の変革.

最近の動き

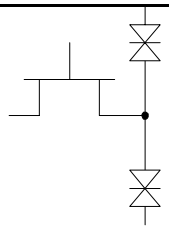
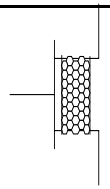
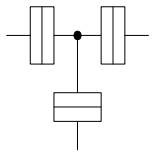
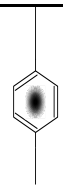
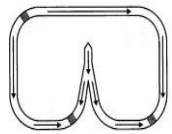
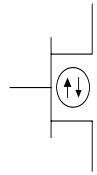
1. 2005年版では新原理デバイス（Beyond CMOS）が主流.
2. 日本の主張により2007年版からCMOSとの融合を強調.
3. 2009年版でさらにその流れが強まる.
4. 2008年7月にBeyond CMOSの絞り込みの議論.
5. 2010年4月にはメモリの絞り込みの議論を行う予定.

2007 ITRS ERD

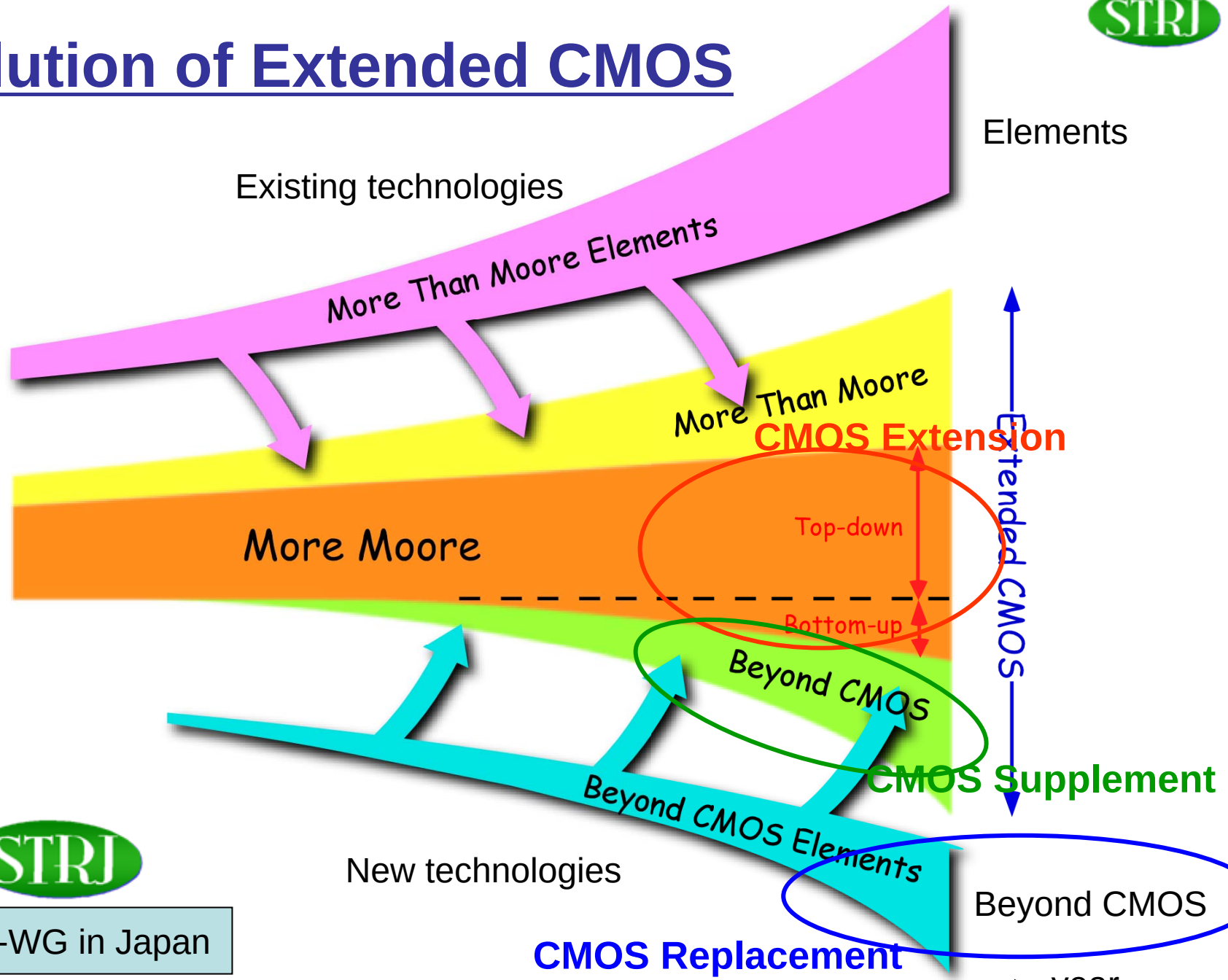
CMOS Scaling & Replacement Devices (1st)

Device							
	FET	**CMOS Extension 低次元構造**	**CMOS Extension III-V チャネル**	**単電子トランジスタ**	**分子**	**強磁性ロジック**	**スピントランジスタ**
	Ref.	**CMOS Extension**			**Beyond CMOS**		
Types	Si CMOS	•CNT FET •NW FET •NW hetero-structures •Nanoribbon transistors	•III-V compound semiconductor channel replacement	SET	•2-terminal •3-terminal FET •3-terminal bipolar transistor •NEMS •Molecular QCA	•Moving domain wall •Hybrid Hall effect •Magnetic Resistive Element •M: QCA	•Spin Gain transistor •HMF Spin MOSFET •Spin Torque Transistor
Supported Architectures	Conventional	Conventional	Conventional	Threshold logic	Memory-based QCA	Lithographically defined	conventional

CMOS Supplement Devices (2nd Table)

						
Device	共鳴トンネルダイオード	マルチフェロイックトンネル接合	単電子トランジスタ	分子デバイス	強磁性デバイス	スピンデバイス
State variable	Charge	Dielectric and magnetic domain polarization	Charge	Molecular Conformation	Ferromagnetic polarization	Precession frequency
Response function	Negative differential resistance	Four resistive states	Coulomb blockade	Hysteritic	Non-linear	Nonlinear

Evolution of Extended CMOS



ERD-WG in Japan

2009年版のロジックテーブル分類

Titles for the three Emerging Research Logic Tables

Table 1: MOSFETS: Extending the channel to the End of the Roadmap

Table 2: Charge based Beyond CMOS: Non-Conventional FETs and other Charge-based information carrier devices

Table 3: Alternative Information Processing Devices

Logic: Table 1 (CMOS Extension)

Device		FET [A]						
Typical example devices		Si CMOS	CNT FET	Graphene Nanoribbon FET	Nanowire	III-V FETs	Ge FETs	Unconventional geometries FinFET
Cell Size (spatial pitch) [B]	Projected	100 nm	100 nm [D]	100 nm [I]	30 nm [??]	15 nm	15nm	100 nm [C]
	Demonstrated	590 nm	~1.5 0m [E]	1.5 µ [J]	~1 µ [M]	40nm [GE] ?	26nm [GA] ?	300 nm [T]
Density (device/cm^2)	Projected	1.00E+10	4.50E+09	4.50E+09	1E11 [???]	1.00E+11	1.00E+11	1E10 [C]
	Demonstrated	2.80E+08	4.00E+07	4.00E+07	1E8 [????]	1.5E10 [GF]	3E10 [GB]	4.7E9[U]
Switch Speed	Projected	12 THz	6.3 THz [F]	???	6.5 THz [Q] [N]]	N/A	N/A	12 THz [C]
	Demonstrated	1.5 THz	4GHz [G]	26 GHz[K]	250 GHz [O]	2THz [GG]	290GHz [GC]	> 200 GHz[V]
Circuit Speed	Projected	61 GHz	61 GHz [C]	61 GHz [C]	100 GHz [P]	N/A	N/A	61GHz [C]
	Demonstrated	5.6 GHz	220 Hz [H]	22 kHz[L]	11.7 MHz [Q]]	N/A	N/A	8 GHz[W]
Switching Energy, J	Projected	3.00E-18	3.00E-18	3.00E-18	4E-20J [R]	N/A	N/A	3E-18 [C]
	Demonstrated	1.00E-16	1E-11 [H]	??????	6.0 E-16J [S]]	N/A	4.0E-15 [GD]	N/A
Throughput, GBit/ns/cm^2	Projected	238	238	61	1.00E-04	N/A	N/A	238 [C]
	Demonstrated	1.6	1.00E-08	Data not available	1.20E-04	N/A	N/A	N/A
Operational Temperature		RT	RT	RT	RT	RT	RT	RT
Materials System		Si	CNT, Graphene		Si, Ge, III-V, II-VI, In_2O_3, ZnO, TiO_2, SiC	InGaAs, InAs, InSb	InGaAs, InAs, InSb	Ge
Research Activity [AD]			171	???	447			

Logic: Table 2 (Charge-Based)

Device		FET [A]				Spin Transistor		
Typical example devices		Si CMOS	Tunnel FET	I-MOS	Negative Cg FET	Spin FET	Single Electron Transistor	MEMS
bCell Size (spatial pitch) [B]	Projected	100 nm	All-silicon tunnel Strained Ge or III-V Heterostructure	100 nm	100 nm [same as CMOS]	100 nm for spin MOSFET	40 nm [L]	100 nm W3
	Demonstrated	590 nm	Projected: 20nm [U1] Demonstrated: 70 nm, 100nm [U2, U3]	2000 nm	N/A	~1□m (channel length) for Spin FET [ST3]	~200 nm [H, I]	900 nm
Density (device/cm^2)	Projected	1.00E+10	Not known: channel length scalable down to	1.00E+10	1E10 [same as CMOS]	~1E10 for spin MOSFET [ST3]	6.00E+10	1.00E+10
	Demonstrated	2.80E+08	~1E10	2.50E+07	N/A	Not investigated	~2E9	1 /cm**2 W2
Switch Speed	Projected	12 THz	Not known	> 1 THz	1 THz [based on 1 nm movement of dipoles with a	~10 THz or less for spin MOSFET [ST4]	10 THz [M]	1 GHz W4
	Demonstrated	1.5 THz	Si/Ge/IIIAs tunneling source: 1GHz/ 1 THz/ 3 THz [U1]	not known	N/A	30GHz for Spin FET [ST3]	2 THz [N]	0.18 GHz W5
Circuit Speed	Projected	61 GHz	Not known	61 GHz	~10 GHz (based on 1THz switch speed estimate)	~10GHz or less for spin MOSFET [ST4]	1 GHz [L]	1 GHz
	Demonstrated	5.6 GHz	Not known: will depend on the source material used	not known	N/A	Not investigated	1 MHz [F]	.18 GHz
Switching Energy, J	Projected	3.00E-18	Not known	3.00E-16	1.00E-19	1E-17-1E-18 for spin MOSFET [ST4]	1×10^{-18} [L] [$>1.5\times10^{-17}$] [O]	5E -17 J W 6,W7
	Demonstrated	1.00E-16	Si/Ge/IIIAs tunneling source: 90/90/3000E-18 J/um at VDD=0.5V, L=20nm [U1]	not known	N/A	Not investigated	8×10^{-17} [P] [$>1.3\times10^{-14}$] [O]	
Binary Throughput, GBit/ns/cm^2	Projected	238	Not known	not known	Not known	~200	10	10

Logic: Table 3 (Alternatives)

	Collective spin devices	Moving Domain wall	Atomic switch	Molecular	Pseudospi ntronc	Nano magnetic
State Variable	Spin	Polarization, magnetization	metal cations / atoms	Molecular configuration	Charge distribution symmetry in two layers	Magneric polarization patterns
Response Function	Sinusoidal, various	Non linear	Non-linear	Nonlinear, NDR	Gate controlled NDR	Non linear
Class—Example	Spin Wave Mach Zender	Ferromagnetic wire devices	Programable logic	Combinatorial logic circuits	Bilayer Pseudospin Field Effent Transistor	MQCA majority gate
Architecture	Morphic	Morphic	Morphic, cross bar	Morphic	Morphic	Morphic
Application	Signal Processing	Low power, reconfigurable logic	Non volitale logic	Combinatorial logic circuits	General purpose logic	General purpose logic
Comments			Low resistance, low power		Extremely low power	Low power, high density
Status	Demonstrated	Simulated	Demonstrated	Simulated	Simulated, theory	Demonstrated
Material Issues	High propagation loss, slow propagation velocity	High permeability material required			Low defect bilayer graphene, contacts	

Memory

		Capaciatnce-based	Resistance-based						
		Ferroelectric FET memory	**Nanomechanical Memory**	**Spin Torque Ttransfer Memory**	**Nanothermal Memory**	**Nanoionic Memory**	**Electronic Effects Memory**	**Macromolecular Memory**	**Molecular Memories**
Storage Mechanism		Remnant polarization on a ferroelectric gate dielectric	Electrostatically-controlled mechanical switch	Magnetization of the ferromagnetic layer	Thermo-chemical redox process, 2) Thremal phase	Ion transport and redox reaction	Multiple mechanisms	Multiple mechanisms	Multiple mechanisms
Cell Elements		1T	1T1R or 1D1R	1T1R	1T1R or 1D1R	1T1R or 1D1R	1T1R or 1D1R	1T1R or 1D1R	1T1R or 1D1R
Device Types		FET with FE gate insulator	1) nanobridge/ cantilever 2) telescoping CNT 3) Nanoparticle	Magnetization change by spin transfer torque	1) Fuse/Antifuse Memory 2) nanowire PCM	1) cation migration 2) anion migration	1) Charge trapping 2) Mott transition 3) FE barrier effects	M-I-M (nc)-I-M	Bi-stable switch
Feature size F	Min. required	<65 nm	<65 nm	<65 nm	<65 nm	<65 nm	<65 nm	<65 nm	<65 nm
	Best projected	22 nm [A1]	5-10 nm [B1]	7-10 nm	5-10 nm	5-10 nm	5-10 nm	5-10 nm	5 nm [H1]
	Demonstrated	~2 m [A2]	180 nm [B2]	50 nm [C1]	180 nm [D1]	90 nm [E1]	1 m [F1]	250 nm [G1]	30 nm [H2]

Fundamental Guiding Principles

1. ***Computational State Variable(s) other than Solely Electron Charge***
2. ***Non-thermal Equilibrium Systems***
3. ***Novel Energy Transfer Interactions***
4. ***Nanoscale Thermal Management***
5. ***Sub-lithographic Manufacturing Process***
6. ***Alternative Architectures***

Critical Assessment (評価)

	Scalability [1]	Performance [2]	Energy Efficiency [3]	Gain [4]	Operational Reliability [5]	Operational Temperature [6]	CMOS Technological Compatibility [7]	CMOS Architectural Compatibility [8]
Unconventional Geometry MOSFETs (Gate-all-around MOSFETs, etc.)	2.4	2.4	2.3	2.1	2.1	2.5	2.3	2.6
CNT MOSFETs	2.4	2.4	2.4	2.1	2.1	2.6	1.9	2.8
Nanowire MOSFETs	2.4	2.2	2.3	2.1	2.1	2.5	2.2	2.6
Ge MOSFETs	2.0	2.5	2.2	2.2	1.9	2.5	2.3	2.7

Carbon-Based Nanoelectronics

Table ERD8: Research and Technology Development Schedule proposed for Carbon-based Nanoelectronics to impact the Industry's Timetable for Scaling Information Processing Tech

First Year of IC Production	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024
CMOS Extension Devices																
CNT and Graphine Devices																
Controlled growth																
Chiraliy of CNTs																
Semiconducting vs metallic																
n/p Doping Control																
Diameter of CNTs																
Direction of CNTs																
Wall thickess - Single wall																
Graphene Epitaxy																
Edge Control of Graphene																
Bandgap Control of Graphene																
Ohmic contacts																
Hi-K Gate dielectric & gate metal																
Heterobandgap junction structures																
Beyond CMOS Devices																
CNT Devices																
NEMS																
Molecular Electronics																
Graphine Devices																
Veselago Electron Lens																
Pseudospintronics																
Quantum Interference																
Quantum Hall Effect																
Bi-layer structures																

Narrow Options

This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.

Research Required
Development Underway
Qualification / Pre-Production
Continuous Improvement

まとめ

1. CMOSの延長技術の研究が進展．大きな期待が寄せられている．
2. Beyond CMOSのみで情報処理を行うことは困難との考え方がさらに広まる．Beyond CMOSがCMOSに融合する考え方が一般化．
3. もっとも集中すべきBeyond CMOSとしてカーボンベースナノエレクトロニクスのロードマップを作成．