WG5 (リソグラフィWG)活動報告 「光延命とEUVの現状」

NECエレクトロニクス㈱　内山　貴之

－内容－

- WG5(リソグラフィWG)の活動体制
- ITRS2009リソグラフィの概要
- リソグラフィの現状と課題
  - 光リソグラフィの延命と課題
  - EUVリソグラフィ技術の現状と課題
- 2010年度の活動方針
- まとめ

略語

NA	Numerical Aperture	
CD	Critical Dimension, CDU (CD Uniformity)	
DOF	Depth of Focus	
LER/LWR	Line Edge Roughness/Line Width Roughness	
RET	Resolution Enhancement Techniques	
OAI	Off-Axis Illumination	
PSM	Phase Shifting Mask	cPSM (complementary PSM), APSM (Alternating PSM), EPSM (Embedded PSM), Att. PSM (Attenuated PSM)
EDA	Electronic Design Automation	
OPC	Optical Proximity Corrections, RB/MBOPC (Rule Base/Model Base OPC)	
DFM	Design for Manufacturing/Design for Manufacturability	
SB/SRAF	Scattering Bar/Sub Resolution Assist Feature™	
MEEF	Mask Error Enhancement Factor (=MEF)	
ARC	Anti-Reflection Coating, BARC (Bottom ARC), TARC (Top ARC)	
AMC	Airborne Molecular Contamination	
DE	Double Exposure	
DP	Double Patterning	
SADP	Self Aligned DP	
ESD	Electro Static Discharge	
NGL	Next Generation Lithography	
EUVL	Extreme Ultraviolet Lithography	
ML2	Maskless Lithography	
NIL	NanoImprint Lithography	
UV-NIL	Ultraviolet NIL	
SFIL	Step & Flash Imprint Lithography	
DSA	Directed Self Assembly	

WG5(リソグラフィWG)の活動体制

ーJEITA半導体部会/関連会社ー

- **内山 貴之/リーダー** (NECEL)
- **笹子 勝 /サブリーダー** (**パナソニック**)
- **羽入 勇** (**富士通マイクロエレクトロニクス**)
- **須向 一行** (**ルネサステクノロジ**)
- **東川 巌** (**東芝**)
- **守屋 茂 ➔川平　博一**(**ソニー**)
- **和田 恵治** (**ローム**)
- **田中 秀仁** (**シャープ**)
- **山口 敦子** (**日立製作所**)

ーコンソーシアムー

- **山部 正樹/事務局** (ASET-D2I)
- **寺澤 恒男** (Selete)
- **笠間 邦彦** (EUVA)

ーSEAJ、他ー

- **森 晋 ➔ 奥村　正彦** (SEAJ:　**ニコン**)
- **龜山 雅臣➔ 奥村　正彦 /国際担当**　(**ニコン**)
- **山田 雄一** (SEAJ:　**キヤノン**)
- **中島 英男** (SEAJ:　TEL)
- **山口 哲男** (SEAJ:　**ニューフレアテクノロジィ**)
- **大久保 靖** (HOYA)
- **林 直也** (**大日本印刷**)
- **外岡 要治 ➔菊地　保貴** (**凸版印刷**)
- **小野寺 純一 ➔佐藤　和史**(**東京応化工業**)
- **栗原 啓志郎** (**アライアンスコア**)

計　21名

ITRS Lithography Technology Requirements

ITRS 2009

Year of Production	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019
DRAM ½ pitch (nm) (contacted)	52	45	40	36	32	28	25	23	20	18	16
DRAM											
DRAM ½ pitch (nm)	52	45	40	36	32	28	25	23	20	18	16
CD control (3 sigma) (nm) [B]	5	4.7	4.2	3.7	3.3	2.9	2.6	2.3	2.1	1.9	1.7
Contact in resist (nm)	57	50	44	39	35	31	28	25	22	20	18
Contact after etch (nm)	52	45	40	36	32	28	25	23	20	18	16
Overlay [A] (3 sigma) (nm)	10	9.0	8.0	7.1	6.4	5.7	5.1	4.5	4.0	3.6	3.2
k1 193 / 1.35NA	0.36	0.31	0.28	0.25	0.22	0.20	0.18	0.16	0.14	0.12	0.11
k1 EUVL		0.83	0.74	0.66	0.59	0.52	0.47	0.58	0.52	0.46	0.41
Flash											
Flash ½ pitch (nm) (un-contacted poly)	38	32	28	25	23	20	18	16	14	13	11
CD control (3 sigma) (nm) [B]	4	3.3	2.9	2.6	2.3	2.1	1.9	1.7	1.5	1.3	1.2
Contact Pitch (nm)	219	190	170	151	135	120	107	95	85	76	67
Contact after etch (nm)	52	45	40	36	32	28	25	23	20	18	16
Overlay [A] (3 sigma) (nm)	12	10.5	9.4	8.3	7.4	6.6	5.9	5.3	4.7	4.2	3.7
k1 193 / 1.35NA	0.26	0.22	0.20	0.18	0.16	0.14	0.12	0.11	0.10	0.09	0.08
k1 EUVL		0.61	0.55	0.49	0.43	0.39	0.33	0.41	0.37	0.33	0.29
MPU											
MPU/ASIC Metal 1 (M1) ½ pitch (nm)	54	45	38	32	27	24	21	19	17	15	13
MPU gate in resist (nm)	47	41	35	31	28	25	22	20	18	16	14
MPU physical gate length (nm) *	29	27	24	22	20	18	17	15	14	13	12
Gate CD control (3 sigma) (nm) [B] **	3.0	2.8	2.5	2.3	2.1	1.9	1.7	1.6	1.5	1.3	1.2
Contact in resist (nm)	66	56	47	39	33	29	26	23	21	19	17
Contact after etch (nm)	60	51	43	36	30	27	24	21	19	17	15
Overlay [A] (3 sigma) (nm)	13	11	9.5	8.0	6.7	6.0	5.3	4.7	4.2	3.8	3.3
k1 193 / 1.35NA	0.37	0.31	0.26	0.22	0.19	0.17	0.15	0.13	0.12	0.11	0.09
k1 EUVL		0.83	0.70	0.59	0.50	0.44	0.39	0.49	0.44	0.39	0.35

Potential Solutions

ITRS 2009

	First Year of IC Production	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021
	DRAM ½ pitch (nm) (contacted)	*52*	*45*	*40*	*36*	*32*	*28*	*25*	*23*	*20*	*18*	*16*	*14*	*13*
	Flash ½ Pitch (nm) (un-contacted Poly)(f)		32	28	25	23	20	18	16	14	13	11	10	8.9
45	193 nm immersion with water													
32	193 nm Immersion Double Pattern	Narrow Options												
	EUV (DRAM / MPU)													
22	EUV													
	193 nm Immersion Double / Multiple Pattern													
	ML2													
	Imprint													
16	EUV													
	Innovative 193nm immersion Multiple Pattern													
	ML2													
	Imprint													
	Directed Self Assembly													
	Interference Lithography													
11	EUV													
	ML2													
	Imprint													
	Directed Self Assembly													
	Interference Lithography													

MPU / DRAM time line

Narrow Options

Narrow Options

Narrow Options

Narrow Options

Flash Time Line

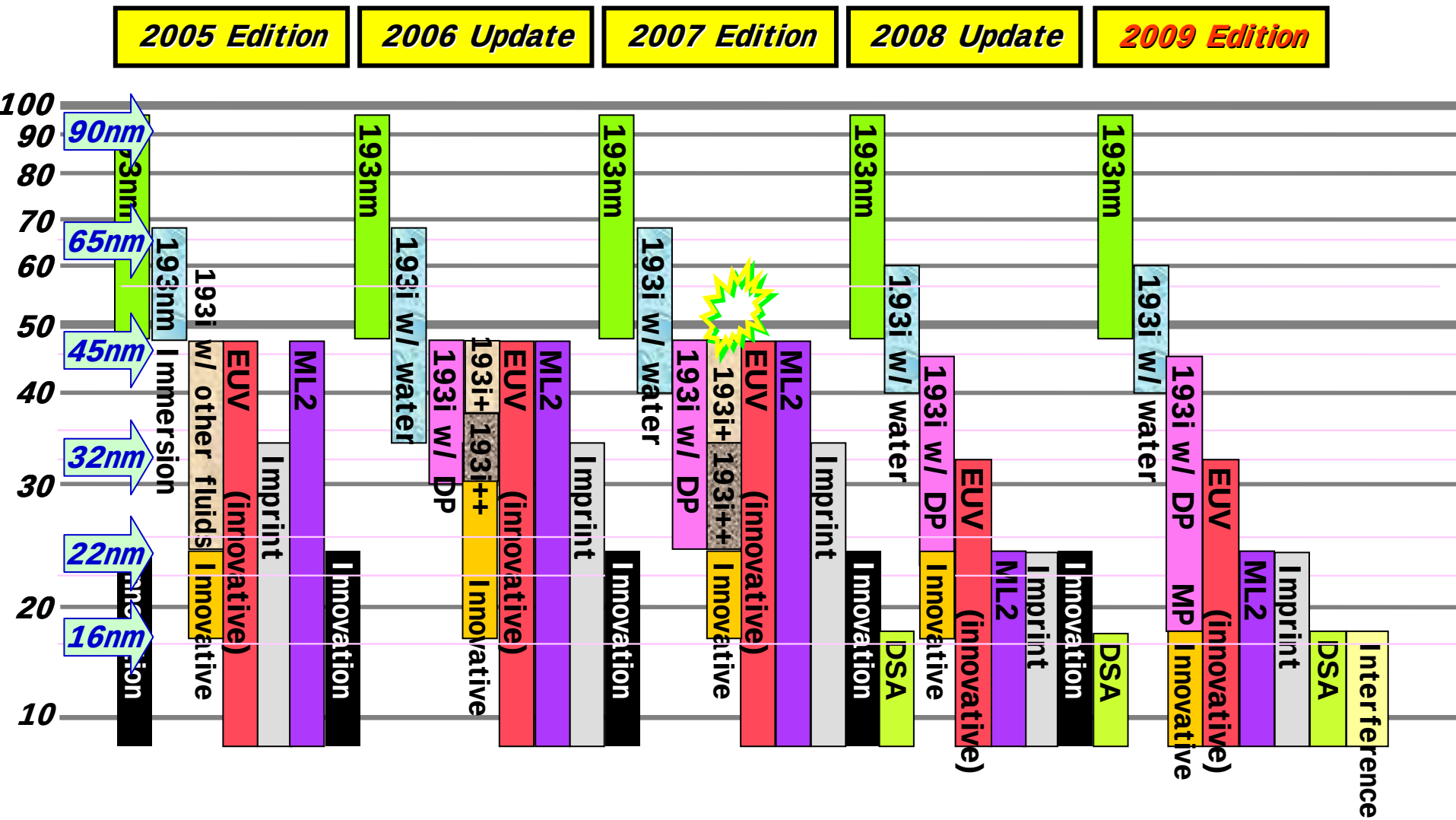
45nm: 193液浸

32nm: 193液浸DP
EUV(DRAM/MPU)

22nm: EUV, 193液浸DP/MP
ML2, Imprint

No proven optical solution below this line

Potential Solutionsの変遷



Difficult Challenges > 22 nm

ITRS 2009

Difficult Challenges > 22 nm	Summary of Issues
Optical masks with features for resolution enhancement and post-optical mask fabrication	Equipment infrastructure (writers, inspection, metrology, cleaning, repair) for assist features
	Registration, CD, and defect control for masks
	Eliminating formation of progressive defects and haze during exposure
	Understanding and achieving the specific signature and specifications for a Double Patterned mask
	Establishing a stable process so that signatures can be corrected.
Double patterning	Overlay of multiple exposures including mask image placement, mask-to-mask defined by two separate exposures
	Availability of software to split the pattern, apply OPC, and verify the quality of the split while preserving critical features and maintaining no more than two exposures for arbitrary designs
	Availability of high productivity scanner, track, and process to maintain low cost-of-ownership
	Photoresists with independent exposure of multiple passes
	Fab logistics and process control to enable low cycle time impact that efficient scheduling of multiple exposure passes.
Cost control and return on investment	Achieving constant/improved ratio of exposure related tool cost to throughput over time
	ROI for small volume products
	Resources for developing multiple technologies at the same time
	Cost-effective resolution enhanced optical masks and post-optical masks, and reducing data volume
	450 mm diameter wafer infrastructure
Process control	New and improved alignment and overlay control methods independent of technology option to <5 overlay error
	Controlling LER, CD changes induced by metrology, and defects < 10 nm in size
	Greater accuracy of resist simulation models
	Accuracy of OPC and OPC verification, especially in presence of polarization effects
	Lithography friendly design and design for manufacturing (DFM)

超解像光マスク 光以降のマスク製造

- 補助パターン付きマスク対応設備インフラ整備
- 位置精度、寸法精度、欠陥制御
- レチクルHAZE対応
- ダブルパターン対応の特殊パターンやスペック
- プロセス安定化

ダブルパターニング

- 多重露光対応のマスク間マッチング含む重ね・寸法精度、パターン分割/OPC/検証ソフトウェア開発
- 低CoOのための高生産性スキャナ/トラック/プロセス開発
- 多重露光対応レジスト開発
- 多重露光対応・短サイクルタイムの搬送・プロセス制御

コスト/ROI

- 露光ツールの生産性改善
- 少量生産品におけるROI確保
- 複数技術の同時開発のリソース確保
- 低コストRETマスク開発とデータ量の低減
- 450mmウェハ対応

プロセス制御

- 3σ<5.7nmのためのアライメント・重ね合わせ技術開発
- LER制御、測定起因CD誤差制御、10nm以下欠陥制御
- レジストシミュレーション高精度化、OPC/検証精度確保、
  リソ・フレンドリィ・デザイン、DFM

Difficult Challenges ≤ 22 nm

ITRS 2009

Difficult Challenges <= 22 nm	*Summary of Issues*
EUV lithography	Source power > 180 W at intermediate focus, acceptable utility requirements through increased conversio
	efficiency and sufficient lifetime of collector optics and source components
	Cost control and return on investment
	Resist with < 1.5 nm 3s LWR, < 10 mJ/cm2 sensitivity and < 20 nm ½ pitch resolution
	Fabrication of Zero Printing Defect Mask Blanks
	Establishing the EUVL mask Blank infrastructure (Substrate defect inspection, actinic blank inspection)
	Establishing the EUVL patterned mask infrastructure (Actinic mask inspection, EUV AIMs)
	Controlling optics contamination to achieve > five-year lifetime
	Protection of EUV masks from defects without pellicles
	Fabrication of optics with < 0.10 nm rms figure error and < 7% intrinsic flare
Resist materials	Limits of chemically amplified resist sensitivity for < 22 nm half pitch due to acid diffusion len
	Materials with improved dimensional and LWR control add (limits)
	Resist and antireflection coating materials composed of alternatives to PFAS compounds
	Low defects in resist materials (size < 10nm)
	Line width roughness < 1.4nm 3 sigma
Mask fabrication	Timeliness and capability of equipment infrastructure (writers, inspection, metrology, cleaning, repair)
	Mask process control methods and yield enhancement
	Cost control and return on investment
Cost control and return on investment	Achieving constant/improved ratio of exposure-related tool cost to throughput
	Development of cost-effective post-optical masks
	Cost effective 450mm lithography systems
	Achieving ROI for small volume products
Difficult Challenges > 22 nm	*Summary of Issues*
193 nm Immersion Multiple Patterning	Cost control and return on investment
	Wafer processing to tighter overlay and CD controls
	Mask fabrication to tighter specifications

EUVリソ

- 許容できる用力での180W以上の光源
- コストコントロールとROI
- レジスト:LWR<1.5nm, 感度<20mJ/cm2, 解像度<20nm
- 無欠陥ブランクス製造
- 寿命5年以上のための光学系コンタミ制御
- ブランクス検査装置開発
- ペリクル無しマスク
- パターン検査装置開発
- 低収差･低フレア光学系製造

レジスト材料

- 22nm-hp以下での化学増幅レジスト感度
- 微細化に対応し、LWR低減可能な材料
- PFAS対応レジストおよび反射防止膜
- 欠陥低減(<10nm)レジスト材料
- LWR低減(3σ<1.4nm)

マスク製造

- 設備インフラ整備の時期と能力
- マスクプロセス制御と歩留改善
- コストとROI

コストとROI

- 露光ツールの生産性改善
- 光マスク以降の低コストマスクの開発
- 低コスト450nmリソシステムの開発
- 少量生産品におけるROI達成

193液浸多重露光

- コスト/ROI
- 厳しい重ね/CD制御を維持するプロセス処理
- 厳しいスペックのマスク製造

Difficult Challenges ≤ 22 nm (cont')

ITRS 2009

Difficult Challenges <= 22 nm	Summary of Issues
Metrology and defect inspection	Defect inspection on patterned wafers for defects < 20 nm
	Resolution and precision for critical dimension measurement down to 6 nm, including line width roughness metrology for 0.8 nm 3s
	Metrology for achieving < 2.8 nm 3s wafer overlay error
	Template inspection for 1X Imprint Patterned Masks
	Phase shifting masks for EUV
Gate CD control improvements and process control	Development of processe
	Development of new and improved alignment and overlay control methods independent of technology option to achieve < 2.8 nm 3s overlay error, especially for imprint lithography
Maskless Lithography	Wafer Throughput
	Cost control and return on investment
	Die-to-database inspection of wafer patterns written with maskless lithography
	Pattern placement - including stitching
	Controlling variability between beams in multibeam systems
Imprint Lithography	Defect-free Imprint templates at 1X dimensions
	Infrastructure for 1X technology Templates (key here is inspection!)
	Template fabrication to tighter specifications
	Protection of Imprint templates from defects without pellicles
	Mask Life time
	Throughput
	Cost control and return on investment
	Overlay
	Process control methods to compensate for systematic CD and overlay errors

メトロロジ･欠陥検査

- 20nm以下欠陥のパターン検査
- LWR3σ=0.8nm含む6nmまでの寸法測定への解像度･精度
- 3σ<2.8nmの重ね精度測定
- ナノインプリント等倍マスク検査
- EUV用位相シフトマスク開発

ゲート寸法制御改善とプロセス制御

- LWR1.4nm以下で3σ<1.5nmのゲート寸法制御技術開発
- 特にNILで3σ<2.8nmのアライメント･重ね合わせ技術開発

マスクレスリソ

- ウェハ処理能力
- コスト/ROI
- ダイtoデータベースパターン欠陥検査
- パターン位置精度
- マルチビームでのビーム変動制御

ナノインプリントリソ

- 無欠陥等倍テンプレート
- 等倍テンプレート用インフラ(キーは検査)
- 厳しいスペックの等倍テンプレート製造
- ペリクルなしテンプレートの欠陥からの保護
- マスク寿命
- 処理能力
- コスト/ROI
- 重ね精度
- 寸法･重ねの系統的誤差補正のためのプロセス制御手法

レイリーの式におけるk1ファクタ(193nm)

k_1 factor @ArF
Resolution [hp]=k_1・λ/NA

hp ➔

↓ NA

HP	120	90	85	80	75	70	65	60	55	50	45	40	36	32
0.70	0.435	0.326	0.30	0.290	0.272	0.254	0.236	0.218	0.199	0.181	0.163	0.145	0.131	0.116
0.75	0.466	0.350	0.2	311	0.291	0.272	3	0.233	0.214	0.194	0.175	0.155	0.140	0.124
0.80	0.497	0.373	0		0.311	0.290	249	0.228	0					.33
0.85	0.528	0.396	0.374		330	0.308		0.242	0					.41
0.90	0.560	0.420	0.396	0.		0.326	0.3		256	0.233	0.210	0.187	0.168	0.149
0.95	0.591	0.443	0.418	0.394		.345	0.320		.271	0.246	0.222	0.197	0.177	0.158
1.00	0.622	0.466	0.440	0.415	0.	0.363	0.337	0.31	0.285	0.259	0.233	0.207	0.187	0.166
1.05	0.653	0.490	0.462	0.435	0.408	0.381	0.354	0.326	0.299	0.272	0.245	0.218	0.196	0.174
1.10	0.684	0.513	0.484	0.456	0.427	0.399	0.370	0.342	0.313	0.285	0.256	0.228	0.205	0.182
1.15	0.715	0.536	0.506	0.477	0.447	0.417	0.387	0.358	0.328	0.298	0.268	0.238	0.215	0.191
1.20	0.746	0.560	0.528	0.497	0.466	0.435	0.404	0.373	0.342	0.311	0.280	0.249	0.224	0.199
1.25	0.777	0.583	0.551	0.518	0.486	0.453	0.421	0.389	0.356	0.324	0.291	0.259	0.233	0.207
1.30	0.808	0.606	0.573	0.539	0.505	0.472	0.438	0.404	0.370	0.337	0.303	0.269	0.242	0.216
1.35	0.839	0.630	0.595	0.560	0.525	0.490	0.455	0.420	0.385	0.350	0.315	0.280	0.252	0.224
1.40	0.870	0.653	0.617	0.580	0.544	0.508	0.472	0.435	0					282
1.45	0.902	0.676	0.639	0.601	0.563	0.526	0.488	0.451	0					0.240
1.50	0.			622	0.583	0.544	0.505	0.466	0.427	0.389	0.350	0.311	0.280	0.249
1.55	0.			642	0.602	0.562	0.522	0.482	0.442	0.402	0.361	0.321	0.289	0.257
1.60	0.995	0.746	0.705	0.663	0.622	0.580	0.539	0.497	0.456	0.415	0.373	0.332	0.298	0.265
1.65	1.026	0.769	0.727	0.684	0.641	0.598	0.556	0.513	0.470	0.427	0.385	0.342	0.308	0.274
1.70	1.057	0.793	0.749	0.705	0.661	0.617	0.573	0.528	0.484	0.440	0.396	0.352	0.317	0.282

DRAM/MPU ASIC
k1=0.40~0.32

NAND FLASH
k1=0.30~0.28

解像限界以下(<0.25)
➔ダブルパターニング

Smaller k_1

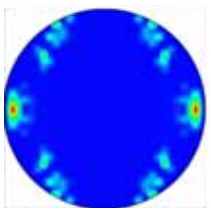
高屈折液浸

Computational lithography

OPC & optimization

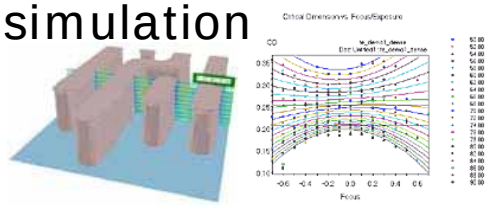
OPC
Resist modeling
Mask 3D
SRAF
Verification

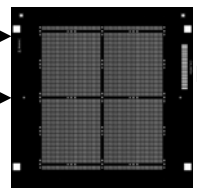
SMO
(Source Mask Optimization)



Pixelated source & SRAF

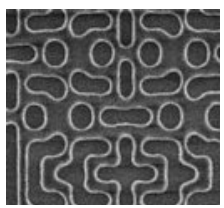
Lithography process simulation





Mask

Scanner

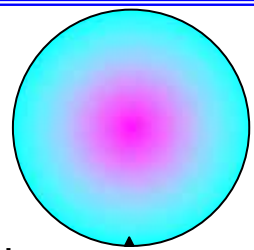


Analysis & evaluation

Feed back

Process control

CDU

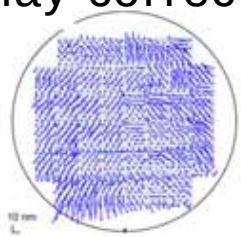


Exp. dose correction
PEB temp. zone control

Scanner knobs optimization
for CDU and OPE matching

Exp. dose | Focus | Pupil | Flare | Aberration | Laser BW

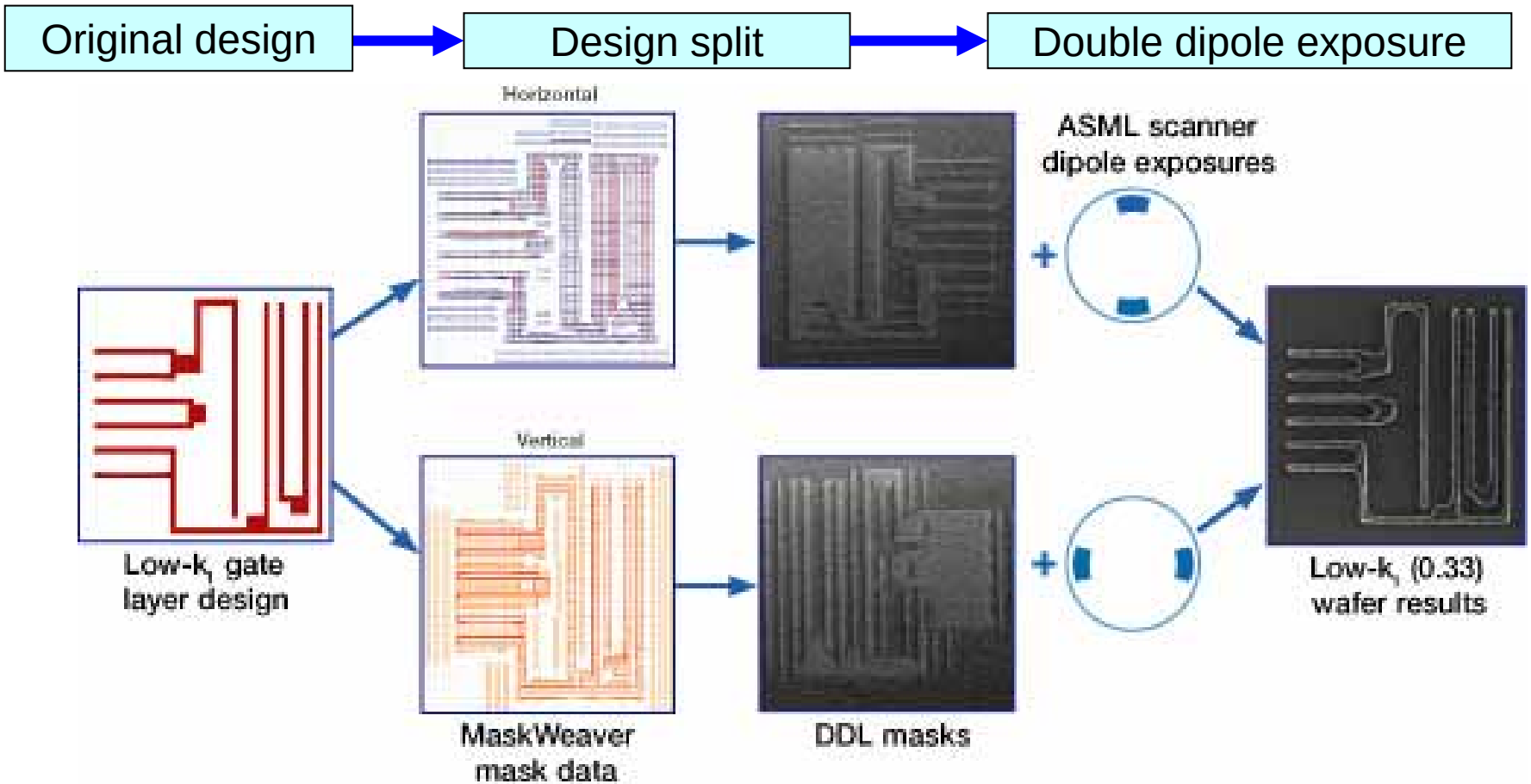
Overlay correction



High order correction

http://www.brion.com/smo_summary.asp
http://www.kla-tencor.co.jp/product/product_s/PROLITH.html

ダブルパターニング[k1>0.25]; Double dipole



ダブルパターニング[k1<0.25]

ITRS 2009

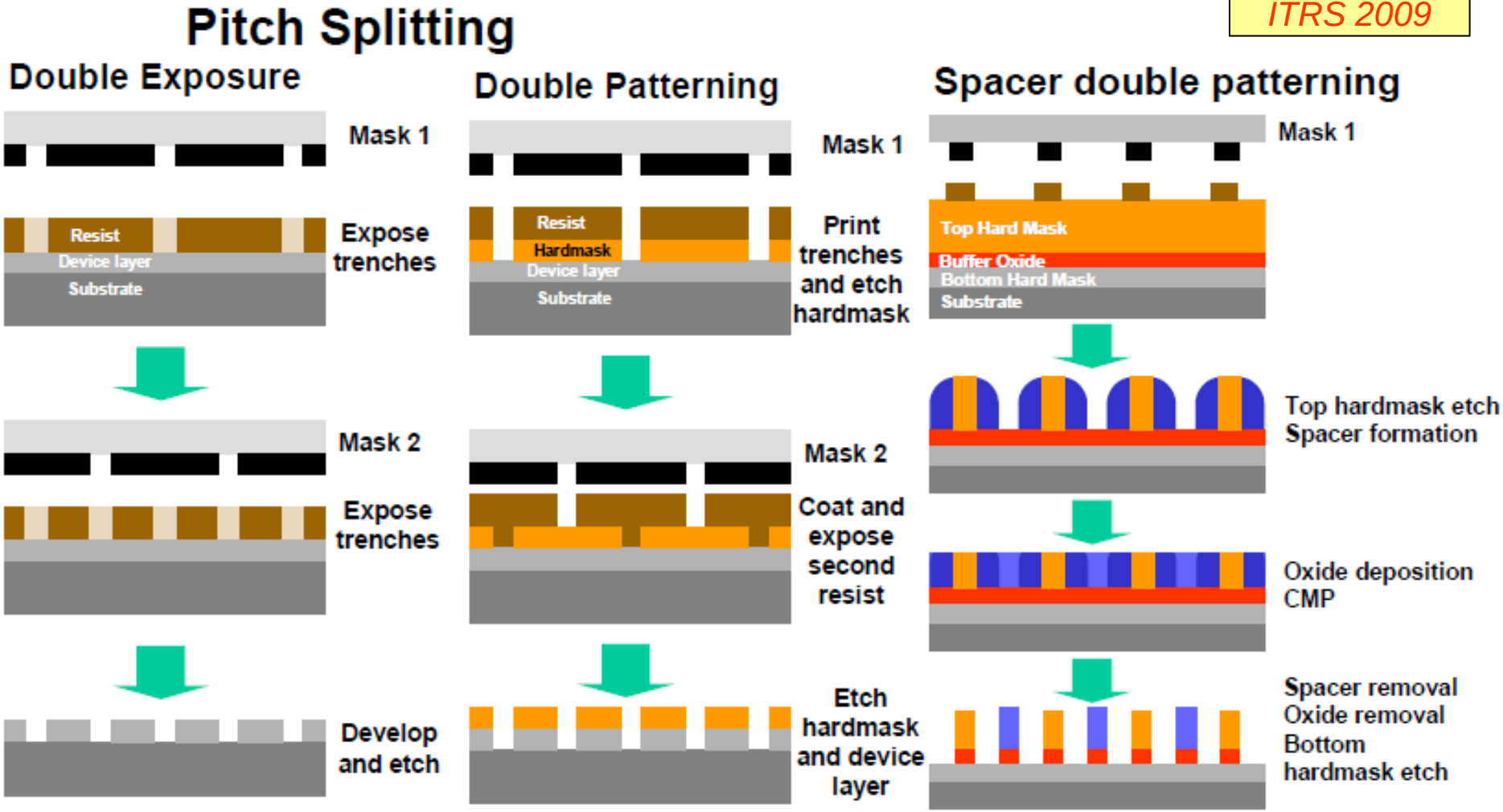


Figure LITH1 Process Flows for Pitch Splitting (DE, DP), and Spacer Patterning

Double Patterning / Spacer Requirements

ITRS 2009

Year of Production	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019
DRAM/ MPU/ ASIC (M1) ½ pitch (nm) (contacted)	52	45	40	36	32	28	25	23	20	18	16
DRAM CD control (3 sigma) (nm)	5.4	4.7	4.2	3.7	3.3	2.9	2.6	2.3	2.1	1.9	1.7
Flash ½ pitch (nm) (un-contacted poly)	38	32	28	25	23	20	18	16	14	13	11
MPU/ASIC Metal 1 (M1) ½ Pitch (nm)(contacted)	54	45	38	32							
MPU gate in resist (nm)	47	41	35	31							
MPU physical gate length (nm)	29	27	24	22							
Gate CD control (etched) (3 sigma) (nm)	3.0	2.8	2.5	2.3	2.1	1.9	1.7	1.6	1.5	1.3	1.2
Overlay (3 sigma) (nm)	10	9.0	8.0	7.1	6.4	5.7	5.1	4.5	4.0	3.6	3.2
Contact in resist (nm)	66	56	47	39	33	29	26	23	21	19	17
Generic Pitch Splitting - Double Patterning Requirements Driven by MPU metal 1/2 Pitch											
Mean CD Difference in DP Lines	0.9	0.8	0.6	0.5	0.5	0.4	0.4	0.3	0.3	0.3	0.2
Pooled Dual Line CD control (3 sigma) (nm)	3.3	3.0	2.7	2.4	2.2	2.0	1.8	1.7	1.5	1.4	1.3
Max. mean overlay for MPU LFLE or LELE	0.8	0.7	0.6	0.5	0.4	0.4	0.3	0.3	0.3	0.2	0.2
Overlay 3s for MPU LFLE or LELE	5.5	4.6	3.8	3.1	2.6	2.3	2.0	1.8	1.5	1.4	1.2
Printed Dependent Space CD control for MPU LFLE-LELE (nm,3s)	6.4	5.4	4.5	3.8	3.2	2.9	2.5	2.3	2.0	1.8	1.6
Generic Spacer Patterning Requirements - Driven By Flash											
Nominal printed duty cycle	1:3	1:3	1:3	1:3	1:3	1:3	1:3	1:3	1:3	1:3	1:3
Core Gap (Line) CD Control (3 sigma) (nm)	3.0	2.5	2.3	2.0	1.8	1.6	1.4	1.3	1.1	1.0	0.9
Line - Deposited Sidewall Thickness uniformity (3 sigma) (nm)	1.9	1.6	1.4	1.3	1.1	1.0	0.9	0.8	0.7	0.6	0.6
Space Uniformity (Bi-Modal) 3 sigma	4.5	3.8	3.4	3.0	2.7	2.4	2.1	1.9	1.7	1.5	1.4
Mean CD Differce causing Bi-modal Spacce CD	0.69	0.58	0.52	0.46	0.41	0.37	0.33	0.29	0.26	0.23	0.21
Overlay for spacer process	11.9	10.0	8.9	8.0	7.1	6.3	5.6	5.0	4.5	4.0	3.5
Generic Mask Requirements											
Mask magnification [B]	4	4	4	4	4	4	4	4	4	4	4
Mask nominal image size (nm) [C]	186	162	141	126	112	100	89	79	71	63	56
Mask minimum primary feature size [D]	130	114	99	88	78	70	62	55	49	44	39
Mask sub-resolution feature size (nm) opaque [E]	93	81	71	63	56	50	44	40	35	31	28
Image placement (nm, multipoint) [F]	6.2	5.4	4.8	4.3	3.8	3.4	3.0	2.7	2.4	2.1	1.9
CD mean to target (nm) [M]	4.1	3.6	3.2	2.9	2.5	2.3	2.0	1.8	1.6	1.4	1.3
Pitch Spliting - Double Patterning Specific Mask Rquirements											
Image placement (nm, multipoint) for double patterning of dependent layers [V]	4.4	3.8	3.4	3.0	2.7	2.4	2.1	1.9	1.7	1.5	1.4
Difference in CD Mean-to-target for two masks used as a double patterning set (nm) [W]	2.1	1.8	1.6	1.4	1.3	1.1	1.0	0.9	0.8	0.7	0.6

シングル露光の重ね精度

ピッチスプリットDP
重ね精度要求厳しい

スペーサーDP
重ね精度要求緩い

通常光マスクへの要求

ピッチスプリット
DPマスクへの要求
位置・CD精度厳しい

リソグラフィ技術の現状：光リソグラフィの延命と課題

ITRS 2009

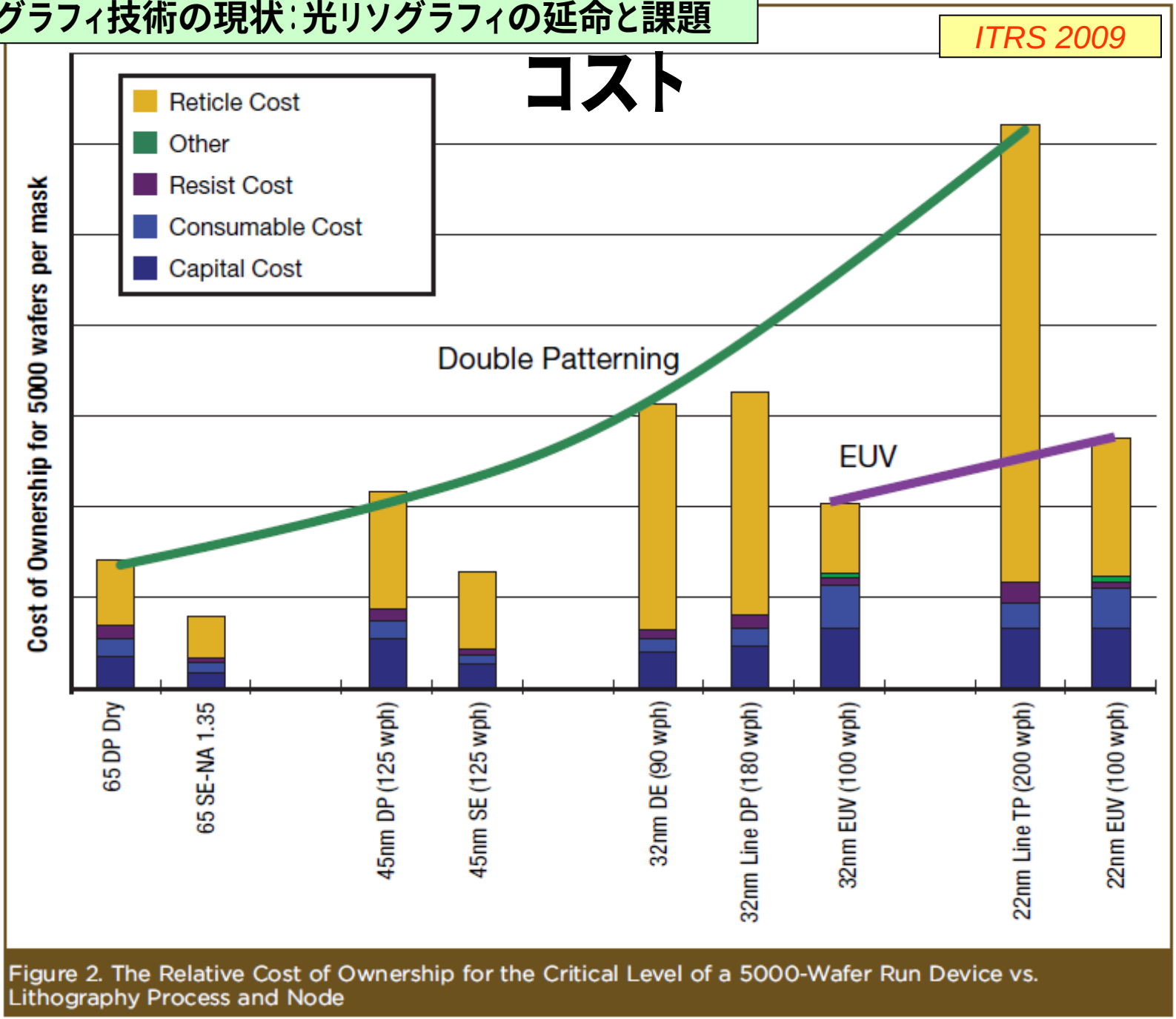


Figure 2. The Relative Cost of Ownership for the Critical Level of a 5000-Wafer Run Device vs. Lithography Process and Node

NGLの現状

ITRS 2009

EUV Lithography	Maskless Lithography	Imprint Lithography
Source Power > 180 W at Intermediate Focus With HVM Reliability Lifetime of Collector Optics and Source Components	**E-Beam Patterning System** Throughput CD – Stitching Errors Cross Talk Between Beams Wafer Heating During Write Pattern Overlay System Calibrations	**Mask** 1X Mask Pattern Inspection and Repair 1X Specifications 1X Mask Writing Time (Cost) 1X Defect-Free Process Mask Life
Resist LWR – < 1.5nm 3s Dose – < 10 mJ/cm² Resolution < 20nm 1/2 Pitch	**Resist** LWR – < 1.5nm 3s Dose - Adequate for Throughput Resolution < 20nm 1/2 Pitch	**Resist** Viscosity – Throughput
Masks Multilayer Defect Densities < 0.003/cm² Actinic Blank Inspection – Phase Defects Substrate Inspection – Phase Defect Source EUV Aerial Image Metrology (AIMs) – Defect Review EUV Actinic Pattern Inspection Defect-Free Reticle Handling	**Image Verification** Patterning Repeating Error – Defect Checking	**Imprinting System** Throughput Defects Overlay

Needs Invention to Reach Manufacturing Numbers

Needs 3X Improvement or More

Needs Less Than 3X Improvement

EUV Focus Areas 2005-2009: 22 nm half-pitch insertion target

SEMATECH

2005 / 32hp	2006 / 32hp	2007 / 22hp	2008 / 22hp	2009 / 22hp
1. Resist resolution, sensitivity & LER met simultaneously	1. Reliable high power source & collector module	1. Reliable high power source & collector module	1. Long-term source operation with 100 W at IF and 5MJ/day	1. Mask yield & defect inspection/review infrastructure
2. Collector lifetime	2. Resist resolution, sensitivity & LER met simultaneously	2. Resist resolution, sensitivity & LER met simultaneously	2. Defect free masks through lifecycle & inspection/review infrastructure	2. Long-term reliable source operation with 200 W at IF
3. Availability of defect free mask	3. Availability of defect free mask	3. Availability of defect free mask	3. Resist resolution, sensitivity & LER met simultaneously	3. Resist resolution, sensitivity & LER met simultaneously
4. Source power	4. Reticle protection during storage, handling and use	4. Reticle protection during storage, handling and use	• Reticle protection during storage, handling and use	• EUVL manufacturing integration
• Reticle protection during storage, handling and use	5. Projection and illuminator optics quality & lifetime	5. Projection and illuminator optics quality & lifetime	• Projection / illuminator optics and mask lifetime	
• Projection and illuminator optics quality & lifetime				

SEMATECH EUVL Symposium 2009

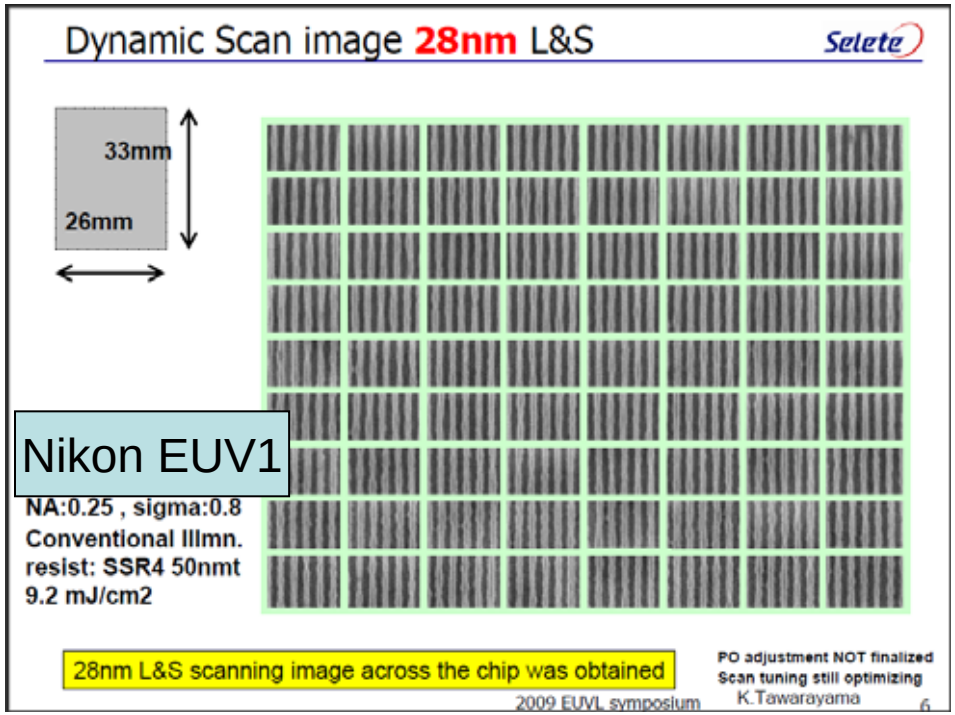
EUVL pilot line insertion in 2011/12 and HVM introduction in 2013

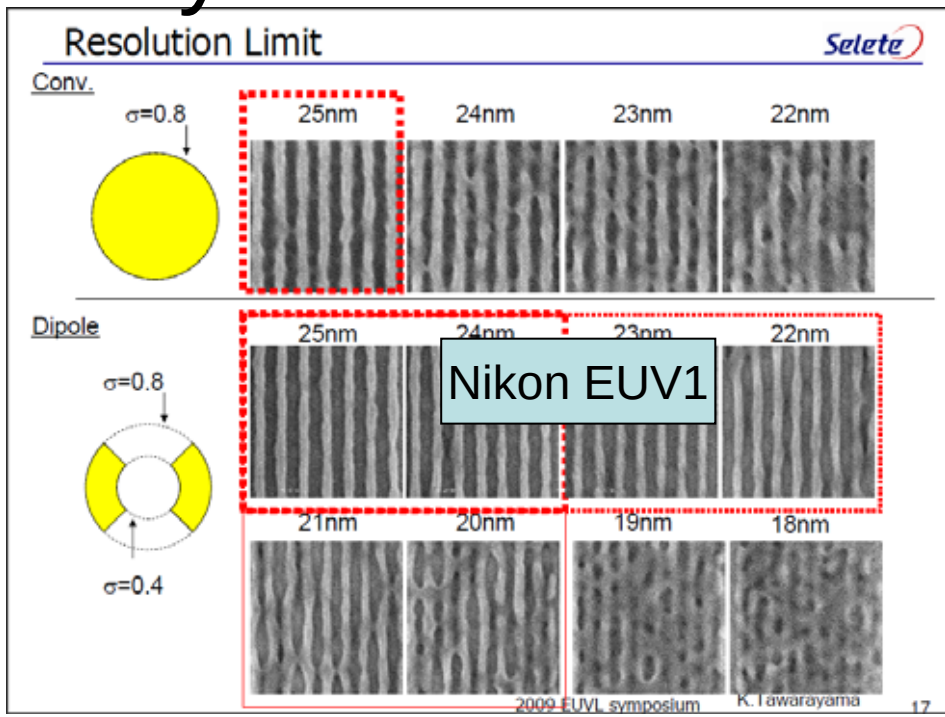
EUV status ~ マスク関係インフラ整備

- EUVL用マスク検査装置
  - マスクブランクス欠陥検査装置(Actinic inspection)
    - Seleteで開発中
  - パターン欠陥検査装置
    - DUV光/EBを用いた検査装置開発中
  - EUV-AIMS (Aerial Image Measurement System)
    [EUV転写像測定装置]
    - Carl Zeissが開発検討中

- EMI (EUV Mask Infrastructure)プログラム [SEMATECH]
  により加速(6社)

EUV status ~ system



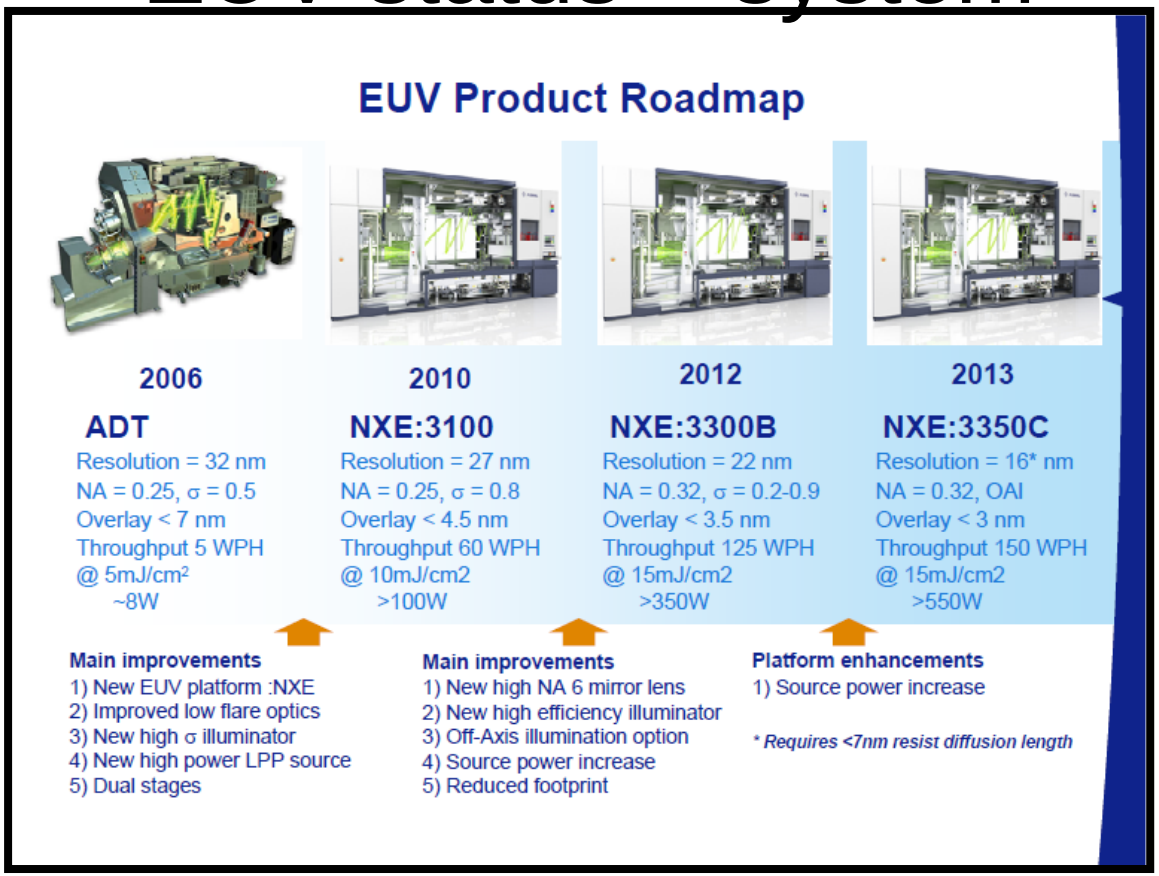


K. Tawarayama, et. al. (Selete), International Symposium on Extreme Ultraviolet Lithography, O_ET-05, 2009

先週開催のSPIE Advanced Lithography 2010

[Selete]：　ハーフ・ピッチ35nmのDD配線工程(M1/V1/M2)へEUVL (Nikon EUV1)を適用、電気特性確認

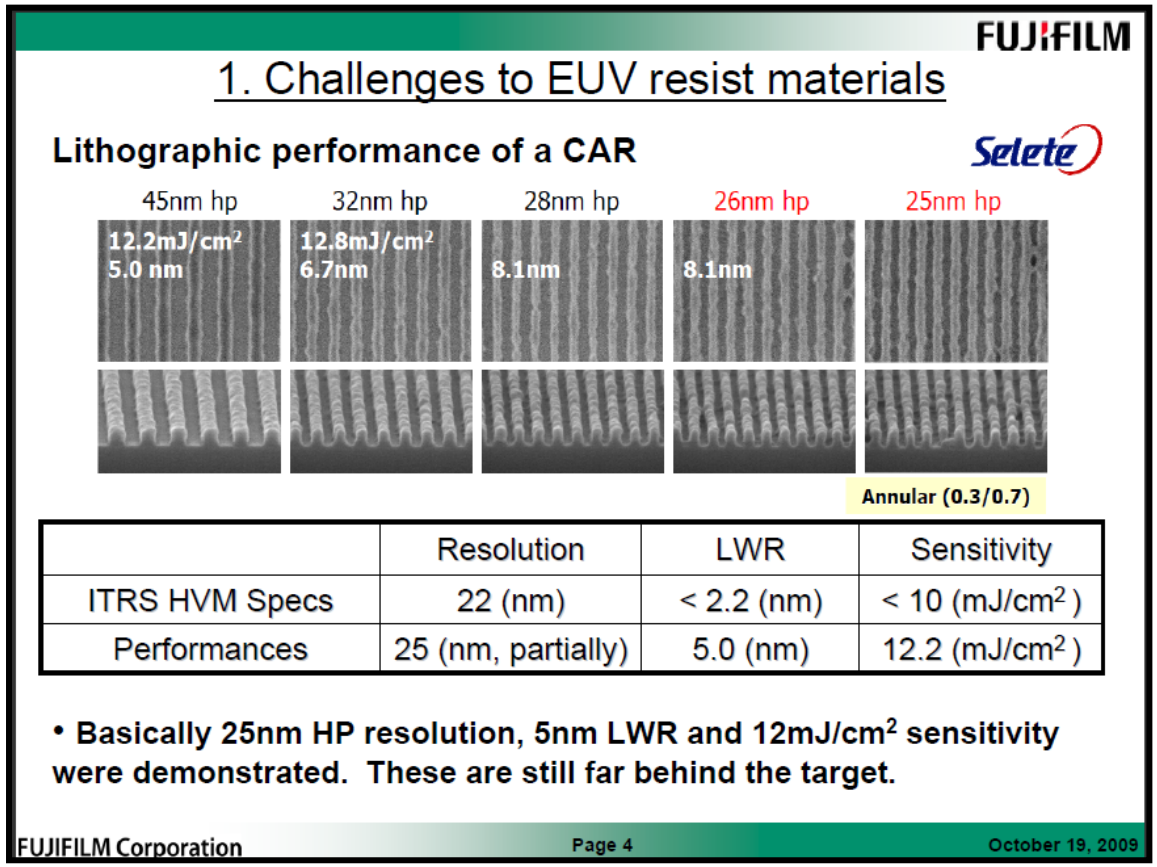
EUV status ~ system



J. Benschop (ASML), International Symposium on Extreme Ultraviolet Lithography, Keynote 1, 2009

先週開催のSPIE Advanced Lithography 2010
[ASML]　：ASMLのNXE:3100は6台受注、光源はLPPを搭載
　　15WPH(20W)➔60WPH(100W)へ改善予定
[Nikon]　：Nikonの量産対応は2014年以降16nmから

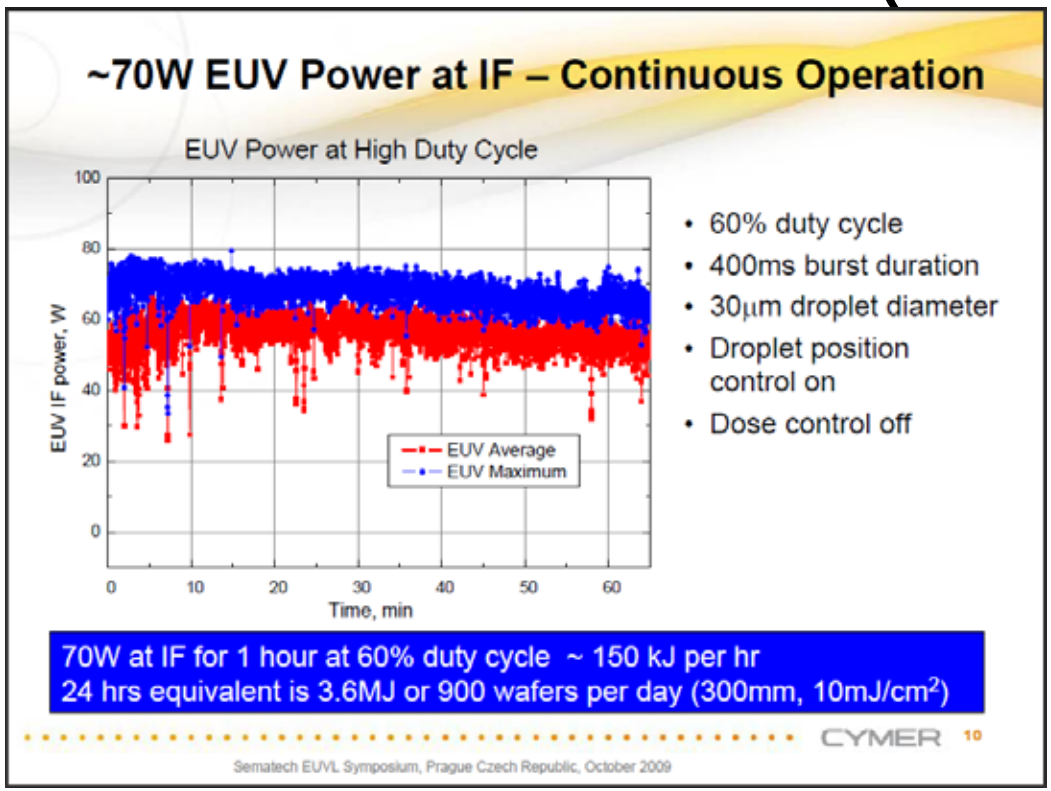
EUV status ~ resist



S. Tarutani, et. al. (Fujifilm), International Symposium on Extreme Ultraviolet Lithography, O_R1-01, 2009

先週開催のSPIE Advanced Lithography 2010
材料(樹脂、酸発生剤)やプロセス最適化(下層膜、リンス処理、現像)で改善
[Intel]： 解像度: HP=22nm, LWR=4.3nm, 10.9mJ/cm^2

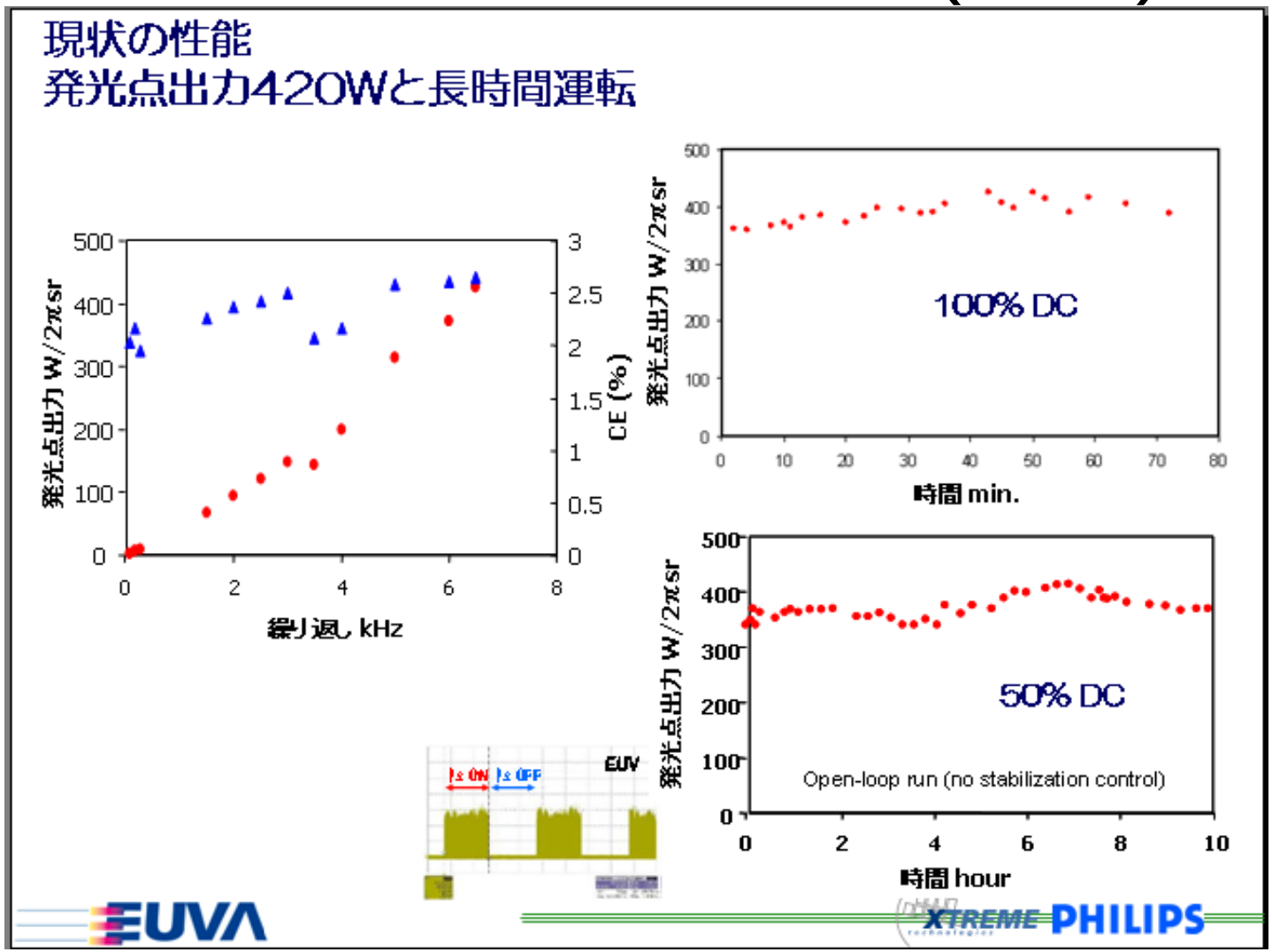
EUV status ~ source (LPP)



D. Brandt, et. al. (Cymer), International Symposium on Extreme Ultraviolet Lithography, O_SCI-03, 2009

先週開催のSPIE Advanced Lithography 2010
LPP光源は少しずつ改善が進む
[Cymer] ：LPP光源は90W@IF/DC80％へ向上、IFパワーは露光量制御とフィルタにより1/2に➔さらなるパワーアップ必要
[Gigaphoton] ：LPPで70W@IF/DC20％＝14W サイマーを追従

EUV status ~ source (DPP)



データ提供：EUVA

➔34W@IF相当

2010年度の活動方針

- ITRS 2010 update/ITRS 2011**改訂に向けた取り組み**
  - **各テーブルの見直し**
  - NGL**進捗確認**
    - EUV**光源パワー**、EUV**マスクインフラ整備**、EUV**レジスト開発**

    ➔光リソからEUVへの移行時期見極め
    コスト、マスク寿命、1工程のマスク数等
    - ML2、Imprint**開発の進捗**

- **新たな取り組みへの対応を議論**
  - **アプリケーション毎のリソグラフィ検討**
    - **少量生産品向け技術、大量生産品向け技術、ファンダリ用技術等**
  - **欠陥許容レベルの検証**
    - **デバイスタイプ毎(メモリ、ロジック等)**
  - Computational Lithography
  - Interference Lithography

まとめ

- 2010年のリソグラフィ技術
  - 45 nm hpのDRAM/MPU　➔193nm液浸シングル露光
  - 32 nm hpのFlash　➔ダブルパターニング (Spacer)
- 2013年のリソグラフィ技術
  - 32 nm hpのDRAM/MPU
  - 22 nm hpのFlash　➔両者ダブルパターニング または EUV
- ダブルパターニングは非常に複雑なパラメータ制御が要求される。特にマスクの複雑性が困難。
- EUVリソにおいては、マスクインフラ整備が最大の課題。ただし、光源やレジストも未だ課題。
- LWRと寸法制御は依然として大きな課題である。
- 依然として16nm以降のリソグラフィ技術は不透明である。