「リソグラフィの最新状況」

WG5 (リソグラフィWG)
ルネサスエレクトロニクス（株） 内山　貴之

－内容－

- WG5(リソグラフィWG)の活動体制
- ITRS 2011リソグラフィの概要
- リソグラフィの最新状況
- まとめ

略語

NA	Numerical Aperture
CD	Critical Dimension
CDU	CD Uniformity
DOF	Depth of Focus
LER	Line Edge Roughness
LWR	Line Width Roughness
RET	Resolution Enhancement Techniques
OAI	Off-Axis Illumination
PSM	Phase Shifting Mask
cPSM	complementary PSM
APSM	Alternating PSM
EPSM	Embedded PSM
Att. PSM	Attenuated PSM
EDA	Electronic Design Automation
OPC	Optical Proximity Corrections
RBOPC	Rule Base OPC
MBOPC	Model Base OPC
DFM	Design for Manufacturing Design for Manufacturability
SB	Scattering Bar
SRAF	Sub Resolution Assist Feature™
MEEF	Mask Error Enhancement Factor (=MEF)

ARC	Anti-Reflection Coating
BARC	Bottom ARC
TARC	Top ARC
AMC	Airborne Molecular Contamination
DE	Double Exposure
DP/MP	Double Patterning / Multiple Patterning
SADP	Self Aligned DP
ESD	Electro Static Discharge
NGL	Next Generation Lithography
PXL	Proximity X-ray Lithography
EPL	Electron Projection Lithography
EBDW	Electron Beam Direct Writer
IPL	Ion Projection Lithography
EUVL	Extreme Ultraviolet Lithography
ML2	Maskless Lithography
NIL	NanoImprint Lithography
UV-NIL	Ultraviolet NIL
SFIL	Step & Flash Imprint Lithography
DSA	Directed Self Assembly
LPP	Laser Produced Plasma
DPP	Discharged Produces Plasma

WG5(リソグラフィWG)の活動体制

■JEITA半導体部会/関連会社	内山 貴之/ リーダー (ルネサス エレクトロニクス)
	千々松 達夫/ サブリーダー (富士通セミコンダクター)
	笹子 勝(パナソニック)
	東川 巌 (東芝)
	川平 博一(ソニー)
	和田 恵治 (ローム)
	田中 秀仁 (シャープ)
	山口 敦子➔山本 治朗(日立製作所)
■コンソーシアム	須賀 治 (EIDEC)
■特別委員(SEAJ他)	奥村 正彦/ 国際委員 (SEAJ:　ニコン)
	高橋 和弘 (SEAJ:　キヤノン)
	中島 英男 (SEAJ:　東京エレクトロン)
	山口 哲男 (SEAJ:　ニューフレアテクノロジー)
	笠間 邦彦(SEAJ:　ウシオ電機)
	大久保 靖 (HOYA)
	林 直也 (大日本印刷)
	森本 博明（凸版印刷）
	大森　克実(東京応化工業)
	栗原 啓志郎 (アライアンスコア)

計　19名

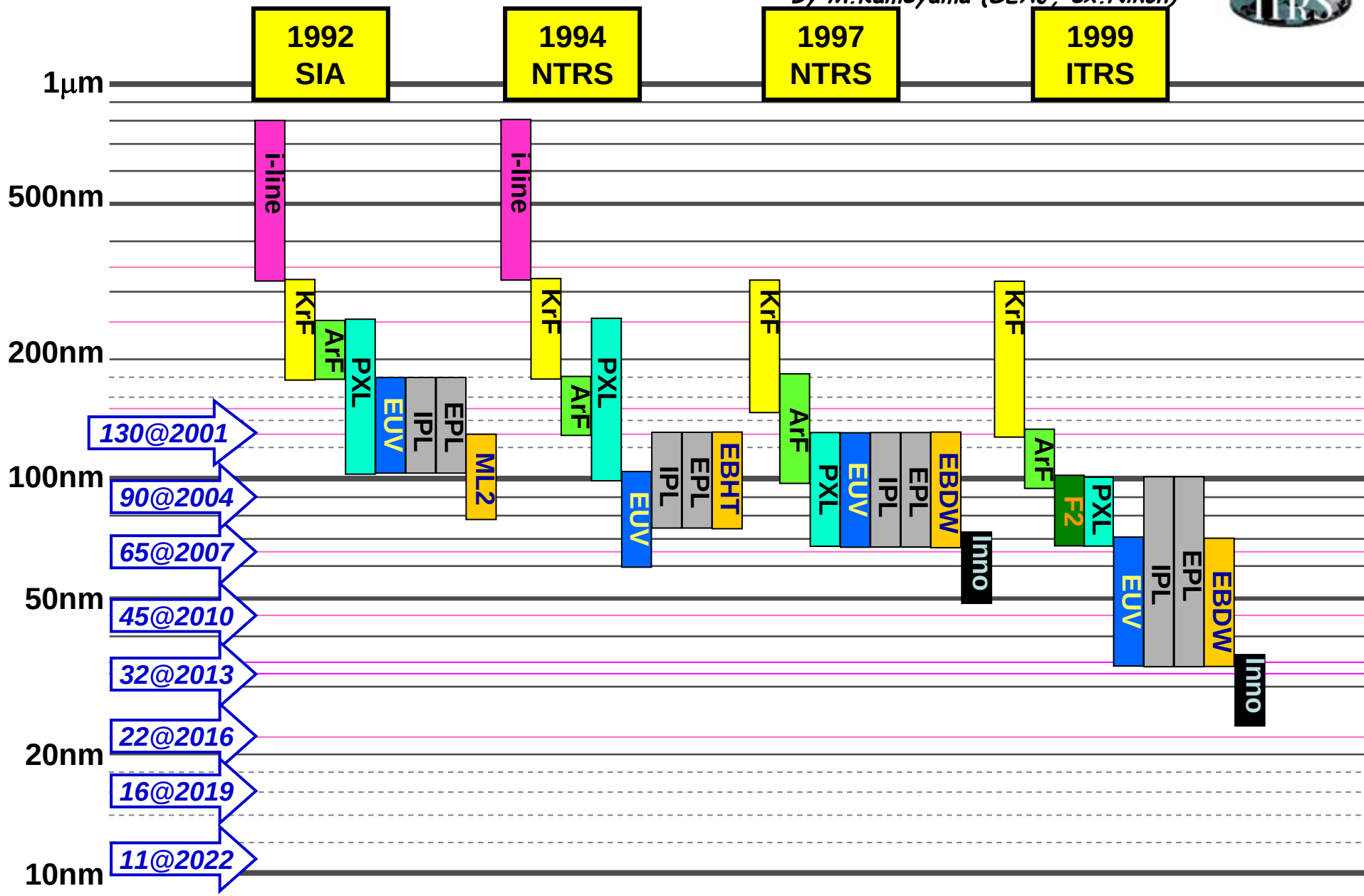
ITRS 2011 リソグラフィの概要

- Potential Solutionsの変遷
- Potential Solutions 見直し
- Difficult Challenge 見直し
- Table見直し
- 項目・カラーリング見直し

  等

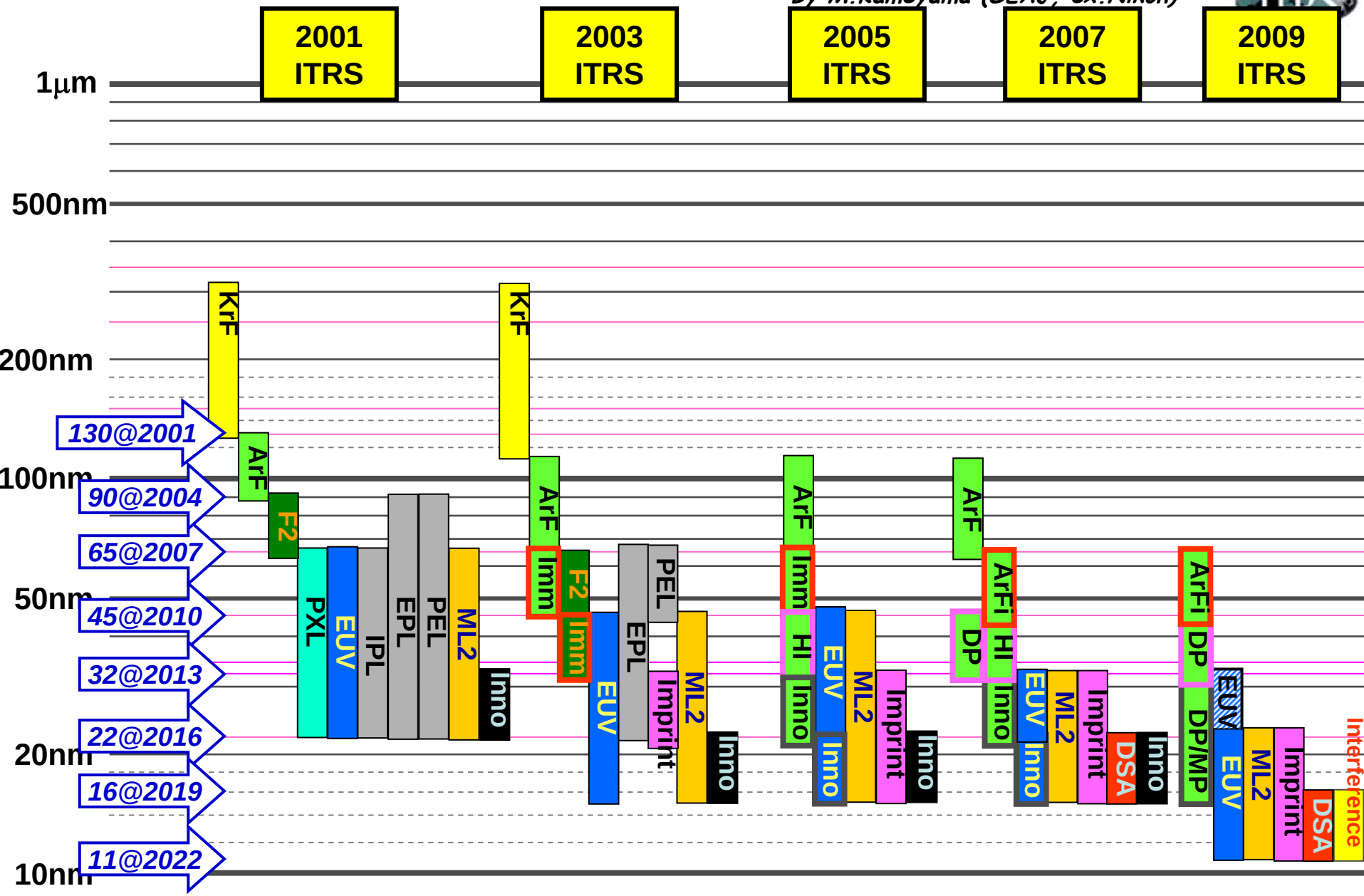
Lithography Potential Solutionsの変遷(1)

By M.Kameyama (SEAJ, ex.Nikon)



Lithography Potential Solutionsの変遷(2)

By M.Kameyama (SEAJ, ex.Nikon)



Lithography Potential Solutionsの変遷(3)

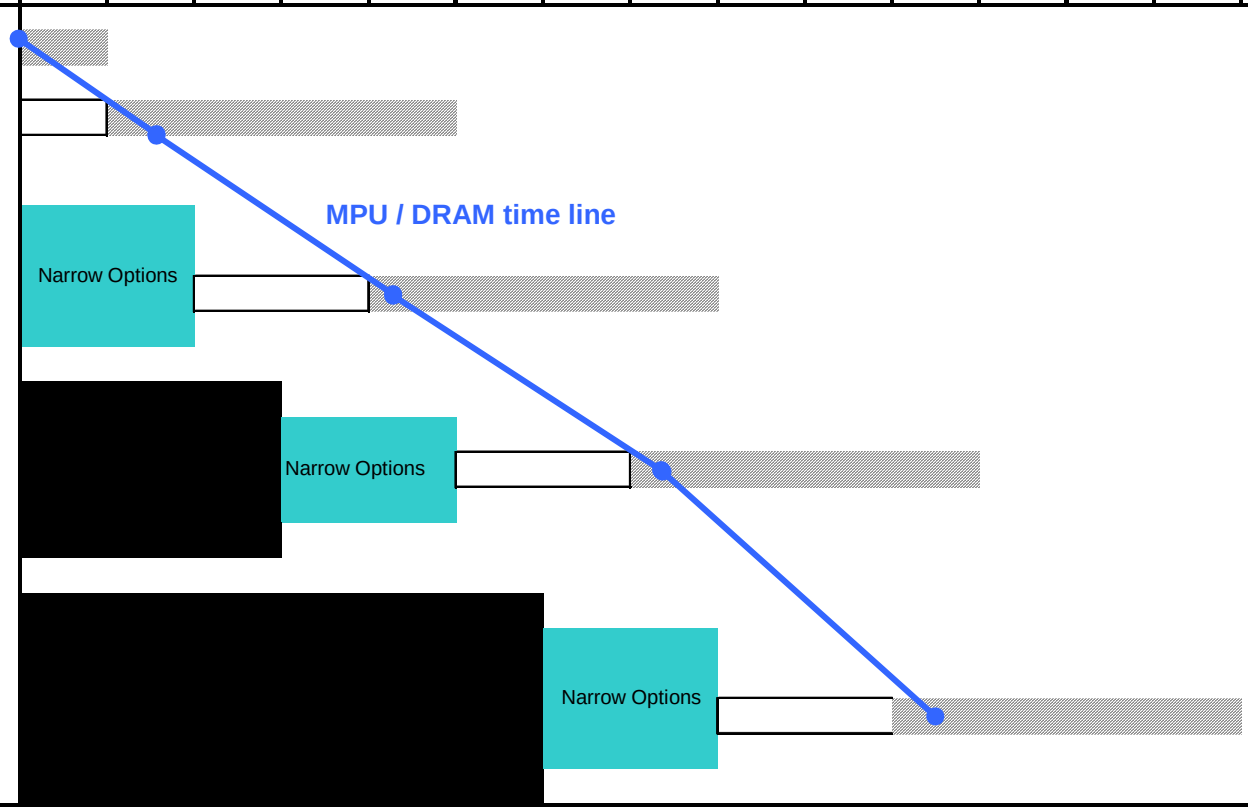
	ArF	F2	ArF i	ArF HI	DP	MP	PXL	EUV	IPL	EPL	NIL	ML2	DSA
1992	250						250	180	180	180		130	
1994	180						250	100	130	130		130	
1997	130						130	130	130	130		130	
1999	130	100					100	70	100	100		70	
2001	110	90					65	65	65	90		65	
2003	110	65	65				X	45	X	65	32	45	
2005	90	X	65	45				45		X	32	45	
2007			65	32	45			32			32	32	22
2009			45	X	32	22		32			22	22	16
2011													

ITRS 2011 "Potential Solutions (MPU/DRAM)"

ITRS 2011

Figure LITH3A DRAM and MPU Potential Solutions

	First Year of IC Production	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026
	DRAM ½ pitch (nm) (contacted)	36	32	28	25	23	20.0	17.9	15.9	14.2	12.6	11.3	10.0	8.9	8.0	7.1	6.3
	MPU/ASIC Metal 1 1/2 pitch (nm)	38	32	27	24	21	18.9	16.9	15.0	13.4	11.9	10.6	9.5	8.4	7.5	7.5	7.5
45	193nm Imm																
32	193 nm DP																
22	EUV 193nm MP ML2 (MPU) Imprint (DRAM)																
16	EUV 193nm MP ML2 Imprint DSA + litho platform																
11	EUV / EUV + MP EUV (6.Xnm) ML2 Imprint Litho + DSA Innovation																



This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.

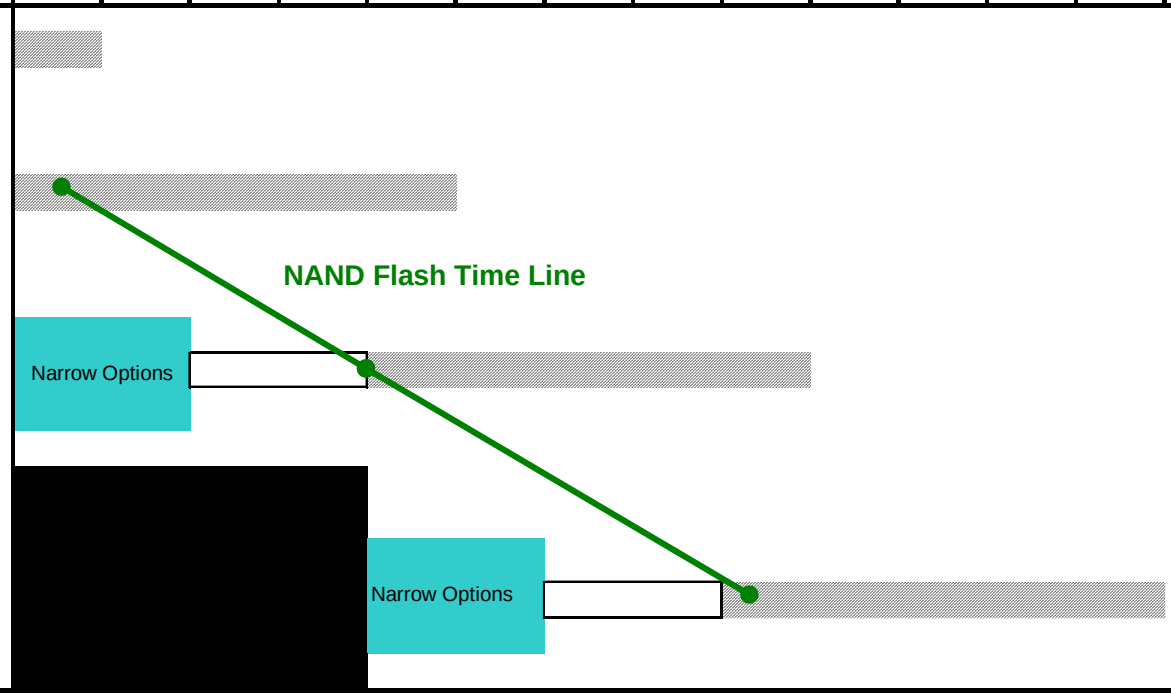
Research Required
Development Underway
Qualification / Pre-Production
Continuous Improvement

ITRS 2011 "Potential Solutions (NAND Flash)"

ITRS 2011

Figure LITH3B Flash Potential Solutions

	First Year of IC Production	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026
	Flash ½ Pitch (nm) (un-contacted Poly)(f)	22	20	18	17	15	14.2	13.0	11.9	10.9	10.0	8.9	8.0	8.0	8.0	8.0	8.0
32	193 nm DP																
22	193 nm DP																
16	193nm MP EUV Imprint																
11	EUV + MP 193nm MP EUV (6.xnm) Imprint EUV + DSA Innovation																



This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.

Research Required
Development Underway
Qualification / Pre-Production
Continuous Improvement

ITRS Lithography Potential Solutions比較

hp(nm	NAND Flash	MPU /DRAM	ITRS2010 update		ITRS2011	
			NAND Flash	MPU/DRAM	NAND Flash	MPU/DRAM
32	2009	2012	193 nm-i DP	193 nm-i DP EUV (DRAM)	193 nm-i DP	193 nm-i DP
22	2011	2015	193 nm-i DP	EUV 193 nm-i DP/MP ML2 (MPU) Imprint (DRAM)	193 nm-i DP	EUV 193 nm-i MP ML2 (MPU) Imprint (DRAM)
16	2014	2018	193nm-i MP EUV Imprint 193nm-i + DSA	EUV 193nm-i MP ML2 Imprint 193nm-i + DSA	193nm-i MP EUV Imprint	EUV 193nm-i MP ML2 (MPU) Imprint (DRAM) DSA+ litho platfo
11	2019	2021	EUV 193nm-i MP Imprint EUV + DSA Innovative patte	EUV ML2 Imprint Litho + DSA Innovative patte	EUV + MP 193nm-i MP EUV (6.X nm) Imprint EUV + DSA Innovation	EUV / EUV + MP EUV (6.X nm) ML2 Imprint Litho + DSA Innovation

Lithography Potential Solutionsの変遷(4)

	ArF	F2	ArF i	ArF HI	DP	MP	PXL	EUV	IPL	EPL	NIL	ML2	DSA	6.Xnm
1992	250						250	180	180	180		130		
1994	180						250	100	130	130		130		
1997	130						130	130	130	130		130		
1999	130	100					100	70	100	100		70		
2001	110	90					65	65	65	90		65		
2003	110	65	65				X	45	X	65	32	45		
2005	90	X	65	45				45		X	32	45		
2007			65	32	45			32			32	32	22	
2009			45	X	32	22		32			22	22	16	
2011			45		22	22		22			22	22	16	11

2011年版リソグラフィの主な変更点

- 光によるシングル露光は40nmまで。2011年以降の32nm/22nm向けのリソグラフィはダブル・マルチパターーニングが主流となった。
- マルチパターーニングテーブルを拡充し、スペーサーダブルパターーニングを明確にした。
- MEEFやk1ファクタといったリソグラフィパラメータの見直しを行った。
- EUVマスク吸収膜厚等の新仕様を追加した。

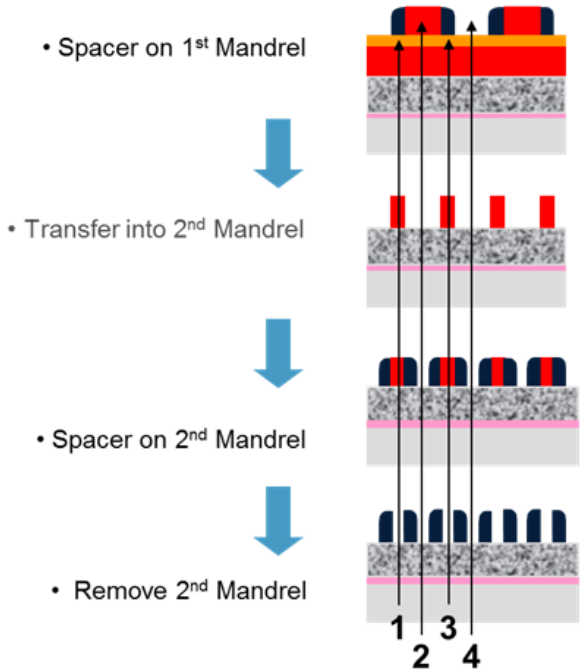
マルチパターニングテーブル見直し

Generic Spacer Patterning Requirements - Driven By Flash		
Nominal printed duty cycle	*1:3*	*1:3*
Core Gap (Line) CD Control (3 sigma) (nm)	*3.0*	
Line - Deposited Sidewall Thickness uniformity (3 sigma) (nm)	*1.9*	
Space Uniformity (Bi-Modal) 3 sigma	*4.5*	
Mean CD Differce causing Bi-modal Spacce CD		
Overlay for spacer process		
Generic Mask Requirements		
Mask magnification [B]	**4**	
Mask nominal image size (nm) [C]	186	
Mask minimum primary feature size [D]	130	
Mask sub-resolution feature size (nm) opaque [E]	93	
Image placement (nm, multipoint) [F]	6.2	
CD mean to target (nm) [M]	4.1	
Pitch Spliting - Double Patterning Specific Mask Rquirements		
Image placement (nm, multipoint) for double patterning of dependent layers [V]	4.4	
Difference in CD Mean-to-target for two masks used as a double patterning set (nm) [W]	2.1	

2011年版

Spacer Based Density Multiplication for Dense Arrays (Driven by NAND)		
Target Pitch	**43.7**	**40.1**
Multiplication Factor [E]	**2X**	**2X**
Manufacturing Process Requirement		
Mandrel Target CD [F]	**21.9**	**20.0**
Mandrel CDU (intra+interfield) [G, M]	**1.3**	**1.2**
Mandrel MTT [H, M]	**0.9**	**0.8**
Spacer CDU [G]	**0.7**	**0.6**
Spacer MTT [H]	**0.7**	**0.6**
Patterned Feature Control [N]		
Line CDU [G]	**0.7**	**0.6**
Line MTT [H]	**0.7**	**0.6**
Line MTT+3sigma [I]	**0.9**	**0.9**
Core Space CDU [G]	**1.3**	**1.2**
Core Space MTT [H]	**0.9**	**0.8**
Core Space MTT+3-sigma [I]	**1.6**	**1.4**
Gap Space CDU [G]	**1.9**	**1.7**
Gap Space MTT [H]	**1.6**	**1.4**
Gap Space MTT+3-sigma (performance limiting featrue) [I,K]	**2.4**	**2.2**
Spacer Defined Space CDU [G,J]		
Spacer Defined Space MTT [H,J]		
Spacer Defined Space MTT+CDU [I,J]		
Spacer DP Overlay Requirements [L]		
Cut/Block mask: for Line end cutting, line removal or trench blocking at minimum pitch [L]	**7.5**	**6.9**

QPT

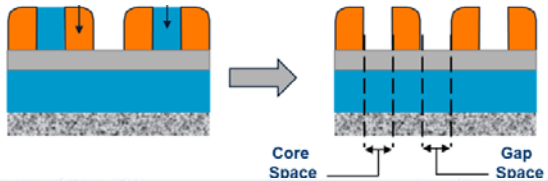


Quad Patterning: 3-data pools for spaces:

"Spacer Defined Space"
- Space #1 & Space #3 originate from the first spacer deposition, and share a single mean & distribution.
- This is a new data pool compared to spacer double patterning.

"Core Space"
- Space #2 in this diagram; originates from first mandrel, which is therefor a lithography derived feature.
- In quad patterning the second spacer deposition contributes additional CD-error, compared to the spacer double patterning core space.

"Gap Space"
- Space #4 in this diagram; originates from first lithographically generated space, which is therefore a lithography derived feature.
- In quad patterning, both the first and second spacer deposition contributes additional CD-error, compared to the spacer double patterning core space.



	A	B	C	D	E	F	G	H	I	J	K
1			SADP Formula's					SAQP Formula's			
2											
3		NAND 1/2 pitch	Half-Pitch	100%	22	20		Half-Pitch	100%	15	12
4											
5	Mfg. Process Capability	Mandrel CDU	=6%*C3	6.0%	1.3	1.2		=6%*H3	6.0%	0.9	0.7
6		Mandrel MTT	=4%*C3	4.0%	0.9	0.8		=4%*H3	4.0%	0.6	0.5
7		Spacer CDU	=3%*C3	3.0%	0.7	0.6		=2%*H3	2.0%	0.3	0.2
8		Spacer MTT	=3%*C3	3.0%	0.7	0.6		=2%*H3	2.0%	0.3	0.2
9											
10	Resulting Patterning Performance	Line CDU	=C7	3.0%	0.7	0.6		=H7	2.0%	0.3	0.2
11		Line MTT	=C8	3.0%	0.7	0.6		=H8	2.0%	0.3	0.2
12		Line MTT+3sigma	=SQRT(C7^2+C8^2)	4.2%	0.9	0.8		=SQRT(H7^2+H8^2)	2.8%	0.4	0.3
13		Core Space CDU	=C5	6.0%	1.3	1.2		=SQRT(H5^2+(2*H7)^2)	7.2%	1.1	0.9
14		Core Space MTT	=C6	4.0%	0.9	0.8		=SQRT(H6^2+(2*H8)^2)	5.7%	0.8	0.7
15		Core Space MTT+3-sigma	=SQRT(C5^2+C6^2)	7.2%	1.6	1.4		=SQRT(H13^2+H14^2)	9.2%	1.4	1.1
16		Gap Space CDU	=SQRT(C5^2+(2*C7)^2)	8.5%	1.9	1.7		=SQRT(H5^2+(2*H7)^2+(2*H7)^2)	8.2%	1.2	1.0
17		Gap Space MTT	=SQRT(C6^2+(2*C8)^2)	7.2%	1.6	1.4		=SQRT(H6^2+(2*H8)^2+(2*H8)^2)	6.9%	1.0	0.8
18		Gap Space MTT+3-sigma	=SQRT(C16^2+C17^2)	11.1%	2.4	2.2		=SQRT(H16^2+H17^2)	10.8%	1.6	1.3
19		Spacer Defined Space CDU						=H7	2.0%	0.3	0.2
20		Spacer Defined Space MTT						=H8	2.0%	0.3	0.2
21		Spacer Defined Space MTT+CDU						=SQRT(H7^2+H8^2)	2.8%	0.4	0.3

ITRS2012年改訂向けた取り組み(案)

- コンタクトパターン向けネガ現像プロセス(NTD)
- EUVマスクラフネスの要求仕様
- 高電圧EBレジスト感度
- DSAの扱い
- ML2テーブル見直し

リソグラフィの最新状況

ITRS 2011

LITH1_Challenges

Short and Long Term Challenges

	Near Term Challenges (2011-2018) (16nm Logic/DRAM @ HVM; Flash 11nm @ optical narrowing with 16nm in HVM)
1	Multiple patterning - cost, throughput, complexity
2	Optical mask - complexity with SRAF, long write time, cost
3	EUV source power to meet throughput requirement; Defect "free" EUV masks availability; mask infrastructure availability; EUV mask in fab handling, storage, and requalification.
4	Resist at 16nm and below that can meet sensitivity, resolution, LER requirements
5	Process control on key parameters such as overlay, CD control, LWR at 16nm HVM
6	Retooling requirements for 450mm transition

	Long Term Challenges (2019 - 2025) (11nm @HVM)
1	Higher source power, increase in NA, chief ray angle change on EUV; Mask material and thickness optimization
2	Defect free DSA processing
3	Infrastructure for 6.Xnm Lithography or multiple patterning for EUVL 13.5nm
4	Metrology tool availability to key parameters such as CDU, thickness control, overlay, defect
5	Early narrow and implement ~2 options with viable infrastructures support

ITRS International Technology Roadmap for Semiconductors

NGLの課題

- EUV
  - 光源開発 現状：30~40W ➔ 目標250W(125WPH)
  - マスクインフラ整備
  - レジスト
- NIL (Nano Imprint Lithography:ナノインプリントリソグラフィ)
  - 重ね合わせ精度 現状: 10nm ➔ 目標 <8nm
  - 欠陥密度 現状: ~10/cm^2 ➔ 目標 <0.01~0.1/cm^2
- ML2 (Maskless Lithography:マスクレスリソグラフィ)
  - スループット ➔2012年目標 1WPH ➔ 最終目標 >100WPH
- DSA (Directed Self Assembly: 誘導自己組織化)
  - LSI適用のための本格的な開発が始まった。
  - 欠陥の評価が始まった。現状~25/cm^2 ➔ 目標 0.01~0.1/cm^2
  - ロジックパターンへの適用は?

EUVリソグラフィの現状

EUV Focus Areas 2007-2011: 22 nm half-pitch insertion target

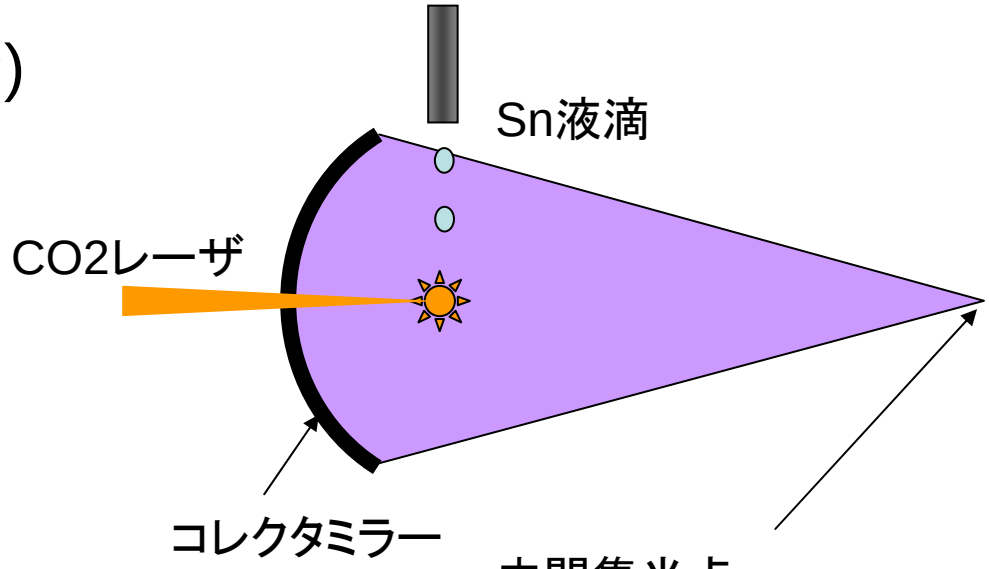
2007 / 22hp	2008 / 22hp	2009 / 22hp	2010 / 22hp	2011 / 22hp
1. Reliable high power source & collector module	1. Long-term source operation with 100 W at IF and 5MJ/day	1. Mask yield & defect inspection/review infrastructure	1. Mask yield & defect inspection/review infrastructure	1. Long-term reliable source operation with 200 W at IF*
Source:#1	Source:#1	Source:#2	Source:#1	Source:#1
2. Resist resolution, sensitivity & LER met simultaneously	2. Defect free masks through lifecycle & inspection/review infrastructure	2. Long-term reliable source operation with 200 W at IF	1. Long-term reliable source operation with 200 W at IF	2. Mask yield & defect inspection/review infrastructure
3. Availability of defect free mask	3. Resist resolution, sensitivity & LER met simultaneously	2. Resist resolution, sensitivity & LER met simultaneously	2. Resist resolution, sensitivity & LER met simultaneously	3. Resist resolution, sensitivity & LER met simultaneously
4. Reticle protection during storage, handling and use	• Reticle protection during storage, handling and use	• EUVL manufacturing integration	• EUVL manufacturing integration	• EUVL manufacturing integration
5. Projection and illuminator optics quality & lifetime	• Projection / illuminator optics and mask lifetime			

*) *This requires a 20 X improvement from current source power status*

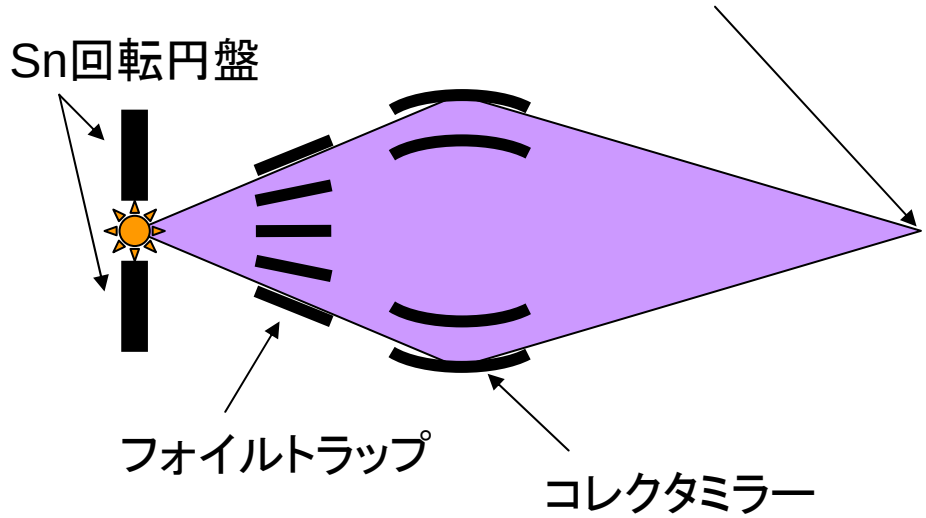
HVM introduction in late 2013 if productivity challenge can be met

#1 EUV光源：目標は今年250W@IF

- LPP(サイマー、ギガフォトン)
  - 現在の出力: ~40Wレベル
  - 熱問題は?
  - デブリ対策は?
  - コレクタミラーの寿命は?
  - ランニングコストは?



- DPP(ウシオ)
  - 現在の出力: 30Wレベル
  - 熱問題は?
  - フォイルトラップの寿命は?
  - コレクタミラーの寿命は?
  - ランニングコストは?



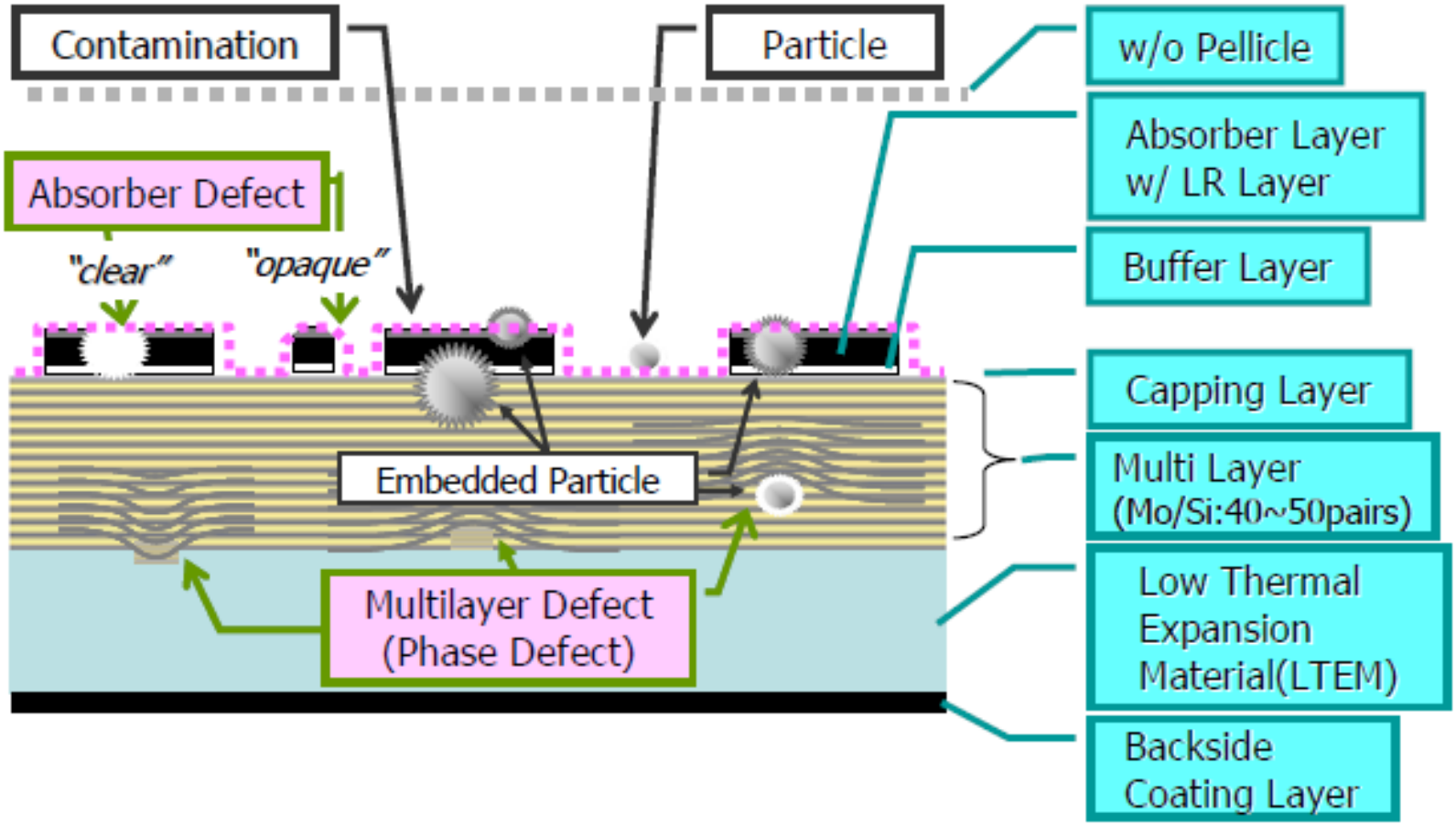
高出力光源を用いた検証

- 高速スキャンによる露光システム性能検証
  - 露光精度(寸法均一性、重ね合わせ精度)
  - スループット
  - 光源、照明光学系、投影光学系の安定性、耐久性
- マスクの耐久性 (Haze含む)
- レジストアウトガス検証
- 実データをもとにした本当のランニングコスト

#2 EUVマスクインフラ整備

- マスクブランク検査装置
  - EUV波長 (EIDEC/Lasertec)
  - DUV波長 (KLA-Tencor)
- マスクパターン検査
  - DUV波長（Nuflare、KLA-Tencor等）
  - EB (AMAT、KLA-Tencor、EIDEC/EBARA等)
  - EUV波長 (KLA-Tencor等)
- 空間像計測
  - EUV AIMS (Carl Zeiss)
- EMI program [SEMATECH]
  - ブランク検査装置 #1 ➔2013年
  - パターン欠陥検査装置 #1 ➔2016年
  - AIMS #1 ➔2014年

EUVマスクは縦方向に複雑



Takashi Kamo (MIRAI-Selete), "Printability of EUVL mask defect detected by actinic blank inspection tool and 199-nm pattern inspection tool", Proc. of SPIE Vol. 7823 78231U-1

EUVマスク

- マスク平坦度 (非テレセン) ➔重ね合わせ誤差
  - 静電チャックのコンタミ
  - マスク平坦度、マスク裏面コンタミ、マスク裏面キズ
  - マスク厚均一性

  ➔ マスク描画位置補正でOK?

- 高速レチクル交換
  - 静電チャックにおける高速レチクル交換

- ペリクル無しの無欠陥マスク
  - マスクハンドリング方法、収納方法、Pod開発・運用
  - ウェハFAB内でのマスク異物検査、マスククリーナー
  - マスク洗浄耐性

#3 EUV レジスト

- RLS トレードオフ
  - 解像度(Resolution): 20nmレベルに改善
  - ラフネス(LWR): 下層制御、プロセス制御で改善
  - 感度(Sensitivity) 10mJ/cm^{2}にあと一歩

- レジストパターン倒れ
  - 膜厚最適化
  - 新リンス技術

まとめ

- 2012年MPU/DRAMの32nm、2011年NAND Flashの22nmは193nmダブルパターニングを適用。
- 2015年のMPU/DRAMの22nmの第1候補にEUVリソグラフィ、2014-15年のNAND Flashの16nmの第1候補は193nmマルチパターニング。
- EUVリソグラフィ開発遅延のため、DP/MP導入による光リソグラフィの延命が採用されるも、コストやプロセス制御に課題。EUVリソグラフィ開発の最大の課題は光源で、実用化に向けた光源開発は今年2012年が最大の山場となる。
- ML2はスループット、NILは欠陥対策が最大の課題で、実用化に必要なレベルに届いていない。DSAでも本格的な欠陥評価が開始され、注目されてきた。また、6.X nm波長のEUVリソグラフィがNGL候補に入った。