2014年度STRJ Workshop

STRJ-WG4(配線)活動報告
微細化ブレークスルー技術とITRS2.0への展開

2015年3月6日

WG4(Interconnects)
筑根 敦弘(大陽日酸)

報告内容

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- STRJ-WG4 構成メンバー
- 2014年度活動内容概要

2. 2014年度活動内容

ITRS関連活動

- ITRS2013の発行(含む和訳)
- ITRS2.0に関する活動

STRJ独自活動(ヒアリング)

- 3D実装技術の開発動向
- 先端CMOSデバイス技術の開発動向
- バリアメタルを中心とした配線技術の開発動向
- 光配線技術の開発動向

3. 2014年度活動まとめと今後の活動予定

主な略語について

A.R.	Aspect Ratio	アスペクト比：(深さ または 高さ)/(幅 または 径)
CNT	Carbon Nano-Tube	カーボンナノチューブ
EM	Electro-migration	エレクトロマイグレーション
ILD	Inter-Layer Dielectric	層間絶縁膜
TDDB	Time-dependent Dielectric Breakdown	経時絶縁破壊
ALD	Atomic Layer Deposition	原子層成長
k (κ)	Dielectric Constant	比誘電率
Low-k	Low Dielectric Constant	低誘電率
μ	Magnetic Permeability	透磁率
PCB	Printed Circuit Board	プリント回路基板
Q	Quality Factor	Q値
RC	Resistance × Capacitance	抵抗と容量の積
tan δ	Tangent Delta	誘電正接
TSV	Through-Silicon Via	シリコン貫通ビア
ULK	Ultra Low-k	極低誘電率
3D	Three-dimensional	三次元

STRJ-WG4 2014年度構成メンバー

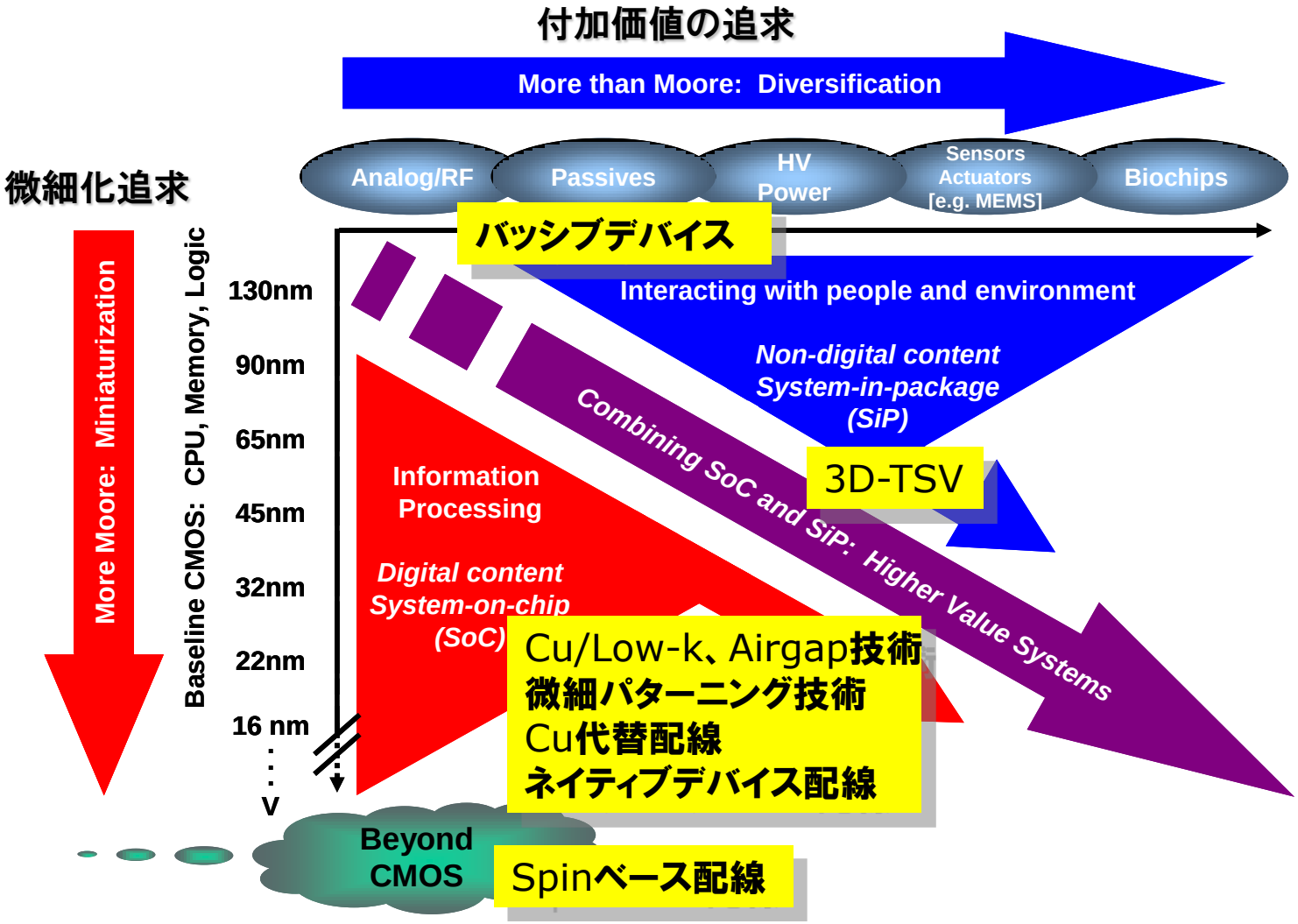
リーダー	磯林 厚伸	[東芝]
サブリーダー	筑根 敦弘	[大陽日酸]
国際対応	中村 友二	[富士通セミコンダクター]
	武田 健一	[日立製作所]
幹事	早川 崇	[SEAJ: 東京エレクトロン]
委員	松本 明	[ルネサスエレクトロニクス]
	庄子 礼二郎	[ソニー]
	柴田 英毅	[東芝]
	蔭山　聡	[ローム]
特別委員	上野 和良	[芝浦工業大学]
	嘉田 守宏	[AIST]
	伊藤 浩之	[東京工業大学]
	李 康旭	[東北大学]
	辻村 学	[荏原製作所]
	今井 正芳	[荏原製作所]
	小林 伸好	[SEAJ: 日本ASM]
	山﨑 治	[シャープ]
	古澤 健志	[日立化成]

2014年度活動内容概要

- STRJ-WG4会議を8回開催
  - 4/21, 6/13, 8/26, 9/22, 10/31, 12/11, 1/14, 2/18
- ITRS2013発行
  - 最終チェックで加筆・修正を行い、5月に正式発行。
  - 和訳作成。
- ITRS2.0活動
  - White Paper発行に向けた資料作成。
    (Focus Topics: Heterogeneous Integration, More Moore)
- 独自活動(開発動向ヒアリング)
  - 8/26　武田健一委員(日立製作所):3D実装技術
  - 8/26　若林整先生(東工大):先端CMOSデバイス技術
  - 12/11 小池淳一先生(東北大):バリアメタルを中心とした配線技術
  - 1/14　中村隆宏氏(PETRA):光配線技術

2014年度活動内容 (ITRS2013関連)

ITRS Interconnect WGの取り扱う技術



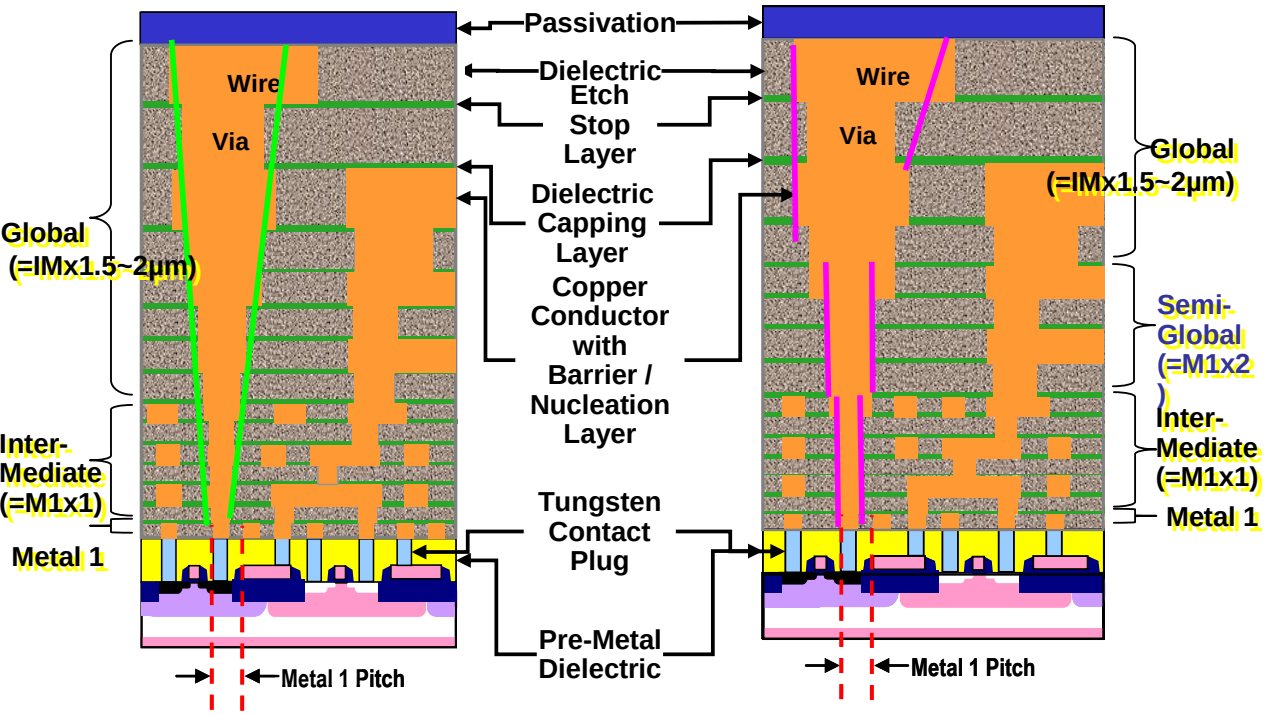
Source: http://www.itrs.net/Links/2012ITRS/2012Chapters/2012Overview.pdf

More Mooreにおける配線技術

ITRS2013関連

MPU Cross-Section

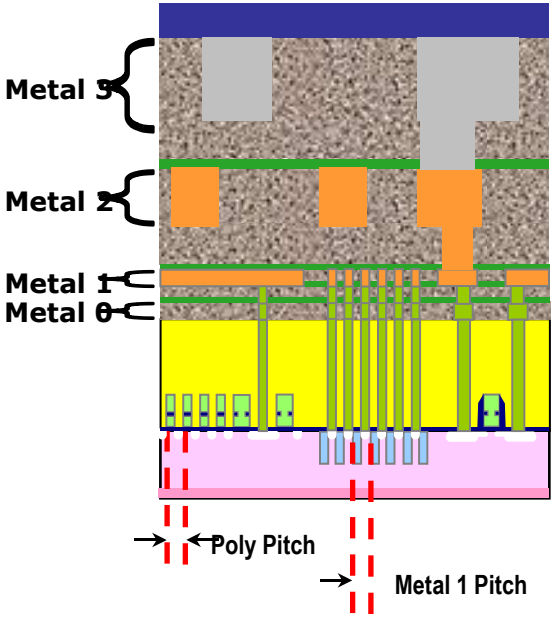
MPU: Microprocessor Unit



SoC Cross-Section

SoC: System on Chip

Flash Cross-Section

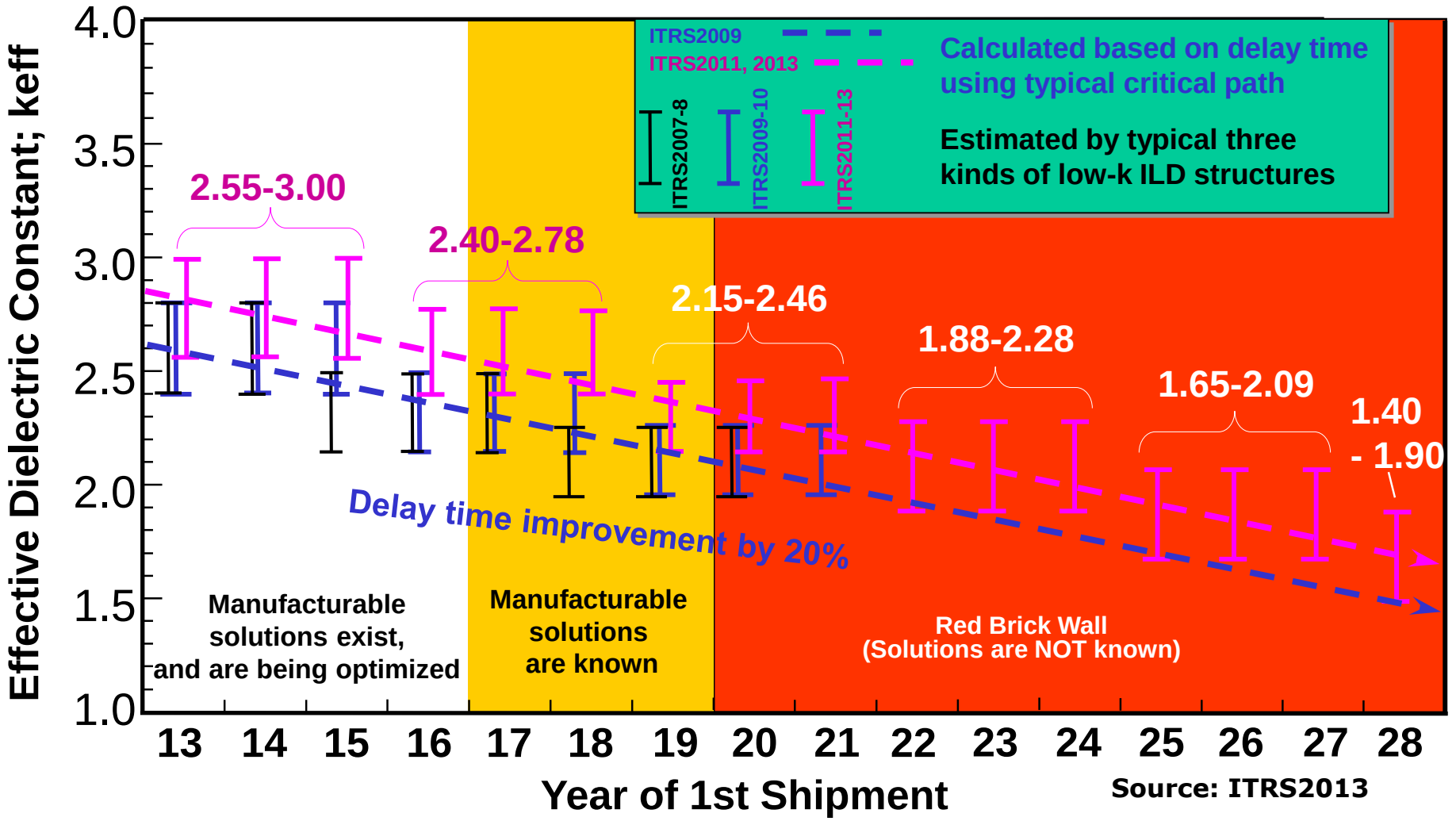


Source: ITRS2013

LogicはCu/Low-k技術、Flashは微細化技術とAirgap技術を中心にロードマップ化

Cu/Low-k技術 – Low-kロードマップ

ITRS2013関連



微細化と低誘電率化の両立の課題多く、改定毎にk_{eff}修正（増大方向）。
ロードマップではデバイス性能向上の観点で年率20%減を実現するk_{eff}方針を提示

2014年度活動内容 (ITRS2.0関連)

Collaboration Priorities
Focus Topics, Teams and Existing Expertise

		EXPERTISE TEAMS														
FOCUS TOPICS	FOCUS TEAM LEADERS	FI	M&S	A&P	MEMS	Litho	FEP	RFAMS	ESH	IC	Metrology	PIDS	YE	Design	Test	ERM	ERD
SYSTEM INTEGRATION	SYSTEM DRIVERS			2	X	X		X		2		X		X	1		X
OUTSIDE SYSTEM CONNECTIVITY	EMERGING RESEARCH MATERIALS / RFAMS		1	1	2			X	2	2	1	2		1	1	X	
HETEROGENEOUS INTEGRATION	ASSEMBLY AND PACKAGING		2	1	1			1	3	1	2	3	2	2	1	1	2
HETEROGENEOUS COMPONENTS	MEMS		X	1	X			X			X			X	2	3	
BEYOND CMOS	EMERGING RESEARCH DEVICES		X	2						2				X		1	X
MORE MOORE	PROCESS INTEGRATION, DEVICES, AND STRUCTURES		X	3		X	X		X	1	X	X		X	3	1	
MANUFACTURING	FACTORY INTEGRATION	X		3	X	X	X	X	X	3	X	X	X		2	2	

FOCUS TEAM

LEVEL 1= ABSOLUTELY NECESSARY
LEVEL 2= NEED OCCASIONAL SYNCHRONIZATION
LEVEL 3= NICE TO KNOW

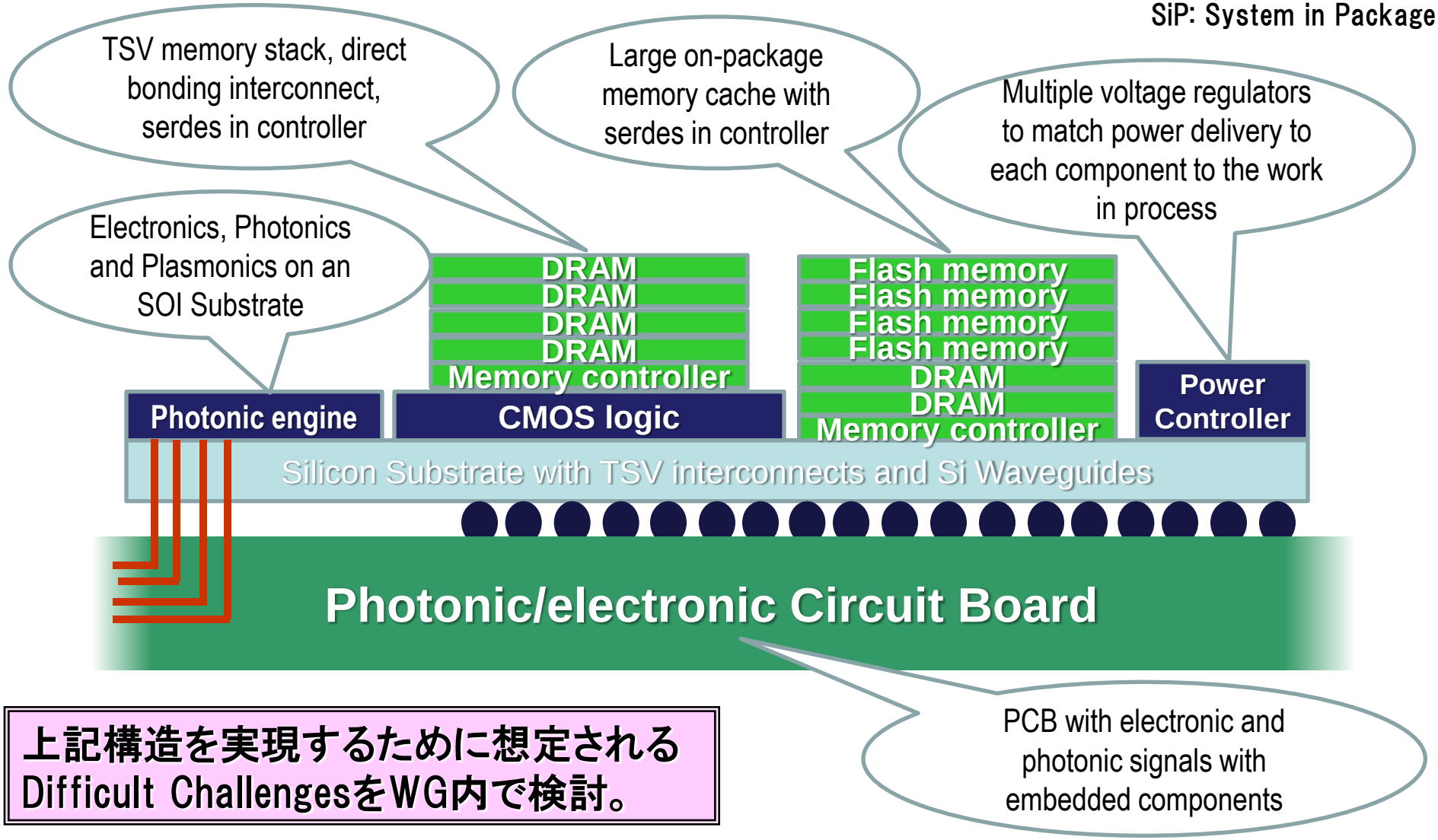
Interconnect WGとして"Heterogeneous Integration"と"More Moore"をLEVEL1に。

ITRS2.0 (Heterogeneous Integration)

ITRS2.0関連

A Potential Solution: 2.5D Photonic Co-integrated SiP

SiP: System in Package



上記構造を実現するために想定される Difficult ChallengesをWG内で検討。

ITRS2.0 (Heterogeneous Integration)

ITRS2.0関連

1. ESD (Electrostatic Discharge): Plasma damage on transistors by TSV etching especially on via last scheme. Low damage TSV etch process and the layout of protection diodes are the key factors.

2. CPI (Chip Package Interaction) Reliability [Process]: Low fracture toughness of ULK (Ultra Low-κ) dielectrics cause failures such as delamination. Material development of ULK with higher modulus and hardness are the key factors.

3. CPI (Chip Package Interaction) Reliability [Design]: A layout optimization is a key for the device using Cu/ULK structure.

4. Stress management in TSV [Via Last]: Yield and reliability in Mx layers where TSV land is a concern.

5. Stress management in TSV [Via Middle]: Stress deformation by copper extrusion in TSV and a KOZ (Keep Out Zone) in transistor layout are the issues.

6. Thermal management [Hot Spot]: Heat dissipation in TSV is an issue. An effective homogenization of hot spot heat either by material or layout optimization are the key factors.

7. Thermal management [Warpage]: Thermal expansion management of each interconnect layer is necessary in thinner Si substrate with TSV

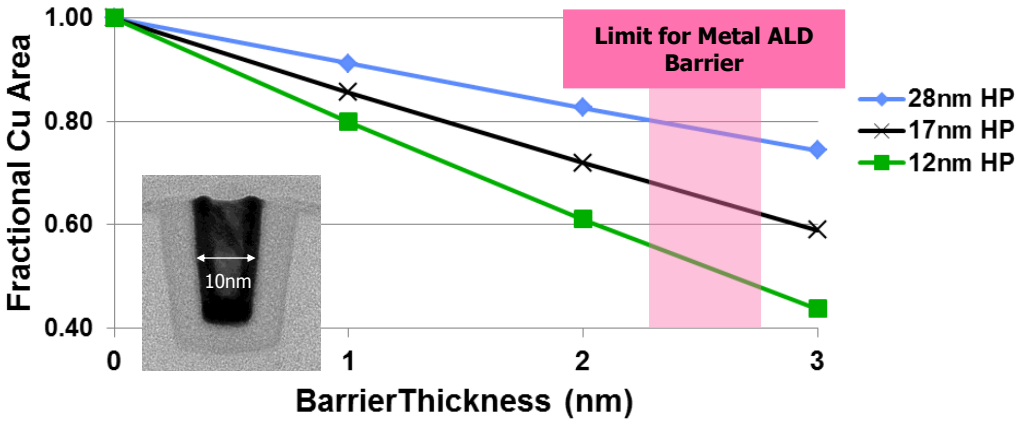
8. Passive Device Integration [Performance]: Higher Q, in other words, thicker metal lines and lower tan δ dielectrics is a key for achieving lower power and lower noise circuits.

9. Passive Device Integration [Cost]: Higher κ film and higher μ are required for higher density and lower footprint layout.

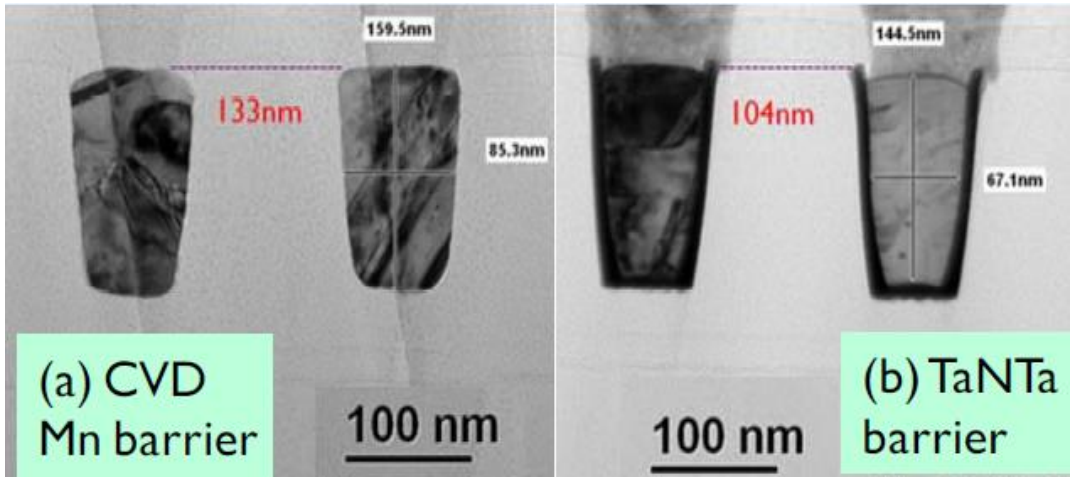
10. Implementation of Optical Interconnects: Optical interconnects for signaling, clock distribution, and I/O requires development of a number of optical components such as light sources, photo detectors, modulators, filters and waveguides. On-chip optical interconnects replacing global interconnects requires the breakthrough to overcome the cost issue.

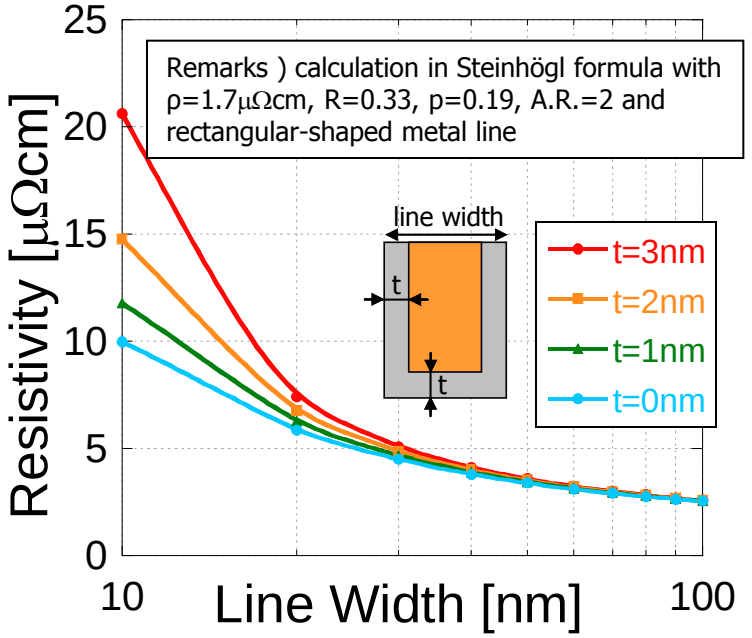
Difficult Challengesとして10項目をWhite Paper案として提出。

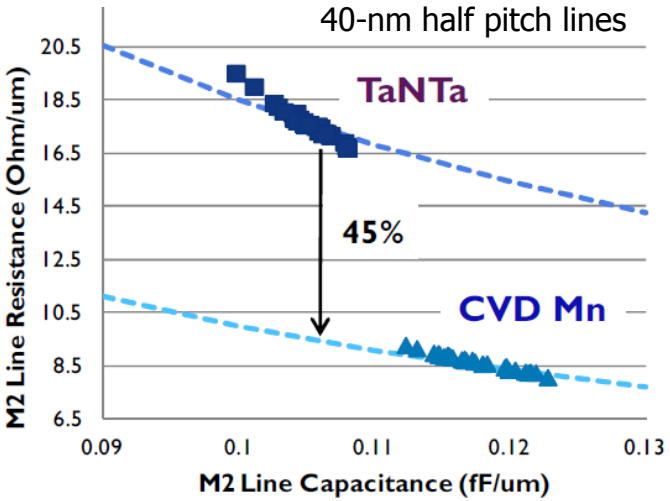
RC Reduction: Near Term



Source: James Clarke and Boyan Boyanov (Intel)







バリアメタルの薄膜化による抵抗低減。

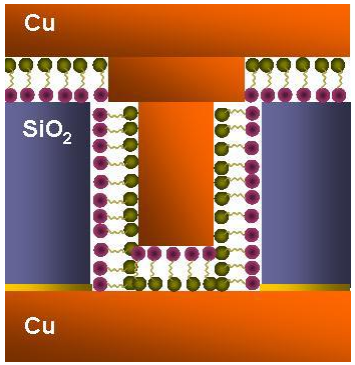
S. K. Siew et al., IITC 2013

RC Reduction: Long Term

Ultrathin Cu Barrier Layers

- SAM (Self-assembled Monolayer)

$NH_2(CH_2)_3Si(OCH_3)_3$

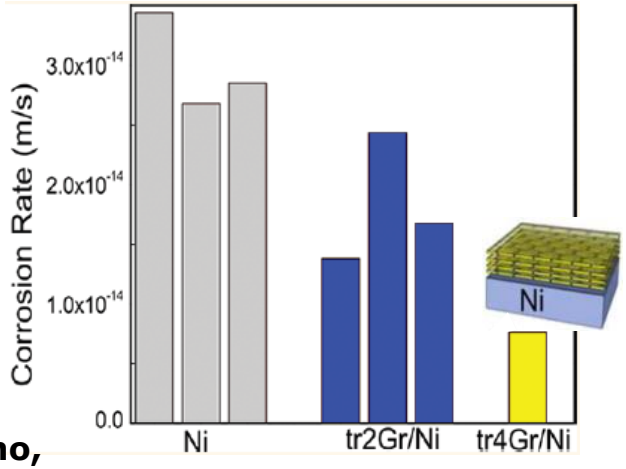


Source: Arantxa Maestre Caro (Intel), at IMEC

- Graphene barrier

Oxidation and corrosion resistance

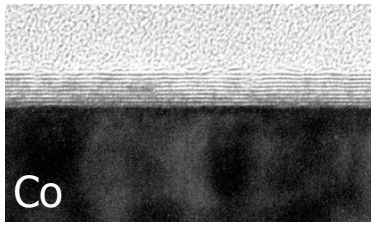
S. Chen et al., ACS Nano, 2011, 5 (2)



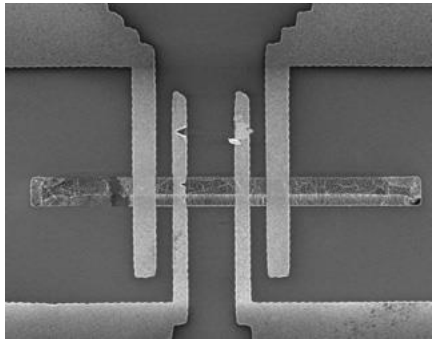
D. Prasai et al., ACS Nano, 2012, 6 (2)

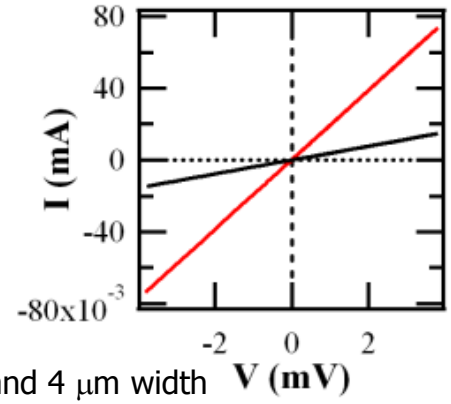
Alternative Conductors

- Graphene



D. Kondo et al., IITC2013





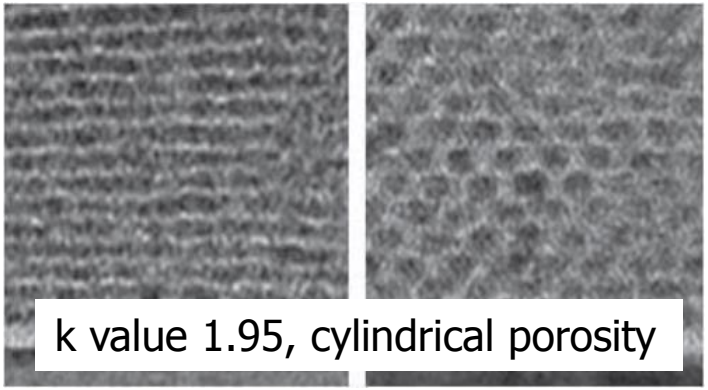
9.1 μΩcm at 6 μm length and 4 μm width

- Other candidates
  - CNT Interconnects
  - CNT-Cu composites

RC Reduction

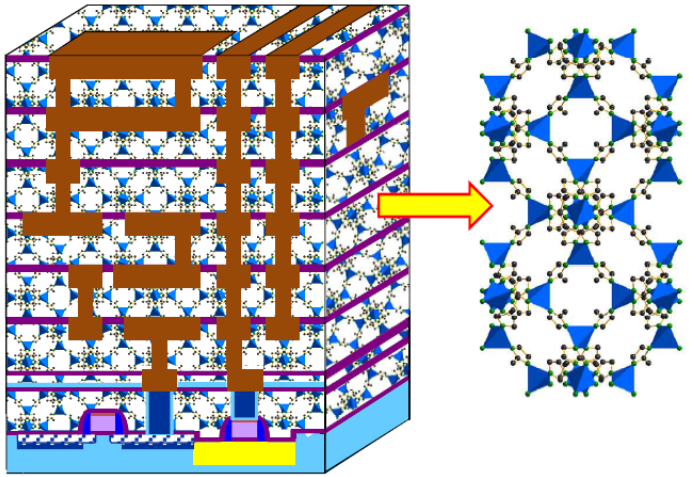
ULK Material Development

- Ordered Materials



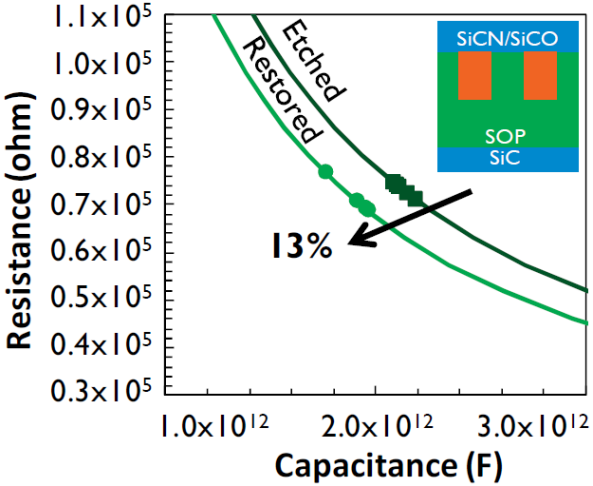
J. S. Clarke et al., VLSI2014

- MOF (Metal Organic Frameworks)
- COF (Covalent Organic Frameworks)



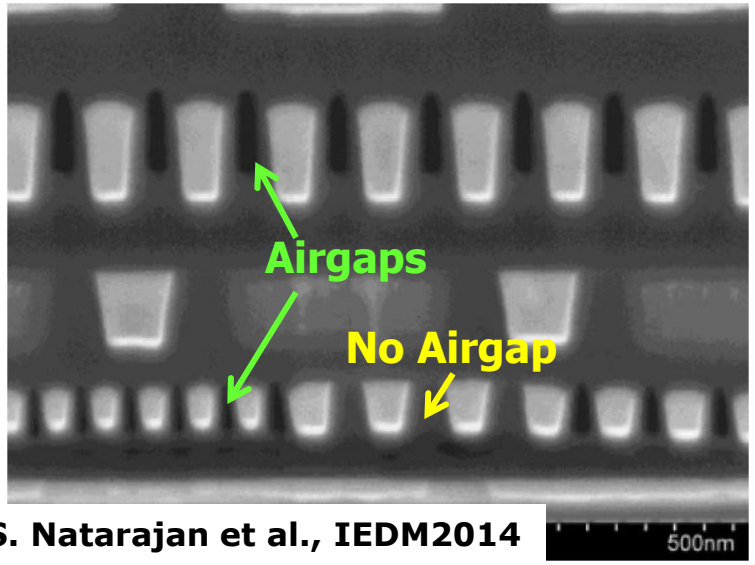
S. Eslava et al., Chem. Mater., 2013, 25 (1)

Damage Repair



C. J. Wilson et al., IITC2012

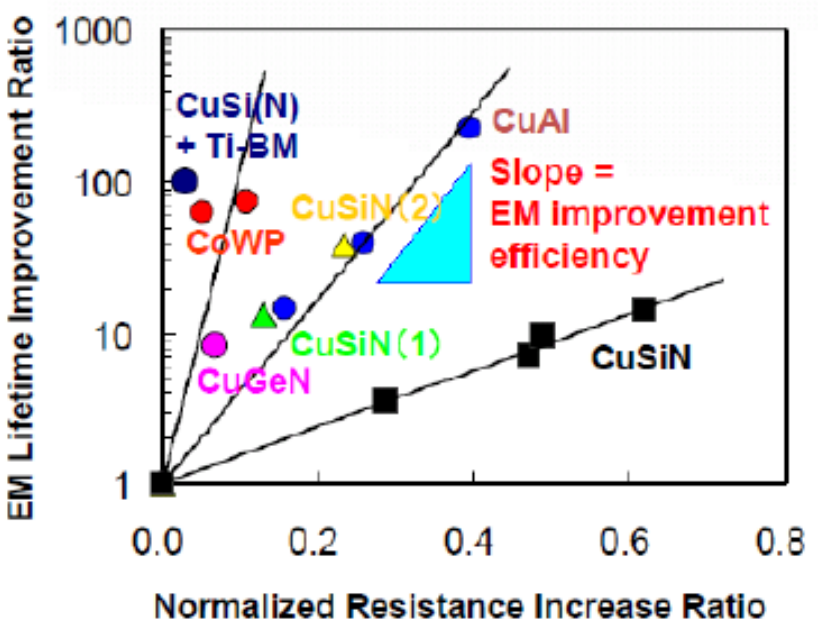
Airgap



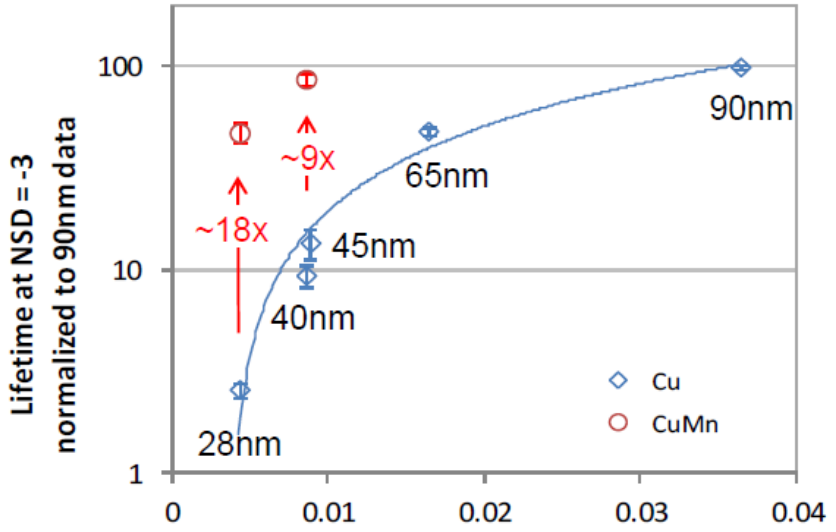
S. Natarajan et al., IEDM2014

Reliability Improvement

EM improvement by alloying

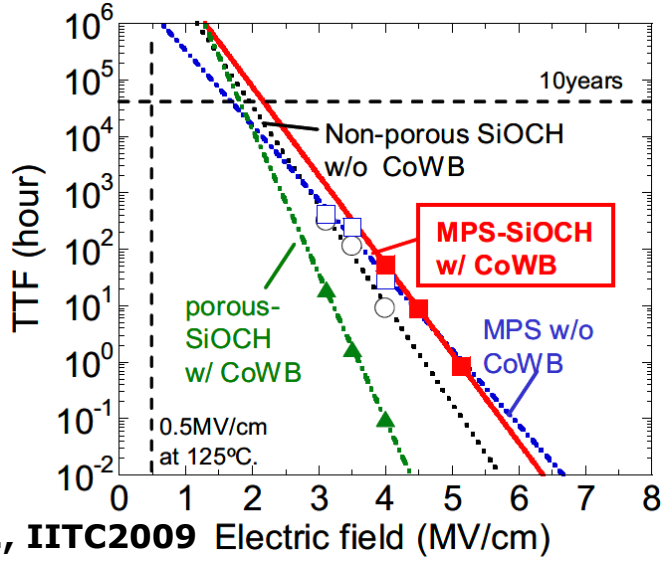


EM improvement by Cu-Mn alloy



Source: ITRS2013

TDDB improvement by structural management of ULK



M. Tagami et al., IITC2009

MPS: Molecular-Pore-Stack

ITRS2.0 (More Moore)

ITRS2.0関連

Critical Challenges	*Summary of Issues*
Materials *Mitigate impact of size effects in interconnect structures*	*Line and via sidewall roughness, intersection of porous low-κ voids with sidewall, barrier roughness, and copper surface roughness will all adversely affect electron scattering in copper lines and cause increases in resistivity.*
Metrology *Three-dimensional control of interconnect features (with its associated metrology) will be required*	*Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels, combined with new materials, reduced feature size and pattern dependent processes, use of alternative memories, optical and RF interconnect, continues to challenge.*
Process *Patterning, cleaning, and filling at nano dimensions*	*As features shrink, etching, cleaning, and filling high aspect ratio structures will be challenging, especially for low-κ dual damascene metal structures and DRAM at nano-dimensions.*
Complexity in Integration *Integration of new processes and structures, including interconnects for emerging devices*	*Combinations of materials and processes used to fabricate new structures create integration complexity. The increased number of levels exacerbate thermomechanical effects. Novel/active devices may be incorporated into the interconnect.*
Practical Approach for 3D *Identify solutions which address 3D interconnect structures and other packaging issues*	*Three-dimensional chip stacking circumvents the deficiencies of traditional interconnect scaling by providing enhanced functional diversity. Engineering manufacturable solutions that meet cost targets for this technology is a key interconnect challenge.*

Difficult Challengesとして上記TableをWhite Paper案として提出。

ITRS2.0 (More Moore)

ITRS2.0関連

	2013-15	2016-18	2019-21	2022-24	2025-27	2028-30
Node	N14	N10	N7	N5	N3	N1.5
Ground rules (CPP, MP, FP, LG) -[nm]	70, 52, 42, 20	52, 42, 30, 16	36, 30, 21, 14	25, 21, 14, 12	18, 14, 10, 10	12, 10, 7, 8
Conductor	Cu	Cu	Cu	Cu, Silicides, Carbon	Cu, Silicides, Carbon	Cu, Silicides, Carbon
Barrier Metal	Ta(N)	Ta(N), Mn(N)	Ta(N), Mn(N)	Ta(N), Mn(N), SAM	Ta(N), Mn(N), SAM	Ta(N), Mn(N), SAM
Alternative Transport				Collective Excitations	Collective Excitations	Collective Excitations
IMD (inter-metal dielectrics) and k value	SiCOH (2.55) Airgap (1.0)	SiCOH (2.40-2.55), Airgap (1.0)	SiCOH (2.20-2.55), Airgap (1.0)	SiCOH (2.20-2.55), Airgap (1.0), MOF, COF	SiCOH (2.00-2.55), Airgap (1.0), MOF, COF	SiCOH (1.80-2.55), Airgap (1.0), MOF, COF

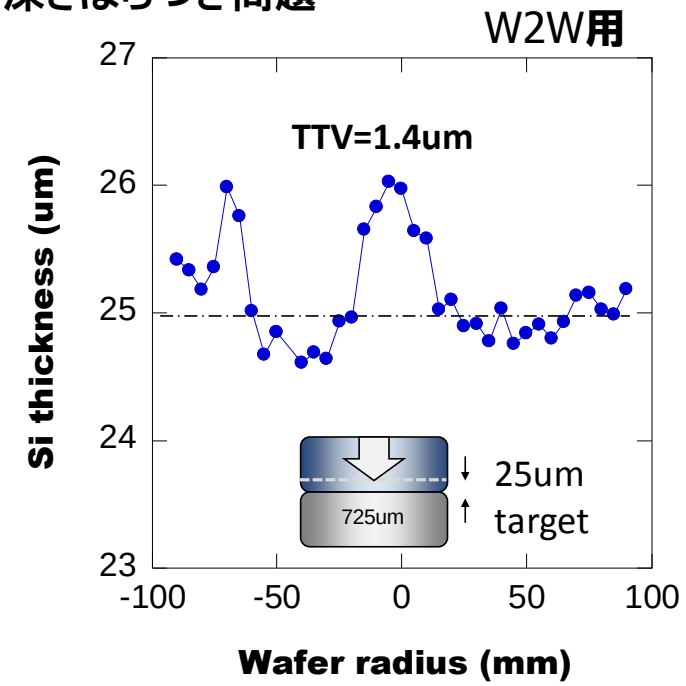
Potential Solutionsとして上記TableをWhite Paper案として提出。（一部修正）

3D実装技術の開発動向

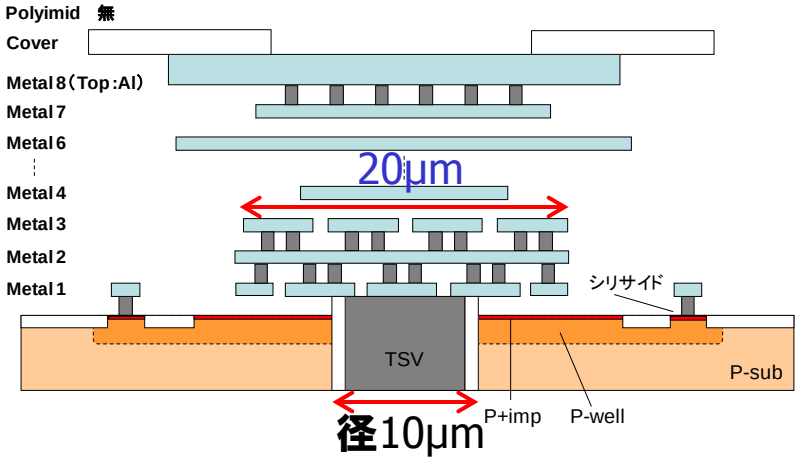
独自活動

VL-TSVプロセスにおける主な課題

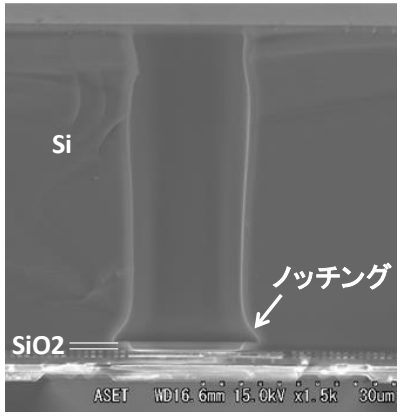
- 薄化の際の基板厚ばらつきによるTSV深さばらつき問題

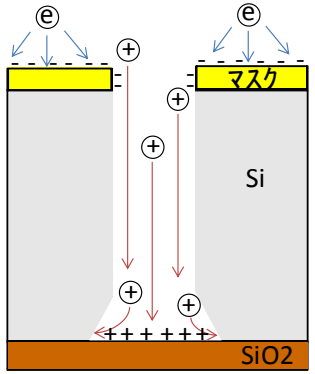


- TSVミスアライメント問題による狭ピッチ化への懸念



- TSV加工形状劣化によるバリアメタルやライナー膜のカバレッジ不良発生





Source: ASET公開資料

NEDO-PJ(Dream Chip, 実施者:ASET)で開発した裏面VL(Via Last)型TSVを用いた3D-LSIのプロセス、性能、信頼性等に関するヒアリングを実施。

先端CMOSデバイス技術の開発動向

独自活動

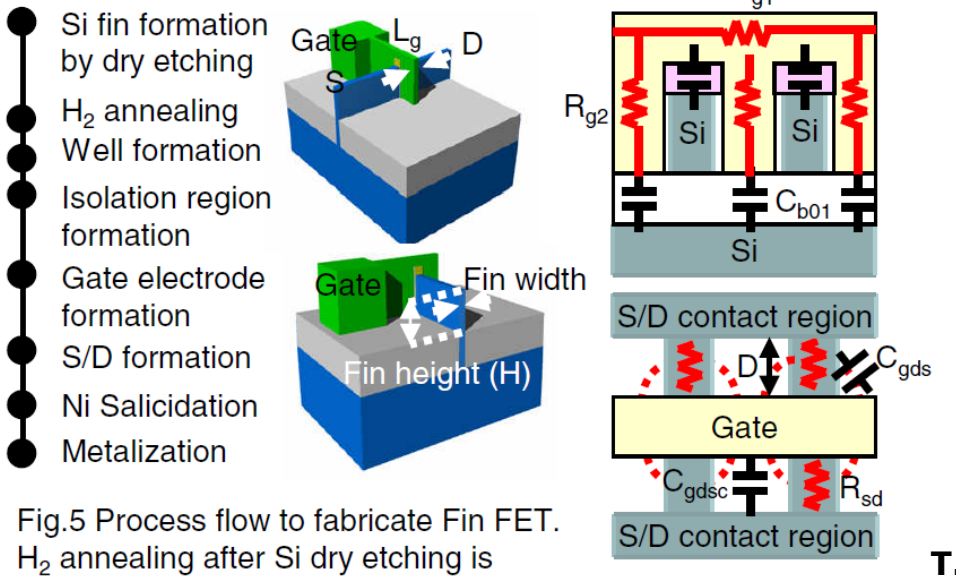


Fig.5 Process flow to fabricate Fin FET. H_2 annealing after Si dry etching is carried out to reduce trap density.

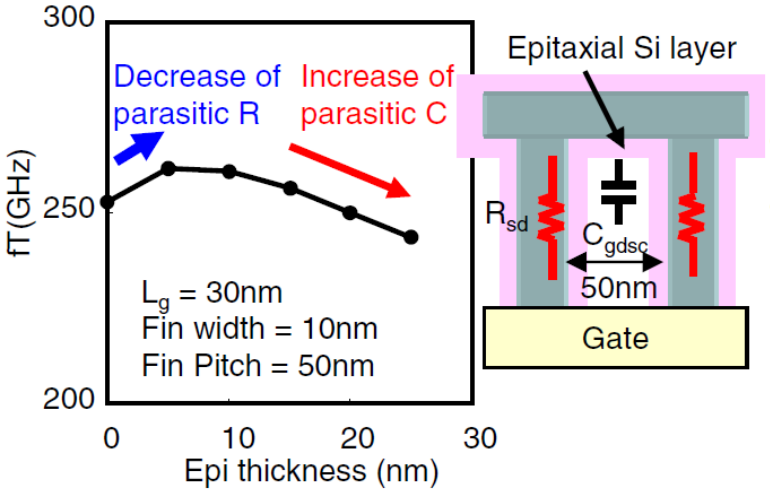


Fig.7 Dependence of f_T on epitaxial Si thickness grown on Source and drain to reduce parasitic resistance.

T. Ohguro et al., VLSI Tech. Symp. 2012

最先端デバイスや将来デバイスにおけるMetal0周りの構造を理解するため、ヒアリングを実施。

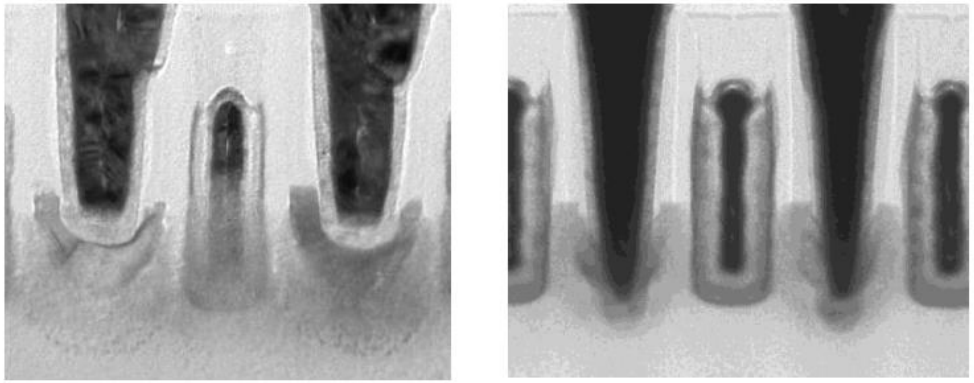
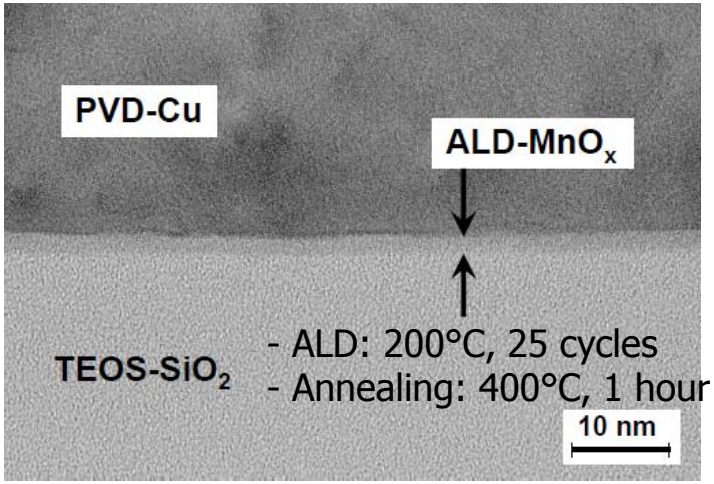


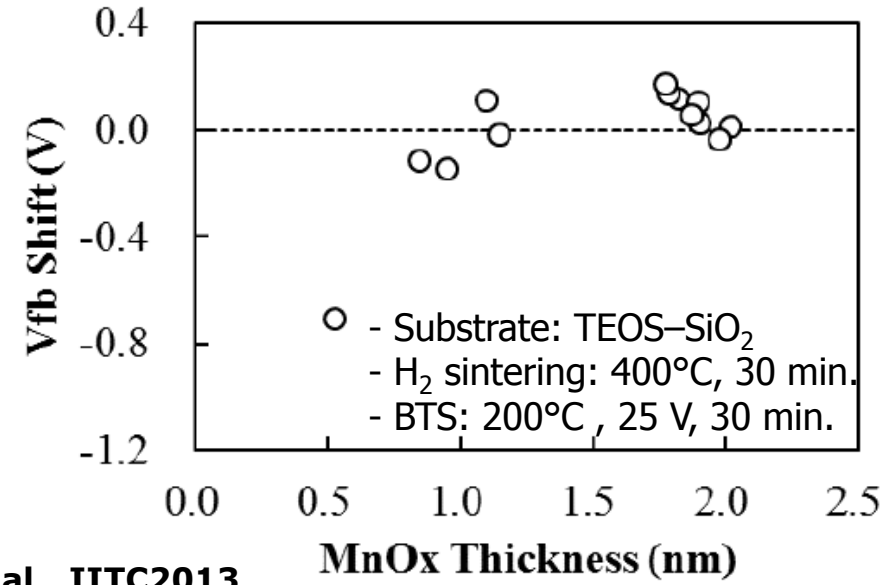
Fig.3 TEMs of tri-gate NMOS (left) and PMOS (right) transistors. Wrap-around of the contacts on S/D leads to illusion of contacts penetrating S/D on PMOS TEM.

C. Auth et al., VLSI Tech. Symp. 2012

バリアメタルを中心とした配線技術の開発動向

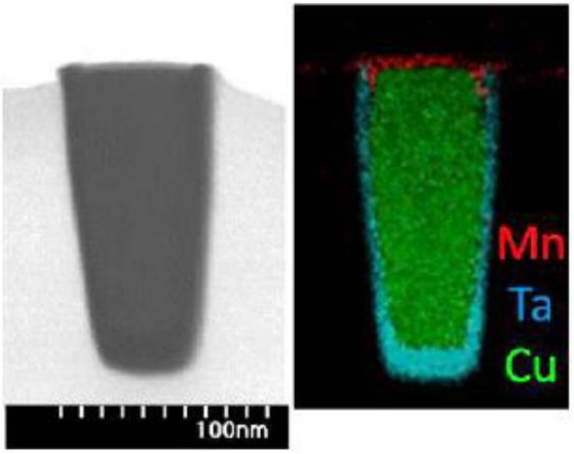
独自活動

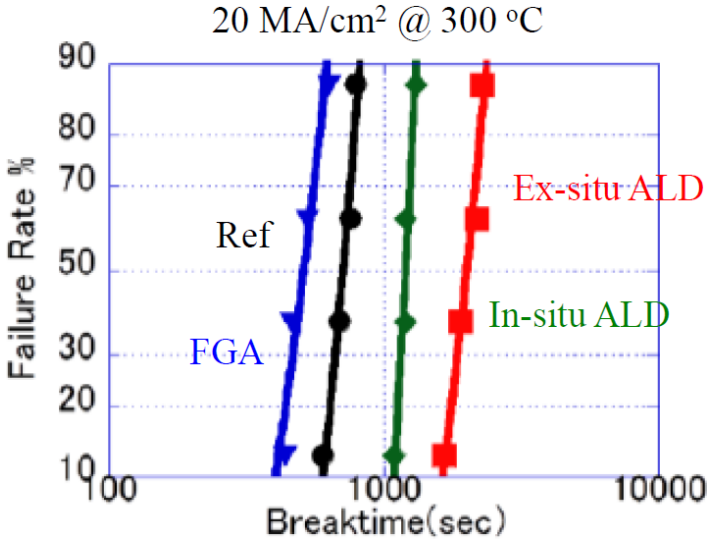




K. Matsumoto et al., IITC2013

Mn系バリアメタルによる膜厚1nm以下への可能性や、キャップメタルへの適用による信頼性向上のヒアリングを実施。

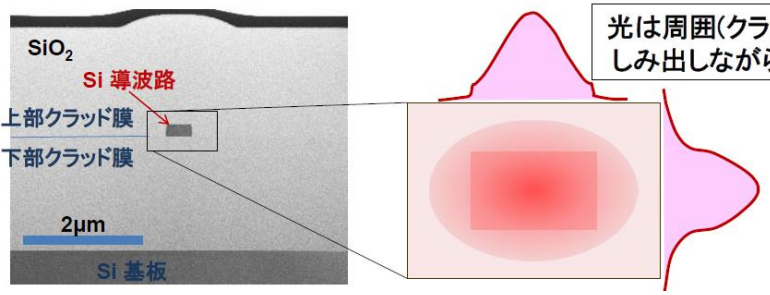


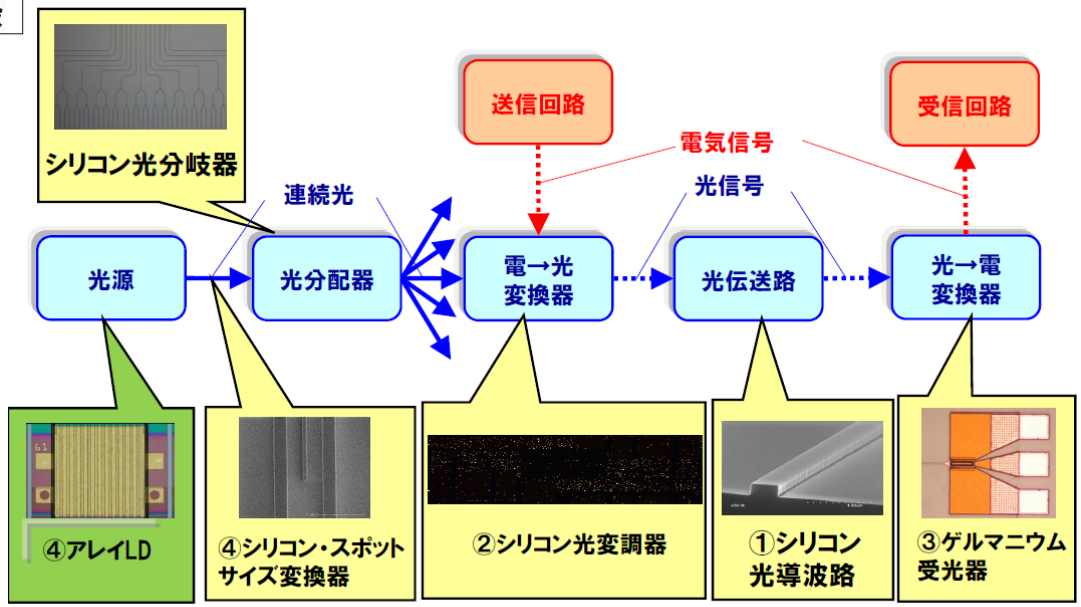


H. Kawasaki et al., IITC2014

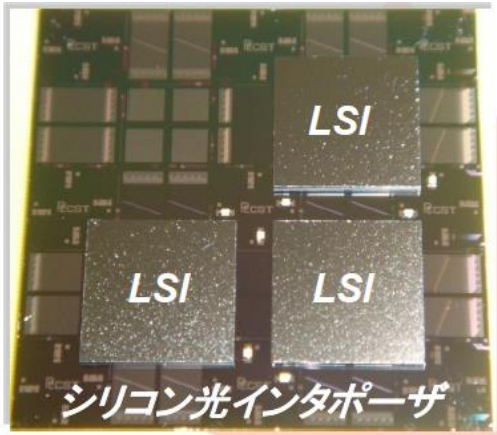
光配線技術の開発動向

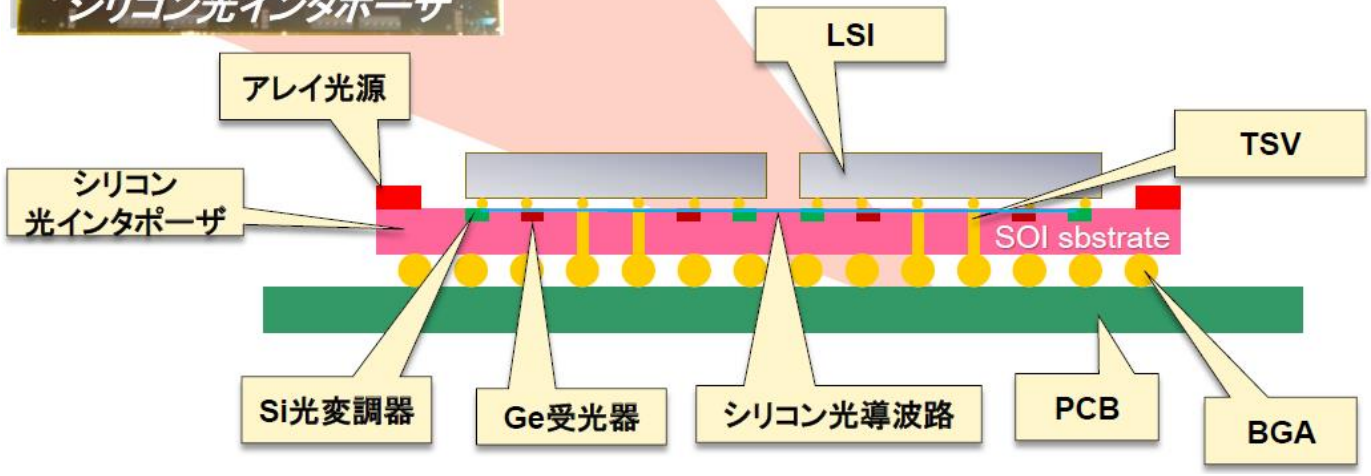
独自活動





LD以外は全てSiウエハプロセスで集積可能





Heterogeneous Integrationを念頭に、シリコンフォトニクス技術のヒアリングを実施。

Source: PETRA公開資料

2014年度活動のまとめと2015年度計画

◎ 2014年度の主な活動

★ ITRS関連活動

- ITRS2013の発行(含む和訳)
- ITRS2.0 White Paper発行に向けた資料作成
  (Focus Topics: Heterogeneous Integration, More Moore)

★ STRJ独自活動(技術動向調査)

- 3D実装技術
- 先端CMOSデバイス技術
- バリアメタルを中心とした配線技術
- 光配線技術

◎ 2015年度の活動予定

★ ITRS2.0関連活動: Heterogeneous Integration, More Mooreの配線パート作成

★ 独自活動: 微細化とMore than Mooreの配線技術動向調査