

International Technology Roadmap for Semiconductors 2001



富士通 (株)
福島 敏高

ITRSの変遷

米国 国内版

1991
Micro Tech 2000
Workshop Report

1992NTRS

1994NTRS

1997NTRS

国際版

2001 ITRS

<http://public.itrs.net>



2000 ITRS
Update

1999 ITRS



1998 ITRS
Update

1998

世界半導体会議
日米トップミーティング

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ITRSのミッション

IRC

・各国間調整

- ・方針
- ・目標
- ・スケジュール
- ・ITWG間調整



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対象技術分野

IRC

← クロスカット ITWGs →

専門 ITWG
(Focus)

	Environment Safety & Health	Metrology	Yield Enhancement	Modeling & Simulation
Design				
Test				
Front End Processes				
Interconnect				
Lithography				
Process Integration				
Assembly & Packaging				
Factory Integration				

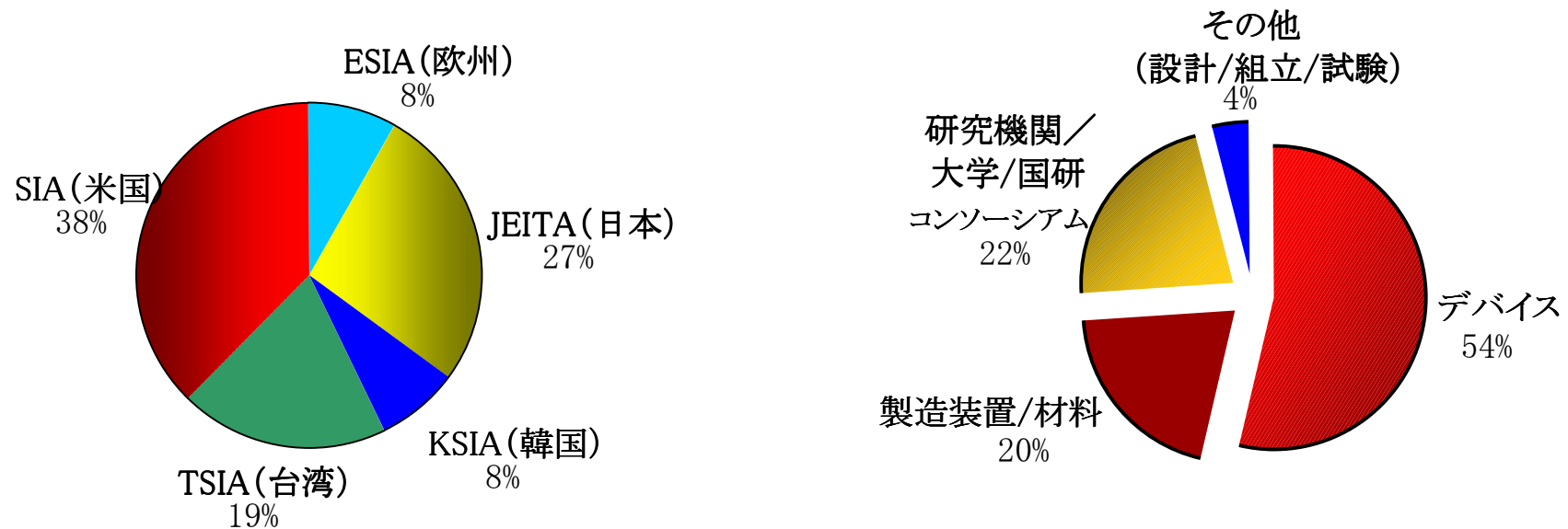
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ITRS 構成メンバー



	デバイス	製造装置/材料	研究機関/ コンソーシアム	大学	政府/国研	その他 (設計/組立/試験)	小計
ESIA (欧州)	38	5	25				68
JEITA (日本)	141	42	22	10	7		222
KSIA (韓国)	32	11	5	9	7		64
TSIA (台湾)	88	17	14	13		29	161
SIA (米国)	146	91	36	24	12	4	313
小計	445	166	102	56	26	33	828

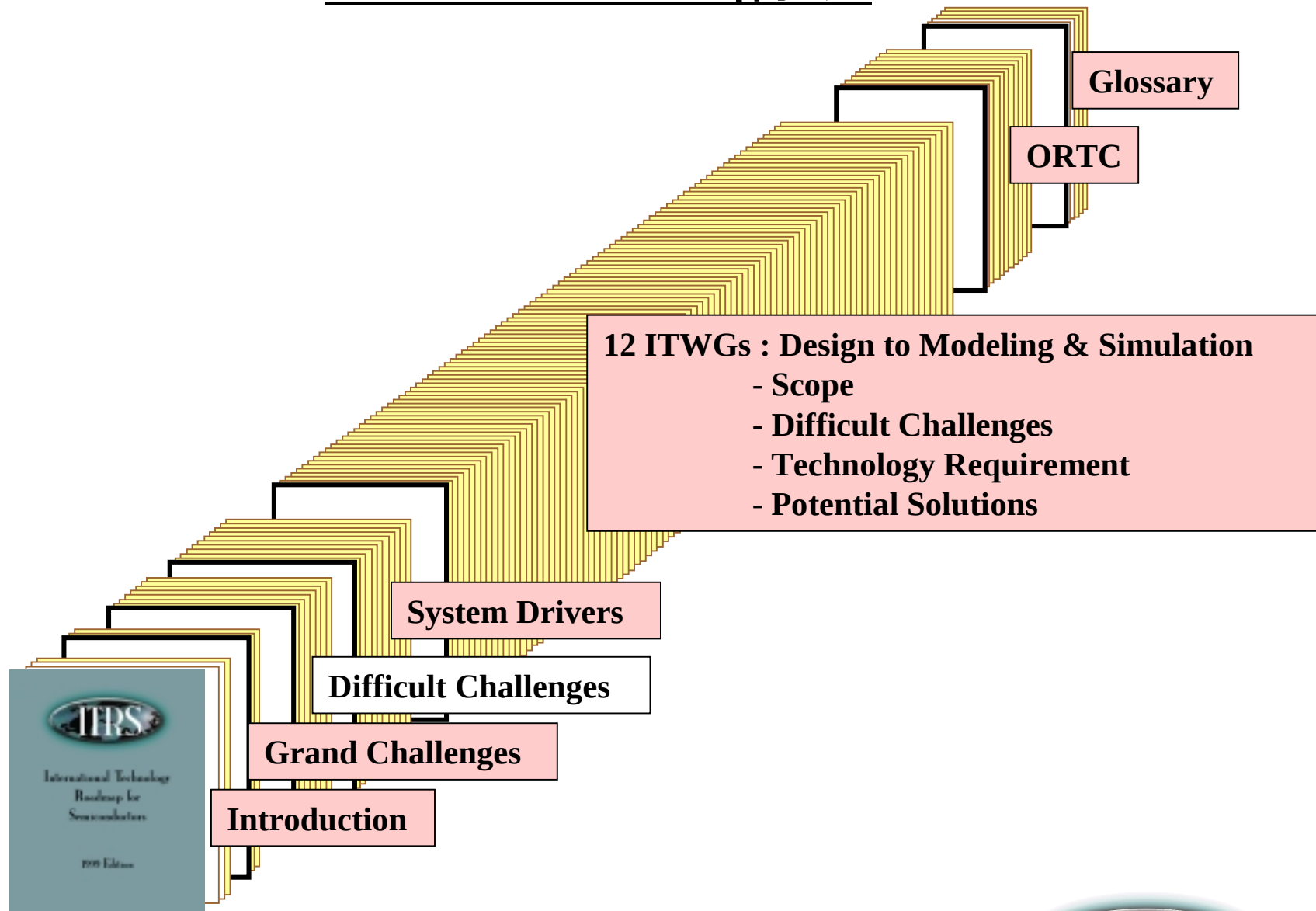
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ITRS2001の構成



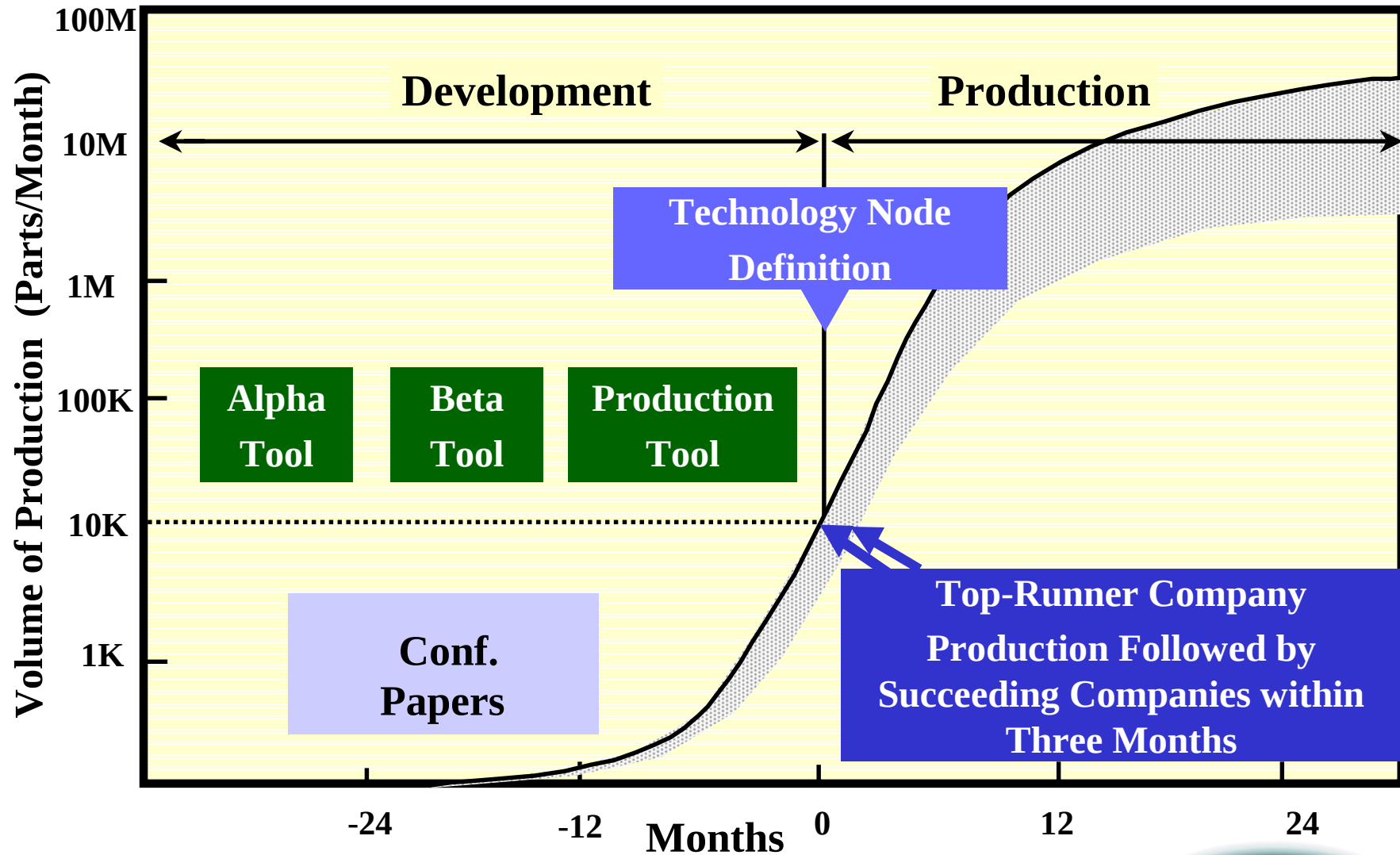
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Technology Node Timing



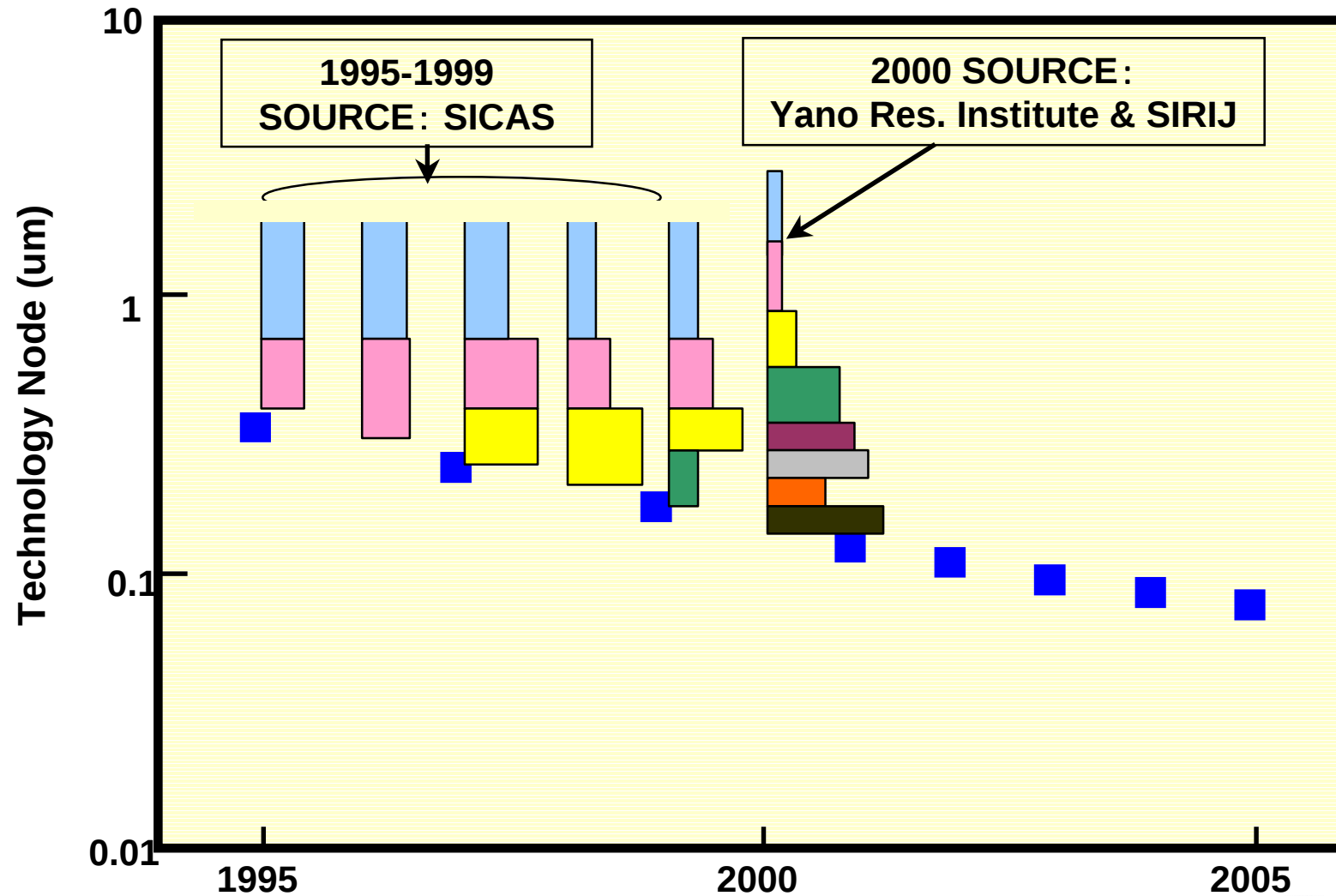
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Technology Distribution in Actual Production



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Technology Node

1999版					2001版 (nm)		
100	→	130	x 0.7	→	91	→	90
70	→	90	x 0.7	→	64	→	65
50	→	65	x 0.7	→	45	→	45
35	→	45	x 0.7	→	31	→	32
25	→	32	x 0.7	→	22	→	22

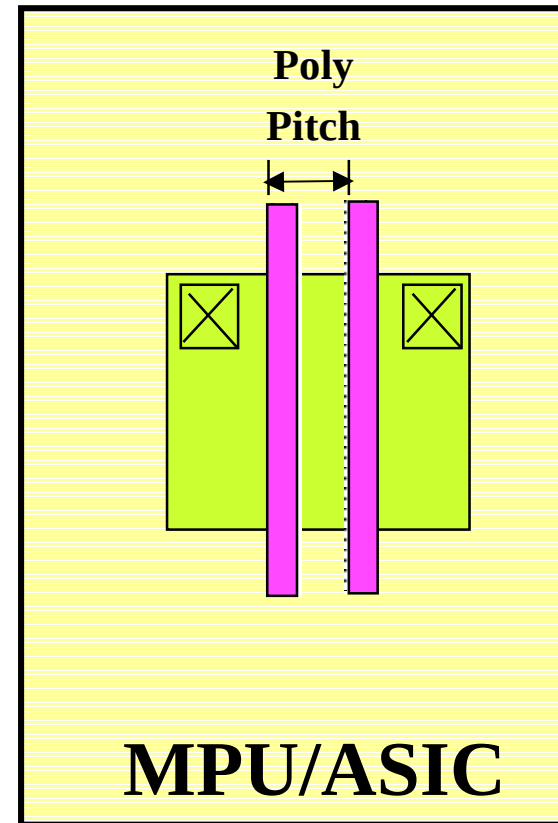
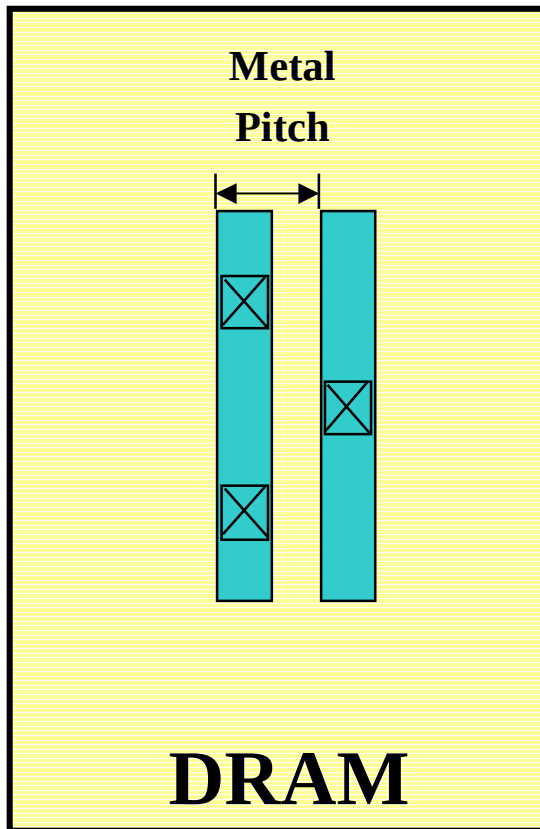
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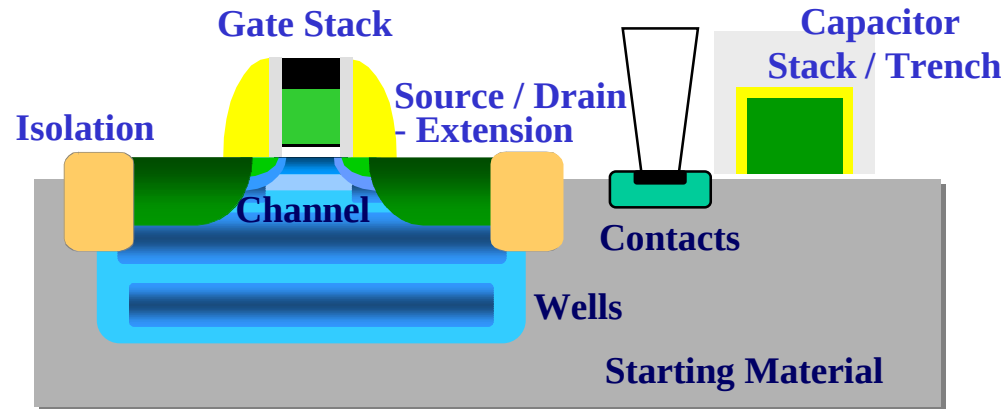
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Half Pitch



FEP Grand Challenges



Near Term (2001-2007)

Enhancing Performance

■ **New Gate Stack and Materials :**

- Oxynitride gate dielectric / high performance MOSFETs
- High κ gate stack / low operating and low standby power MOSFETs

■ **CMOS Integration of New Memory Materials and Processes :**

- High κ DRAM capacitor
- MIM capacitor structures

Long Term (2008-2016)

Cost-effective Manufacturing

■ **Starting Materials alternate beyond 300 mm :**

- Productivity enhancement

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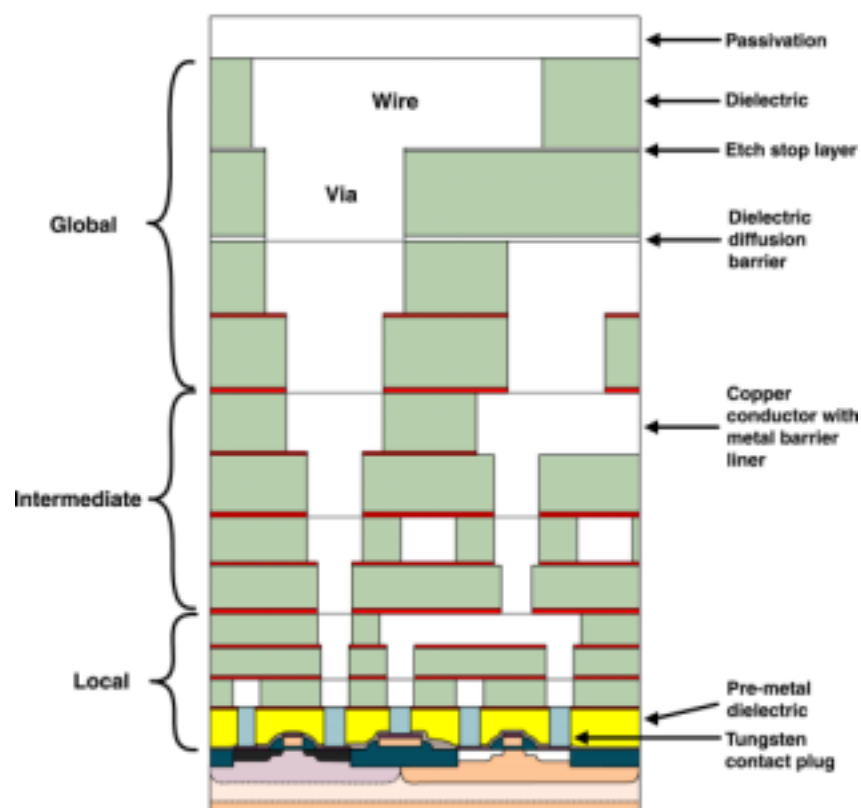
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Interconnect Grand Challenges

Typical Chip Cross Section



Near Term (2001-2007)

Enhancing Performance

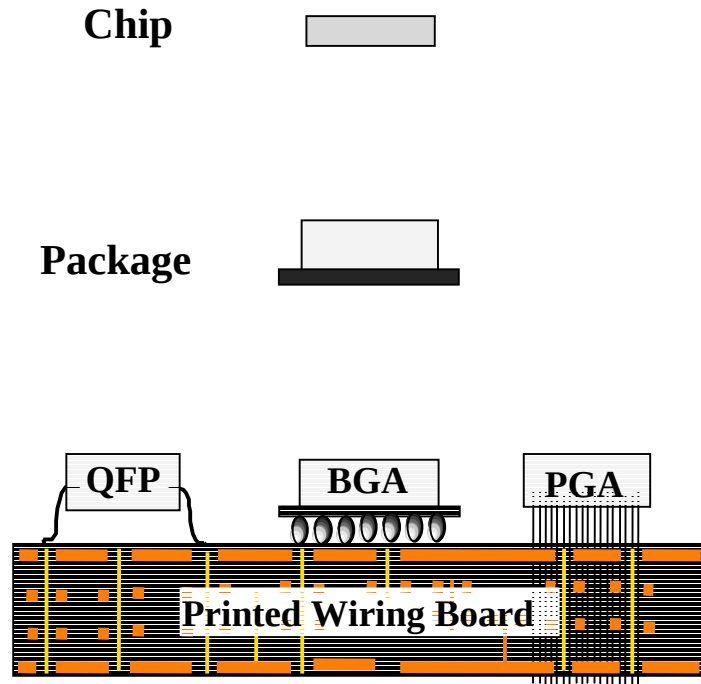
- Introduction of New Materials :
 - High Conductivity and High k Dielectric
- Integration of New Processes and Structures :
 - High Complexity

Long Term (2008-2016)

Enhancing Performance

- Identify Solutions which address Global Wiring Scaling:
 - Beyond Copper and Low k
 - Material Innovation to accelerate Design, Package and Interconnect

Assembly & PKG Grand Challenges



Near Term (2001-2007)

Cost-effective Manufacturing

■ Coordinated Design Tools and Simulators :

- Mix Signal Co-design and Simulation
- Transient Thermal Analysis Tool
- Thermal Mechanical Analysis Tool
- Electrical Analysis Tool
 - Power Disturbs
 - EMI
- High Frequency / Current and Lower Voltage Switching

System Drivers Chapter

1999年版

- SOC、AMS (analog/mixed-signal) に言及したが、主はDRAM、MPU、ASIC
- 其々の品種が、技術ノードに沿って、一様に開発されると仮定



2001年版

- しかし市場は、品種毎に異なった技術／開発時期を要求
- 市場セグメント毎の技術開発動向を分析
 - (1) Portable and Wireless
 - (2) Broadband
 - (3) Internet Switching
 - (4) Mass Storage
 - (5) Consumer
 - (6) Computer
 - (7) Automotive
- 市場セグメントが求める各品種に対する技術要求／開発時期を抽出
 - (a) SOC : Multi-technology, High performance, Low cost, Low power
 - (b) AMS : Low-noise amplifier, Power amplifier, VCO, ADC
 - (c) MPU : high-volume custom

Emerging Research Devices Section

1999年版

■ Beyond CMOS / Novel Devices



2001年版

■ ロードマップの延長線上で性能向上を加速させる技術

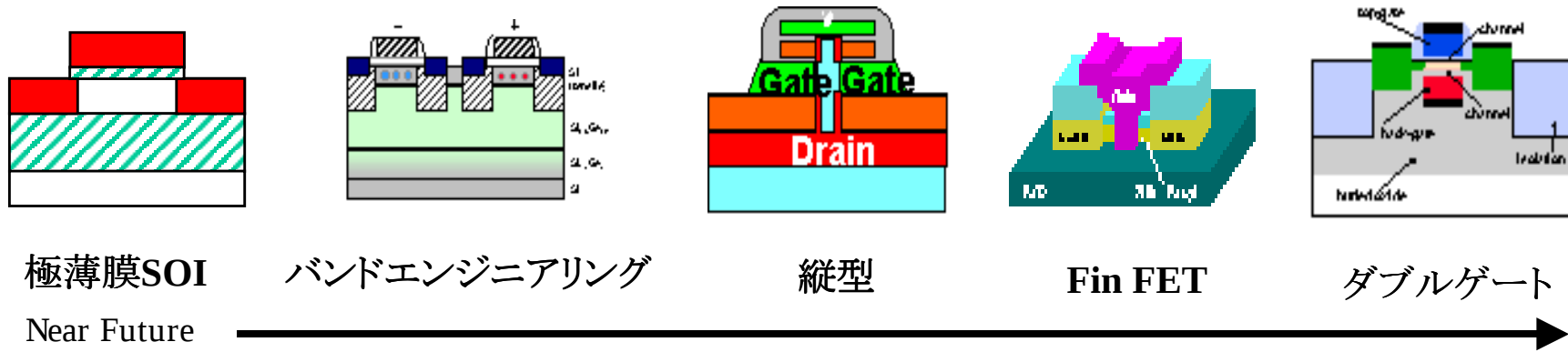
- Non-Classical CMOS
- 新メモリデバイス

■ ロードマップを越える新しい技術・概念

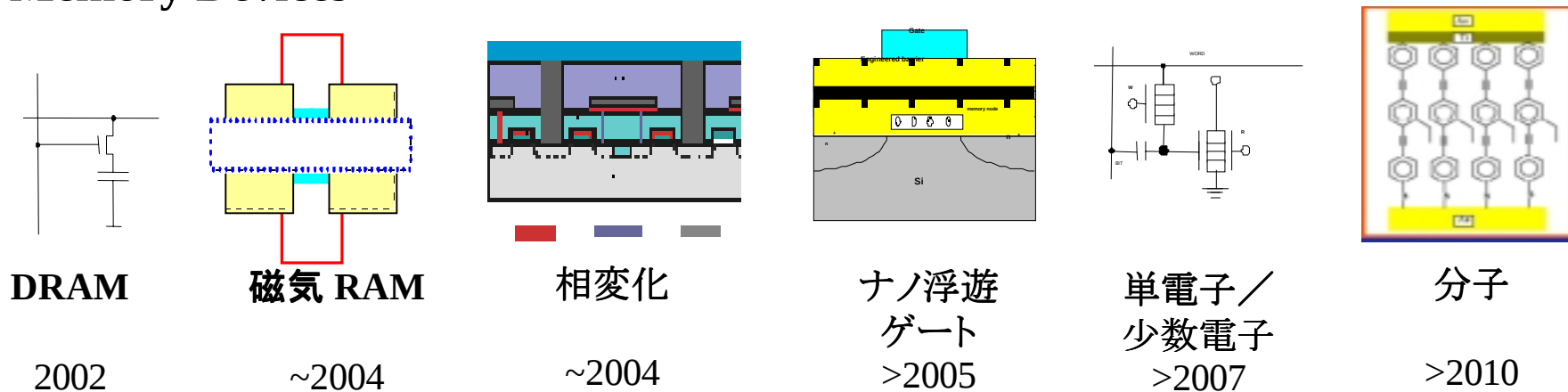
- 新ロジックデバイス
- 新アーキテクチャ

Emerging Research Technologies

Non-Classical CMOS



Memory Devices



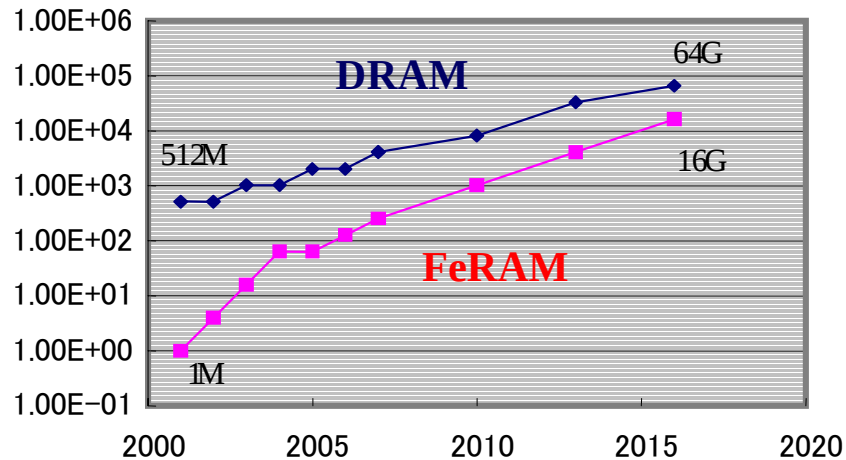
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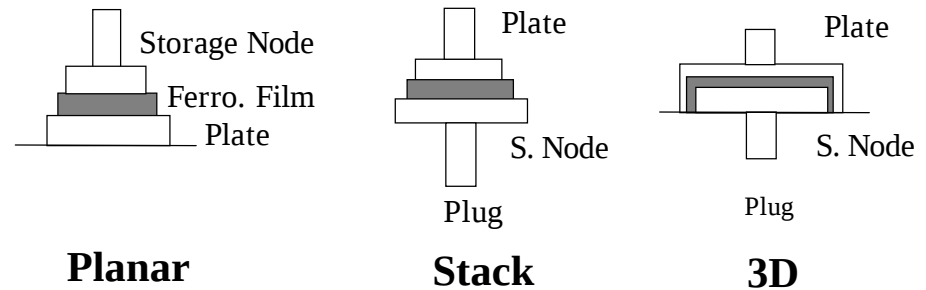
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FeRAM

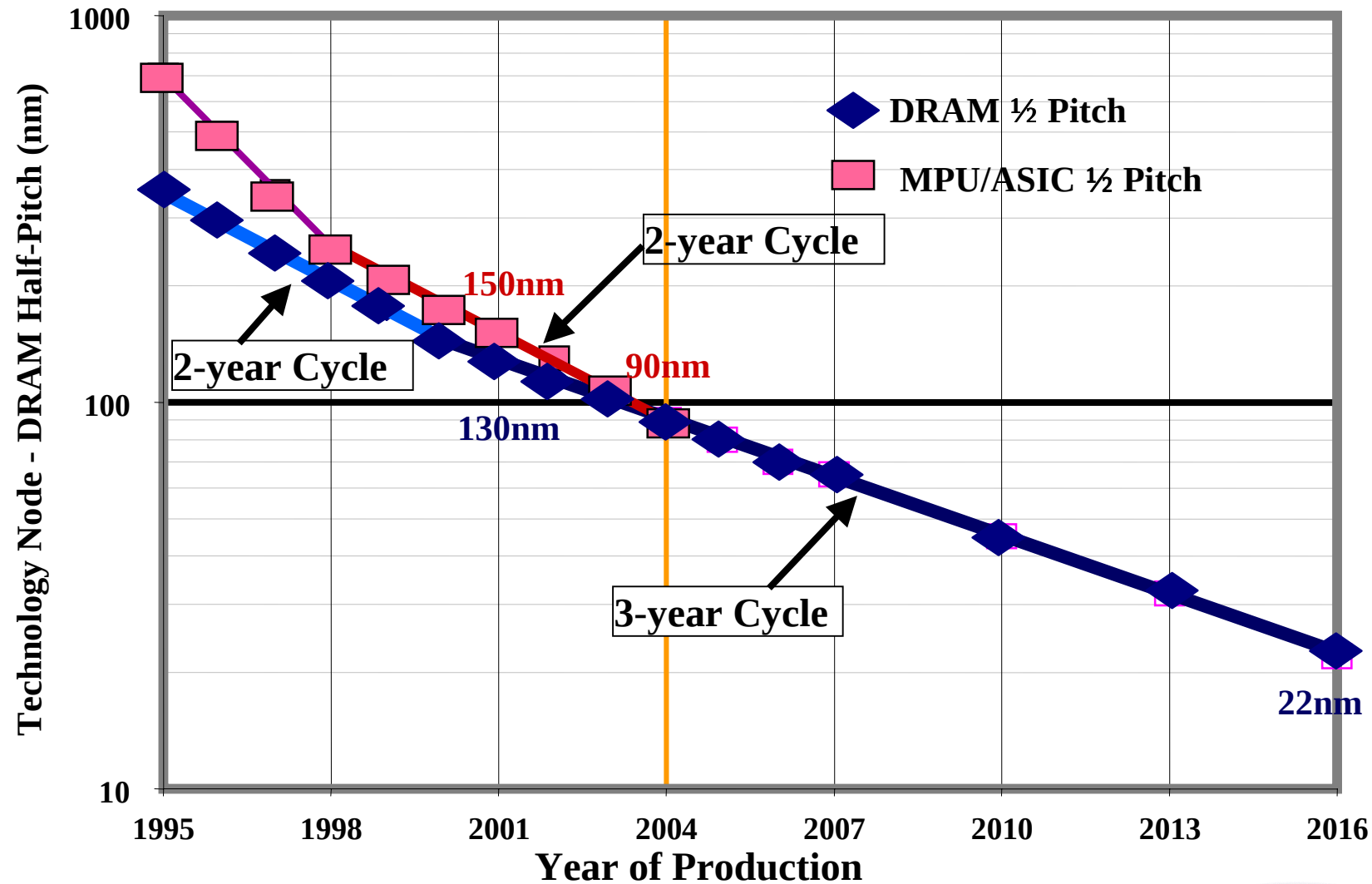


Capacitor Structure



	2001	2002	2003	2004	2005	2006	2007	2010	2013	2016
T. Node (nm)	130	115	100	90	80	70	65	45	32	22
DRAM (bit)	512M		1G		2G		4G	8G	32G	64G
FeRAM (bit)	1M	4M	16M	64M	64M	128M	256M	1G	4G	16G
Access time (ns)	80	65	55	40	30	30	20	16	12	10
Capacitor	planar	planar	stack	stack	stack	stack	3D	3D	3D	3D
T2C or 1T1C	2T2C	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C	1T1C

Half Pitch



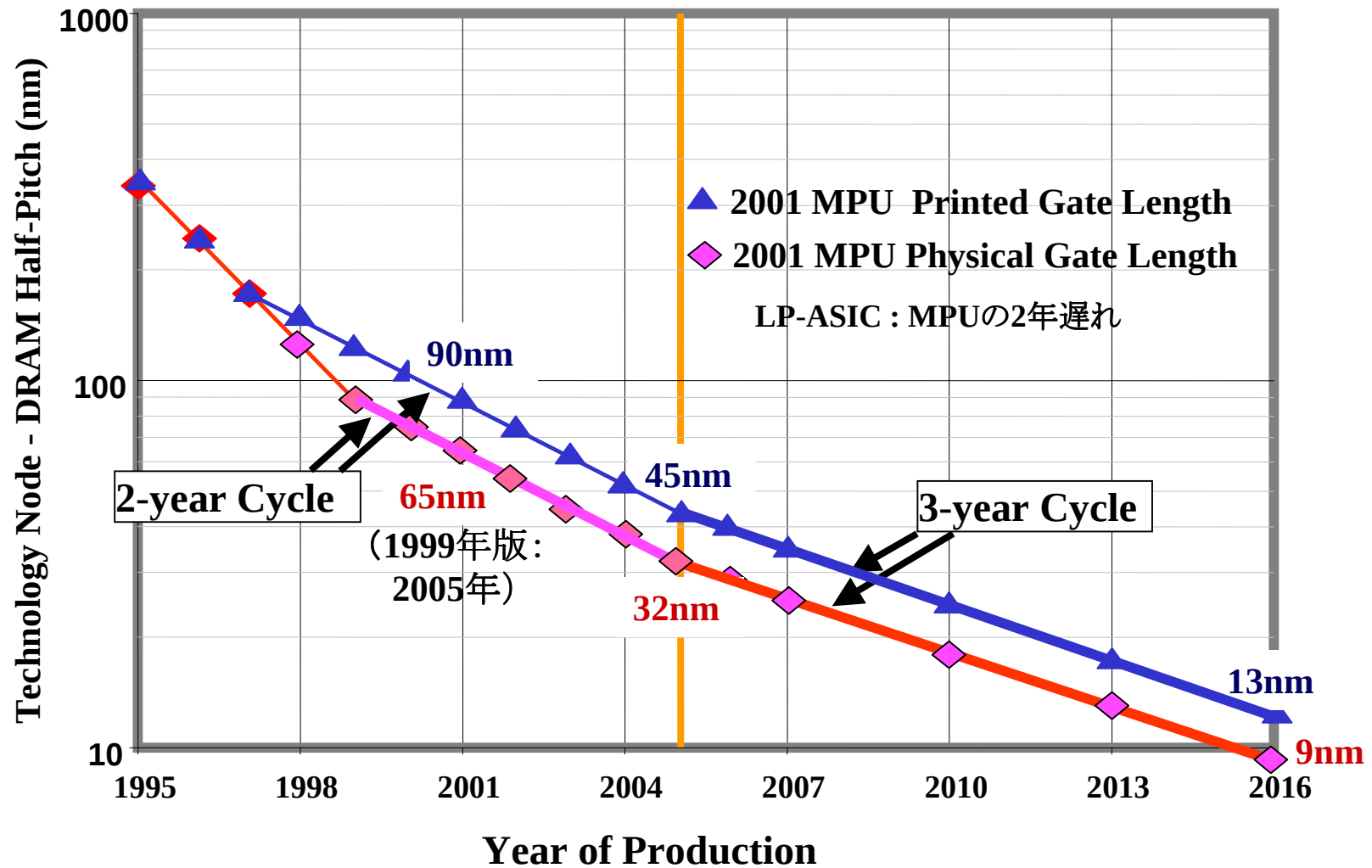
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MPU Gate Length



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Gate Dielectrics / EOT nm (High-k)

Year		2001	2002	2003	2004	2005	2006	2007	2008	2010	2011	2013	2014	2016
T. Node (nm)		130	115	100	90	80	70	65	70	45		32		22
1999年版														
EOT (nm)	MPU	1.5-1.9	1.5-1.9	1.5-1.9	1.2-1.5	1.0-1.5			0.8-1.2		0.6-0.8		0.5-0.6	
2001年版														
EOT (nm)	MPU/ASIC	1.3-1.6	1.2-1.5	1.1-1.6	0.9-1.4	0.8-1.3	0.7-1.2	0.6-1.1		0.5-0.8		0.4-0.6		0.4-0.5
	LOP	2.0-2.4	1.8-2.2	1.6-2.0	1.4-1.8	1.2-1.6	1.1-1.5	1.0-1.4		0.8-1.2		0.7-1.1		0.6-1.0
	LSTP	2.4-2.8	2.2-2.6	2.0-2.4	1.8-2.2	1.6-2.0	1.4-1.8	1.2-1.6		0.9-1.3		0.8-1.2		0.7-1.1
	DRAM	5	4.5	4.1	3.6	3.3	3	2.7		1.55		1.05		0.55

■ LSTPは2005年でHigh-kの導入が必要：
Ig<1pA/um, EOT=1.8nm

Effective Dielectric Constant (Low-k)

Year		2001	2002	2003	2004	2005	2006	2007	2008	2010	2011	2013	2014	2016
T. Node (nm)		130	115	100	90	80	70	65	70	45		32		22
1999年版														
k	MPU	2.7-3.5	2.7-3.5	2.2-2.7	2.2-2.7	1.6-2.2			1.5		<1.5		<1.5	
	DRAM	4.1	3.0-4.1	3.0-4.1	3.0-4.1	2.5-3.0			2.5-3.0		2.0-2.5		2.0-2.3	
2001年版														
k	MPU/ASIC	<2.7	<2.7	<2.7	<2.4	<2.4	<2.4	<2.1		<1.9		<1.7		<1.6
	DRAM	4.1	3.0-4.1	3.0-4.1	3.0-4.1	3.0-4.1	2.6-3.1	2.6-3.1		2.3-2.7		2.3-2.7		2.1

Lithography

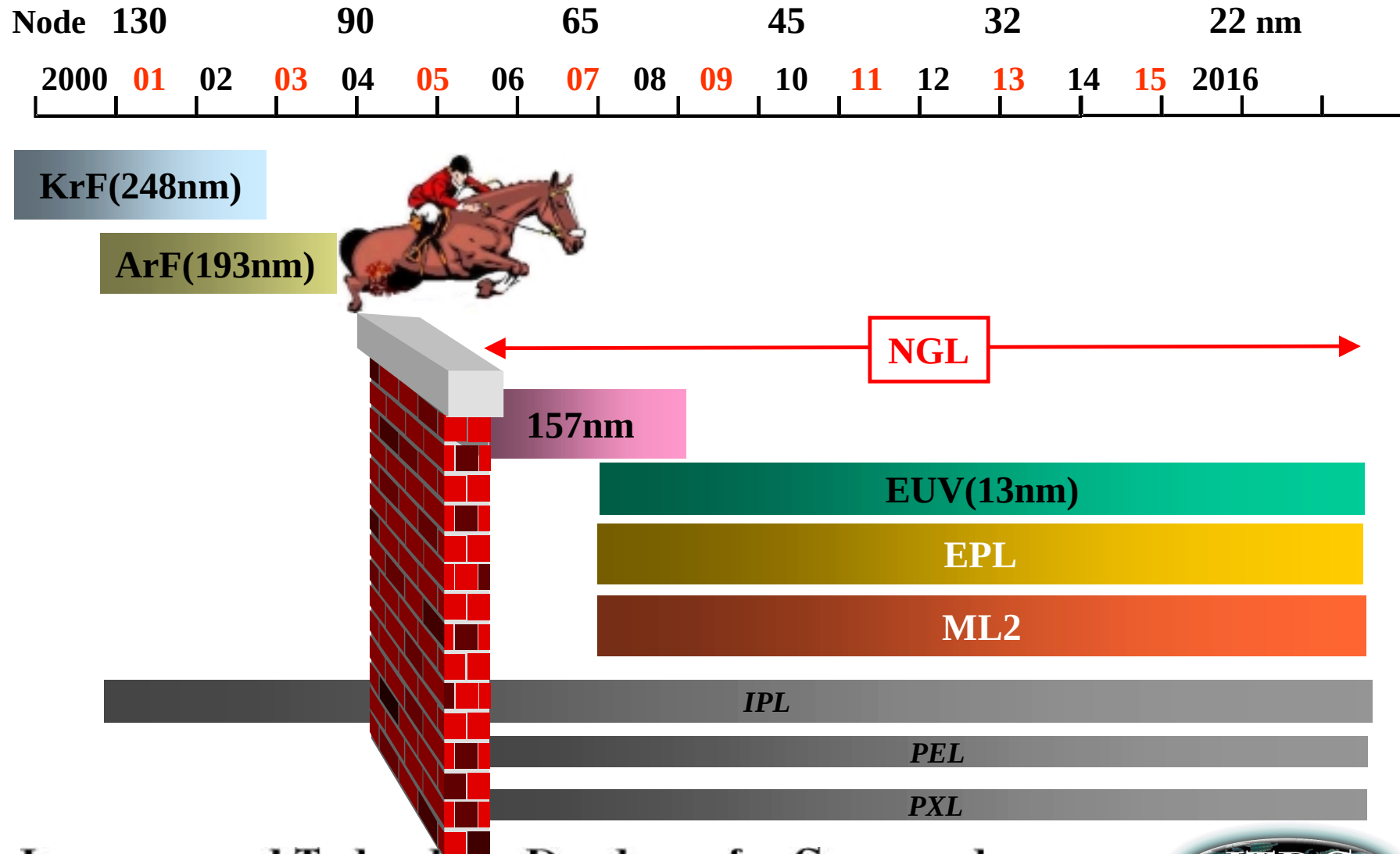
■ 光リソグラフィーを 65nm Node まで延長

- マスクの課題がクローズアップ
レジスト
マスクCD制御

■ 次世代リソグラフィ (NGL)

- マスクテーブルの新設
- コンセンサスに至らず混沌

Lithography Potential Solutions



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Design / Test / Assembly & PKG

■ Design

- 新規設計コスト・モデルの追加
 - ― 設計コストの増加が将来を脅かす

■ Test

- 信頼性評価の追加
 - ― DFTにより ITRS99 で指摘された多くの障害が取り除かれた
 - ― 潜在欠陥を加速する新しい手法の開発が急務

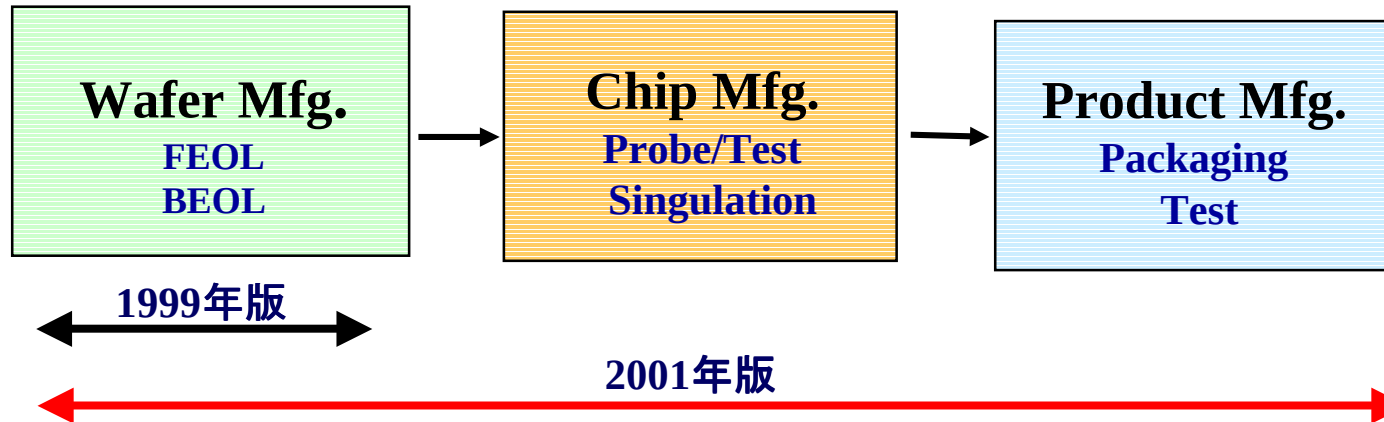
■ Assembly and Packaging

- スコープの拡大
 - ― MEMS、オプトエレクトロニクス、ディスクリート (**Passive Component**)
 - ― 受動部品内蔵基板

FI / YE

■ Factory Integration

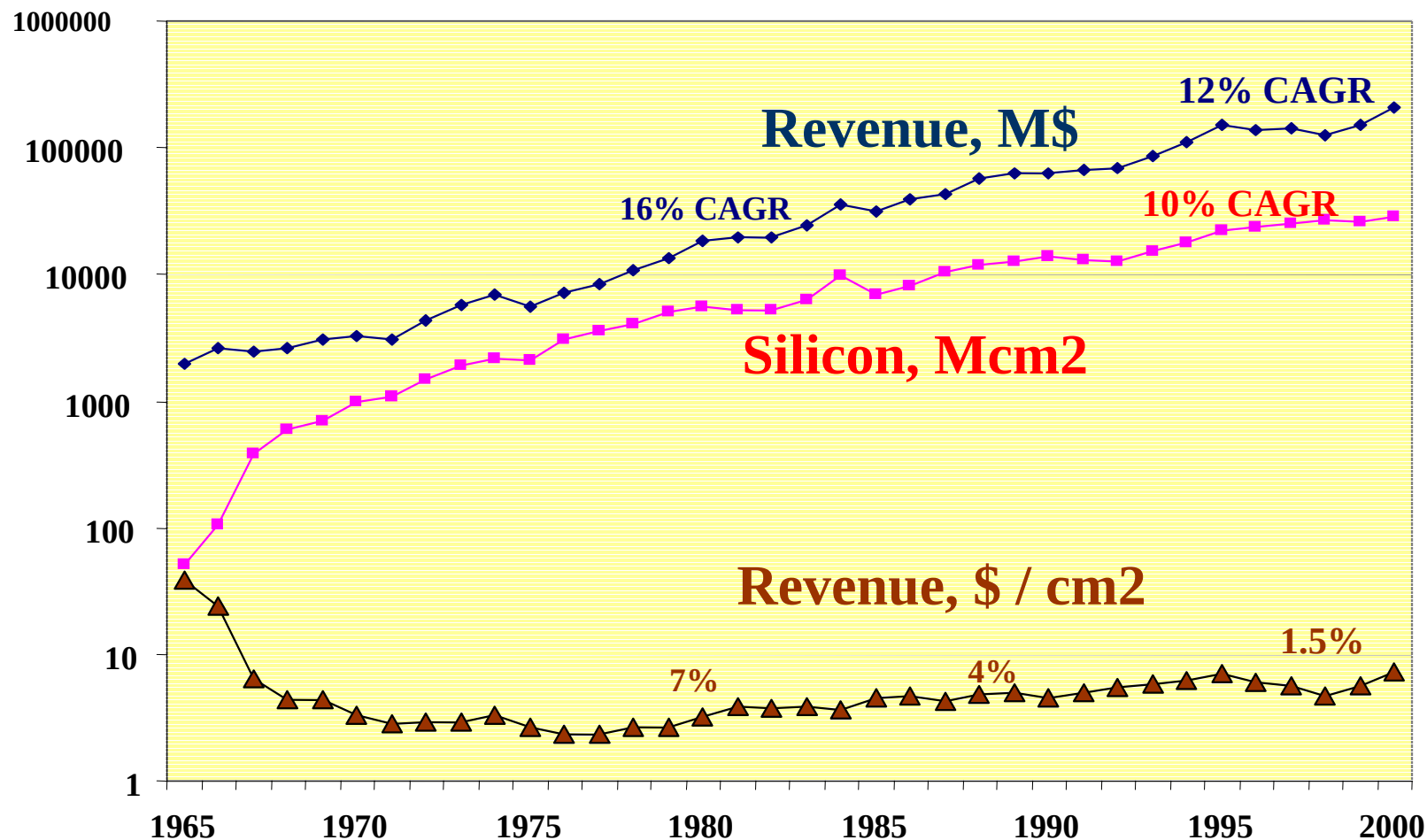
- スコープの拡大



■ Yield Enhancement (旧 Defect Reduction)

- スコープの拡大
 - Defect Detection and Characterization
 - Yield Learning

WW Semiconductor Industry Trends



Source Data: VLSI

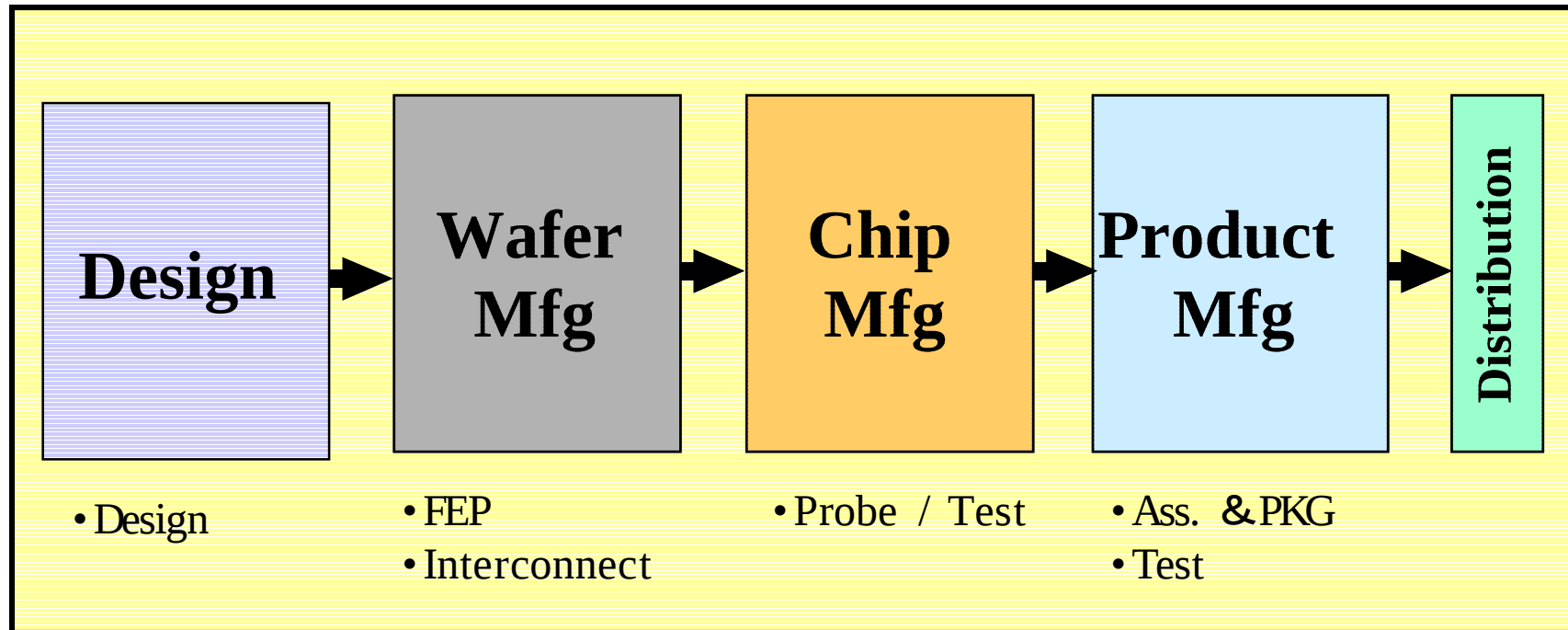
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Total Economy Modelの構築



まとめ

■ System Drivers Chapter

- 市場セグメント毎の技術開発動向の分析と、各品種に対する技術要求／開発時期を抽出

■ Emerging Research Devices Section

- Non-Classical CMOS、新メモリデバイス、新ロジックデバイス、新アーキテクチャを提案

■ DRAM half pitch

- 2001年以降3年サイクル (90nm@2004, 65nm@2007, 32nm@2010)

■ MPU / ASIC-HP half pitch

- 2年サイクルで微細化進み、2004年以降はDRAMと同じ

■ MPU / ASIC-HPのゲート長

- 2005年まで2年サイクルで微細化。LP-ASICはMPUの2年遅れ

■ High-k

- LSTP-ASIC用に2005年、MPU / HP-ASIC用に2007年より導入の必要

■ Low-kは減速

■ 光リソは65nmまで延命

- その後はコンセンサスに至らず

■ Total Economy Modelの構築が必要