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Yield Enhancement Cross-Cut Technology Working Group 2001 Version

2001の変更点

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Difficult Challenges

65nm node and above

- **Yield Model and Defect Budget**
  - Random and systematic yield models have to be developed and validated
  - Process induced defects, equipment generated particles, product/process measurements, and design/layout sensitivities have to be correlated to yield
- **Defect Detection and Characterization**
  - High-speed, cost-effective tools must be developed that rapidly detect defects associated with high-aspect ratio contacts/vias/trenches, and especially defects near/at the bottom of these features
- **Yield Learning**
  - Automated, intelligent analysis and reduction algorithms that correlate facility, design, process, test and WIP data must be developed to enable rapid root cause analysis of yield limiting conditions
  - Wafer-edge management required for yield/defectivity optimization
- **Wafer Environment Contamination Control**
  - Need adaptive water reclaim procedures keyed to particular process needs (define contaminants of interest and those not of interest)

Difficult Challenges
Less than 65nm

- **Yield Model and Defect Budget**
  - Yield models must comprehend greater parametric sensitivities, impact of circuit design, complex integration issues, greater transistor packing, ultra-thin film integrity, etc.
- **Defect Detection and Characterization**
  - Lack of enabling technology to detect or review defects
- **Yield Learning**
  - Failure analysis tools and techniques are needed to enable localization of defects where no visual defect is detected
  - IC designs must be optimized for a given process capability and must be testable/diagnosable.

Scope Expansions

- **Defect Detection and Characterization** 2001の変更点
  - Need recommendation for types of wafers (preparation) and process to be used for maximum sensitivity at each process step
  - Current detection recipes relatively insensitive to wafer-edge defectivity (exclusion area = 2 to 10 mm)

- **Yield Learning**
  - Specific recommendations for test structures and short loops including warning limits for generic process flows
  - Specific sampling model, including evaluation of inventory risk at each sampling level.

Technology Requirements:
Yield Model and Defect Budget

- **GOAL:** Provide reasonable and credible defect targets for tool suppliers

- **Approach Defect budget requirements for the 2001 ITRS:**
  - use results of a 1997, 1999, 2000 studies of current process-induced defects (PID) at Intl. SEMATECH Member Companies.

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  - Calculation based on the negative binomial yield model

$$Ysort = Ys * Yr = Ys * \left\{ \frac{1}{\left(1 + \frac{AD}{\alpha}\right)^{\alpha}} \right\}$$

Ysort = Probe Yield
Ys = Systematic Limited Yield
Yr = Random Defect Limited Yield
A = Chip Area (m^2)
D_0 = Electrical Fault Density ($/m^2$)
α = Cluster Factor

Technology Requirements:
Yield Model and Defect Budget

- **Extrapolation for future technology node requirements:**
  - from median PWP value for typical tool in each process module by considering increase in area, increase in complexity, and shrinking feature size.

$$PWP_n = PWP_{n-1} * \frac{F_n}{F_{n-1}\left(\frac{S_{n-1}}{S_n}\right)^2}$$

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Where:
PWP = Particle per Wafer Pass (/m²)
***n* = Technology Node of Interest**
F = Faults per Mask
S = Minimum Defect Size (nm)

- **Key assumption:**
  - No new process, material, or tool will be acceptable with a larger PWP budget than prior processing methods.
  - Defect budgeting method tends to be a worst case model since all process steps are assumed to be at minimum device geometry.

Technology Requirements:
MPU/DRAM Fault Density Assumptions

- **Assumptions defined in the "Overall Requirements Table Chapter" (ORTC) by the ITRS Die Size WG with $Y_{sort} = Y_s * Y_r$**

Product	*MPU*	*DRAM*
Yield Ramp Phase	*Ramp Phase End*	*Production Phase End*
$Y_{OVERALL}$	75%	85%
Y_{RANDOM}	83%	89.5%
$Y_{SYSTEMATIC}$	90%	95%
Cluster Parameter	5	5

- **With this assumption Defect Budget Targets for MPU and DRAM were calculated**

Yield Model and Defect Budget Tables 76-77

Key 2001 Updates

2001の変更点

- Defect budget target calculation makes use of data from 3 different surveys of ISMT Member Companies (1997, 1999, 2000)
- Defect budget targets include wafer-handling defectivity, for 2001 reduced # of handling steps in generic process flow

2001の変更点

- DRAM defect budget targets not extrapolated from the MPU data, but calculated based on a generic DRAM process flow
- Key assumptions:
  - Random & systematic yield targets same as 1999/2000
  - Model assumes that redundancy is sufficient such that array is not limiting DRAM yield
  - All process steps are at minimum device geometry
- Technology requirement color-code determined by tool yield impact partitioning study
- Including a calculator for DRAM & MPU tool defect budget targets
  - Critical Defect Size, RDLY target, Die Size, # Mask Levels and Cell area user definable

Table 76: YMDB - MPU

Technology Requirements - continued

MPU Random Particles per Wafer pass (PWP) Budget (defects/m2) for Generic Tool Type scaled to 75nm critical defect size or greater (F)										
Year of Introduction	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*	*2010*	*2013*	*2016*
"Technology Node"	*130nm*	*115 nm*	*100nm*	*90nm*	*80nm*	*70nm*	*65nm*	*45nm*	*32nm*	*22nm*
CMP Clean	448	337	228	161	127	90	78	37	18	8
CMP Insulator	1084	814	552	390	308	219	189	90	43	20
CMP Metal	1225	920	623	441	348	247	213	102	48	23
Coat/Develop/Bake	196	147	100	70	56	39	34	16	8	4
CVD Insulator	963	772	523	370	292	207	179	86	40	19
CVD Oxide Mask	1267	950	644	455	360	255	220	105	50	23
Dielectric Track	308	232	157	111	88	62	54	26	12	6
Furnace CVD	549	412	279	198	156	111	95	46	22	10
Furnace Fast Ramp	497	373	253	179	141	100	86	41	19	9
Furnace Oxide/Anneal	321	241	164	116	91	65	56	27	13	6
Implant High Current	430	323	219	155	122	87	75	36	17	8
Implant Low/Med Current	392	295	200	141	112	79	68	33	15	7
Inspect PLY	400	300	203	144	114	81	70	33	16	7
Inspect Visual	429	323	219	155	122	87	75	36	17	8
Litho Cell	332	250	169	120	95	67	58	28	13	6
Litho Stepper	315	237	160	113	90	64	55	26	12	6

2001の変更点

Table 76: YMDB - MPU

Technology Requirements - continued

MPU Random Particles per Wafer pass (PWP) Budget (defects/m2) for Generic Tool Type scaled to 75nm critical defect size or greater (F)										
Year of Introduction	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*	*2010*	*2013*	*2016*
"Technology Node"	*130nm*	*115 nm*	*100nm*	*90nm*	*80nm*	*70nm*	*65nm*	*45nm*	*32nm*	*22nm*
Measure CD	374	281	190	135	106	75	65	31	15	7
Measure Film	321	241	164	116	91	65	56	27	13	6
Measure Overlay	298	224	152	107	85	60	52	25	12	6
Metal CVD	585	439	298	211	166	118	102	49	23	11
Metal Electroplate	302	227	154	109	86	61	52	25	12	6
Metal Etch	1300	976	661	468	370	262	226	108	51	24
Metal PVD	667	501	339	240	190	135	116	56	26	12
Plasma Etch	1183	889	602	426	336	239	206	99	46	22
Plasma Strip	547	411	278	197	156	110	95	46	21	10
RTP CVD	357	268	181	128	101	72	62	30	14	7
RTP Oxide/Anneal	234	175	119	84	66	47	41	19	9	4
Test	91	69	47	33	26	18	16	8	4	2
Vapor Phase Clean	822	617	418	296	234	166	143	68	32	15
Wafer Handling	37	28	19	13	10	7	6	3	1	1
Wet Bench	535	402	272	192	152	108	93	45	21	10

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Defect Calculator

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Table AA Defect Target Calculator

	MPU	DRAM	USER INPUT	
Minimum Critical Defect Size (nm)	*75*	*65*	75	
Random Defect limited Yield (%)	*83.0%*	*89.5%*	83.0%	
Chip Size (mm^2)	*140*	*127*	140	
Number of Mask Levels	*25*	*21*	25	
Peripheral (Logic) Chip Area (%)	*NA*	*45.0%*	100.0%	
Random D_0 ($faults/m^2$)	*1356*	*1963*	1356	1356
Random Faults/Mask	*54*	*93*	54	54
			User Targets	
			MPU	*DRAM*
CMP Clean	448	1072	448	828
CMP Insulator	1084	830	1084	641
CMP Metal	1225	1272	1225	983
Coat/Develop/Bake	196	331	196	256
CVD Insulator	963	920	963	711
CVD Oxide Mask	1267	1129	1267	872
Dielectric Track	308	465	308	359
Furnace CVD	549	635	549	491
Furnace Fast Ramp	497	599	497	463
Furnace Oxide/Anneal	321	479	321	370
Implant High Current	430	557	430	430

Defect Detection Table 78
Key 2001 Updates

- **ITRS Node definition updated to reflect changes made to the ORTC Tables with respect to year/technology node.**
- **High Aspect Ratio inspection can only be achieved at extremely low throughput (1 wafer/hour) and high cost of ownership ($20-$50/wafer). Therefore, it is not a manufacturing process and is currently "red".** 2001の変更点
- **Backside particle size line was reinstated into Table 78 due to member interest.** 2001の変更点

Yield Learning
Key 2001 Updates

- **Yield Learning**
  - **The time necessary to source manufacturing problems is approximately 50% of the theoretical process cycle time on average during yield ramp**
  - **In order to keep the yield learning rate manageable, the process development and technology transfer to manufacturing must be optimized to minimize new defect sources/mechanisms during yield ramp.**
  - **Integrated Data Management (IDM) is critical for maintaining productivity comprehending**
    - **integrated circuit design**
    - **visible defects**
    - **non-visual defects**
    - **parametric data**
    - **electrical test faults**
    - **process trends and excursions**
    - **rapid identification of yield detracting mechanisms**

2001の変更点

Wafer Environment Contamination Control

Key 2001 Updates

- **Atmospheric/Airborne Wafer Environmental Control**
  - Believe assumptions used in past will continue to hold up (e.g. particle deposition, molecular adsorption)
  - No real drivers identified to justify significant deltas from 1999/2000
  - Will tap into SEMI mini-environment group currently collecting data on Atomic/Molecular Contamination (AMC) for standards
  - Must consider capture of reticle requirements for AMC
- **Ultra-Pure H20**
  - Particles: align with defect detection
  - Current mis-match between projected capability (filtration) and detection. Will show projected capability in table.
  - Create “most critical” / “less Critical” categories for ions and metallics.
  - Must coordinate better w/ ESH on water conservation/reclaim.
  - Need sanity check on surface prep.
- **Chemicals**
  - Focus on correcting inconsistencies: Chemical vs Water.
- **Gases**
  - Basically no changes except fo / ORTC Scenarios
  - Likely to remove corrosives fo d add new category for ILD precursors.

2001の変更点

Table 80: Wafer Environment Contam. Control

Test Methodology for Ultrapure Water

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PARAMETER	*MEASURED (POD/POC)*	*TEST METHOD*
Resistivity	Online	Electric cell
Viable bacteria	Lab	Incubation
EPI Bacteria	Lab	Stained samples w/ Fluorescent Microscopy
Scan RDI	Lab	Laser-scanning Cytometry
TOC	Online	Resistivity / CO_2
Reactive Silica	Online or Lab	Colormetric
Colloidal Silica	Calculation	Total minus Reactive
Total Silica	Lab	ICP/MS
Particle Monitoring	Online	Light scatter
Particle Count	Lab	SEM – Capture filter at various pore sizes
Cations, anions, metals	Lab	Ion chromatography, ICP/MS
Dissolved O_2	Online	Electric Cell