WG5 Lithography

- 次の本命は何か? そして間に合うか? -

- **2002 ITRSへの主変更点**
- **ITRSトレンドの変遷**
- リソグラフィ要件
- 課題
- リソグラフィ技術候補
- まとめ

ITRS 2002 の主変更点

- 昨年までに比べて変更点は非常に少ない
  - 現時点でRoadmapの安定性が向上？
- 2002 アップデートでの主変更点は;
  - リソグラフィ案件の表の見直し
    - 白・黄・赤の色の修正
  - 暫定色（横縞）の導入
  - 90nmノード（2004）のリソグラフィ技術候補からF2,イオンビーム、X線を削除
  - オーバーレイと線幅制御に関するリソグラフィとメトロロジー間での矛盾の解消を行った
  - F2におけるペリクルの課題を認識

ITRS Roadmapの変遷

Year	(nm)	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013
Technology Node Update		130			90			65			45			32
SIA 1994 Edition	Generation	180			130			100			70			50
	MPU Half Pitch	230			160			115			80			55
	Gate Length	140			100			70			50			30
SIA 1997 Edition	DRAM Half Pitch	150		130			100			70			50	
	MPU Half Pitch	180		160			115			80			55	
	Gate Length	120		100			70			50			30	
ITRS 1999 Edition	DRAM Half Pitch		130			100			70			50		
	MPU Half Pitch		160			115			80			55		
	Gate Length		85-90			65			45			30-32		
ITRS 2000 Edition	DRAM Half Pitch	130	115	100	90	80	70	65	60	50	45	40	37	33
	MPU/SoC Half Pitch	150	130	115	100	90		70			50			35
	Gate Length	80	70	60	55	50		40			28			20
ITRS2001 ITRS2002 Edition	DRAM Half Pitch	130	115	100	90	80	70	65	60	50	45	40	35	32
	MPU/SoC Half Pitch	150	130	107	90	80	70	65	60	50	45	40	35	32
	SoC Gate resist	130	107	90	75	65	53	45	40	35	32	30	25	22
	SoC Gate Length	90	75	65	53	45	37	32	30	25	22	20	18	16
	MPU Gate resist	90	75	65	53	45	40	35	32	30	25	22	20	18
	MPU Gate Length	65	53	45	37	32	28	25	22	20	18	16	15	13

リソグラフィ要件 - 概要 Near Term

Year of Production	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
	115 nm	*100 nm*	*90 nm*	*80 nm*	*70 nm*	*65 nm*
DRAM						
Half pitch (nm)	115	100	90	80	70	65
Contacts (nm)	130	115	100	90	80	70
Overlay (nm, mean + 3 sigma)	40	35	31	28	25	23
CD control for critical layers (nm, 3 sigma, post-etch, 15% of CD) litho contribution, only	11.0	10.0	9.0	8.0	7.0	7.0
MPU/ASIC						
Half pitch	130	107	90	80	70	65
Gate length (nm, in resist)	75	65	53	45	40	35
Gate length (nm, post-etch) (physical length)	53	45	37	32	28	25
Contacts (nm, in resist)	130	115	100	90	80	70
Gate CD control (nm, 3 sigma, post-etch, 10% of CD, litho only)	4.3	3.7	3.0	2.6	2.3	2.0

STRJ WS: March 4, 2003, WG5 M.Kameyama

Optical Mask Table の修正

	Year of Production	2002	2003	2004	2005	2006	2007
		115nm	100nm	90nm	80nm	70nm	65nm
Was	Mask minimum image size (nm) [C]	300	260	212	180	160	140
Is	Mask minimum image size (nm) [C]	300					
Was	Mask OPC feature size (nm) Clear [D]	230	200	180	160	140	130
Is	Mask OPC feature size (nm) Clear [D]	230					
Was	Mask OPC feature size (nm) Opaque [D]	150	130	106	90	80	70
Is	Mask OPC feature size (nm) Opaque [D]	150					
Was	Image placement (nm, multi-point) [E]	24	21	19	17	15	14
Is	Image placement (nm, multi-point) [E]						
	CD uniformity (nm, 3 sigma) [F] @						
Was	Isolated lines (MPU gates) Binary	6.1	5.1	4.2	3.7	3.4	2.5
Is	Isolated lines (MPU gates) Binary	6.1					
Was	Isolated lines (MPU gates) ALT	8.5	7.2	5.9	5.1	4.8	4
Is	Isolated lines (MPU gates) ALT	8.5					
Was	Contact/vias	6.9	6.1	5.3	4.8	4.3	3.2
Is	Contact/vias	6.9					
Was	Linearity (nm) [G]	17.5	15.2	13.7	12.2	10.6	9.9
Is	Linearity (nm) [G]	17.5					

 = interim solution

EUV Mask Table の修正

	CD Uniformity (nm, 3 sigma) [E]					
Was	Dense lines DRAM (half pitch)	11	10	7	5	3.5
Is	Dense lines DRAM (half pitch)	11	10			
Was	Linearity (nm) [F]	11	10	7	5	3.5
Is	Linearity (nm) [F]	11	10			
	EUVL-specific Mask Requirements					
Was	Mean peak reflectivity	65%	65%	66%	67%	67%
Is	Mean peak reflectivity			66%		
Was	Reflected centroid wavelength uniformity (nm 3sigma) [M]	0.06	0.05	0.05	0.04	0.03
Is	Reflected centroid wavelength uniformity (nm 3sigma) [M]					0.03

- EPL mask tablesでもLinearityに関して同様の修正。

課題: Short Term

Five difficult challenges ≥ 65 nm before 2007.	Summary of issues
Optical mask fabrication with resolution enhancement techniques and post-optical mask fabrication	• Registration, CD control, defectivity, and 157 nm films; defect free multi-layer substrates or membranes. • Equipment infrastructure (writers, inspection, repair).
Cost control and return-on-investment (ROI)	• Achieving constant/improved ratio of tool cost to throughput over time. • Cost-effective resolution enhanced optical masks and post-optical masks. • Sufficient lifetimes for the technologies,
Process control	• Processes to control gate CDs to less than 2 nm (3σ) • New and improved alignment and overlay control methods independent of technology option to < 23 nm overlay.
Resists for ArF and F_2	• Outgassing, LER, SEM induced CD changes, defects ≤ 32 nm.
CaF_2	• Yield, cost, quality.

課題: Long Term

Five difficult challenges < 65 nm beyond 2007.	Summary of issues
Mask fabrication and process control	• Defect-free NGL masks. • Equipment infrastructure (writers, inspection, repair). • Mask process control methods.
Metrology and defect inspection	• Capability for critical dimensions down to 9 nm and metrology for overlay down to 9 nm, and patterned wafer defect inspection for defects < 32 nm.
Cost control and return on investment (ROI)	• Achieving constant/improved ratio of tool cost to throughput. • Development of cost-effective post-optical masks. • Achieving ROI for industry with sufficient lifetimes for the technologies.
Gate CD control improvements; process control; resist materials	• Development of processes to control gate CDs < 1 nm (3 sigma) with appropriate line-edge roughness. • Development of new and improved alignment and overlay control methods independent of technology option to < 9 nm overlay.
Tools for mass production	• Post optical exposure tools capable of meeting requirements of the Roadmap.

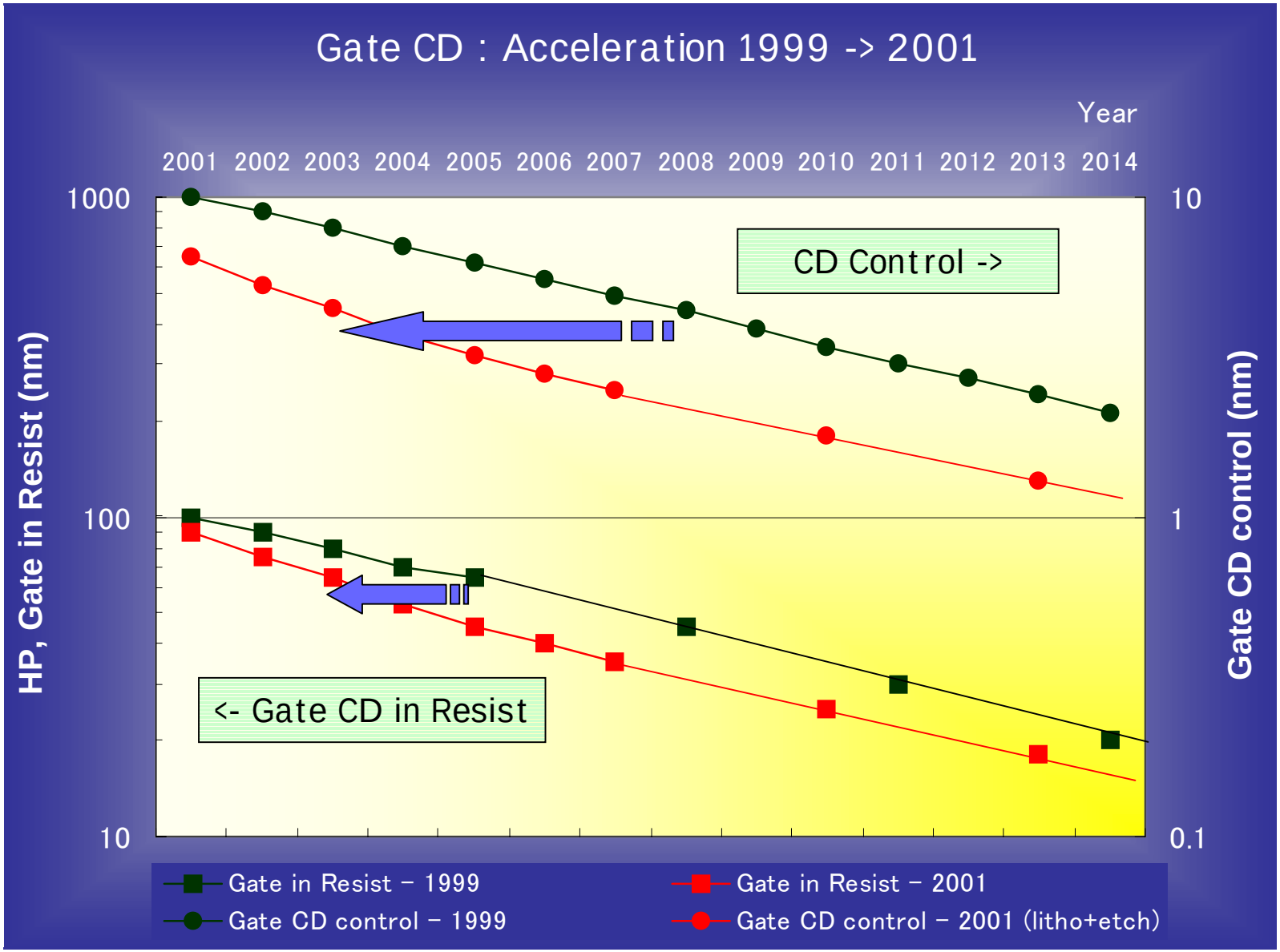
線幅制御（CD Uniformity）に関する議論

Work - In - Progress

- 今のリソグラフィで最大の課題
- CDバジェットの破綻が既に見えている
- 線幅の10%の線幅バラツキは本当に必要なのか？
- 解決法は？

ITRS1999 とITRS2001 における線幅制御の加速

!!! in Resist : 2 year acceleration but MPU gate CD uniformity " 5 years acceleration"



MPU Gate での CD uniformity Budget について

ITRS 2001-P244 *Year of Production*	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
DRAM ½ Pitch (nm)	130	115	100	90	80	70	65
MPU							
MPU gate in resist (nm)	90	75	65	53	45	40	35
MPU gate length after etch (nm)	65	53	45	37	32	28	25
Gate CD control (3 sigma) (nm) Lithography	5.3	4.3	3.7	3	2.6	2.4	2
ITRS 2001-P248							
Mask 4x Isolated lines (MPU gates) Binary	7.4	6.1	5.1	4.2	3.7	3.4	2.5
①ITRS2001でのマスクCD 均一性 (on Wafer) BM-gate on wafer (MEEF 1.4)	2.59	2.14	1.79	1.47	1.30	1.19	0.88
ITRS 2001-P246							
②ITRS2001でのレジスト相当分 (on Wafer):定義不明確？ Resist meets requirements for resolution and CD Control (nm, 3 sigma) **	7.0	6.0	5.0	5.0	4.0	4.0	3.0
③デバイス配分(仮定) *Pattern, topography (3sigma) (nm)*	4.24	3.54	2.96	2.48	2.07	1.73	1.45
④Tool分: **Gate CD control分から①, ②, ③を2乗和の考え方で引いた差分** *Lithography tool -1 (Litho - (Mask, Pattern, Topography, Resist))*	-45.5	-34.4	-23.5	-24.2	-15.1	-15.2	-7.7
⑤レジスト相当分 (on Wafer):再定義 Resist Process (3sigma) (nm)	3.0	2.5	2.0	1.7	1.4	1.1	0.9
⑥Tool分: **Gate CD control分から①, ②, ④を2乗和の考え方で引いた差分** *Lithography tool -2(Litho - (Mask, Pattern, Topography, Resist))*	-5.5	-4.4	-2.5	-1.9	-1.0	-0.4	0.5

★LithoのGate CD controlを マスク、レジスト、デバイス、露光装置の2乗和とすると 現状の数値では、成立しない

★レジスト相当分を再定義しても、露光装置への配分は無理であり、Budgetは成立していない。

STRJ WS: March 4, 2003, WG5 M.Kameyama

CD uniformity Budget 策定上の課題

■ 算出方法について

算出方法: レチクル、デバイス(パターン、トポグラフィ)、レジストプロセス、露光装置の4項の二乗和

ターゲット: 上記4項の2乗和の数値(各要素は3σ定義) が Gate after Etch寸法10％の 2/3比率配分とするならば、

- ITRSに記載された レジスト部分の定義が不明確かつ過大で、そのままでは上記計算に適用しても既に破綻
- ITRSに記述されている 計測精度(下記) のBudget 配分への適用方法は？

Wafer Metrology ITRS 2001-P399

Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
*Wafer gate CD control**	6.5	5.3	4.5	3.7	3.2	2.8	2.5
Wafer CD metrology tool precision (P/T=.2 for isolated lines**)*	1.3	1.1	0.9	0.75	0.65	0.56	0.5
Wafer CD metrology tool precision (P/T=.2 for dense lines**)*	2.6	2.3	2	1.8	1.6	1.4	1.3

Mask Metrology ITRS 2001-P402

Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
Wafer gate CD control*	6.5	5.3	4.5	3.7	3.2	3	2.5
Mask image placement metrology (precision, P/T=0.1)	2.7	2.4	2.1	1.9	1.7	1.7	1.6
Mask CD metrology tool precision* (P/T=0.2 for isolated lines, binary**)	1.8	1.5	1.3	1.1	1	0.9	0.7
Mask CD metrology tool precision* (P/T=0.2 for isolated lines, alternated**)	2.4	2.1	1.75	1.6	1.45	1.3	1.15

■ 目標数値について

算出方法: Gate after Etch 寸法から算出

- Litho の検定が レジスト像レベルであることから in Resist と after Etch の相関情報が欲しい
- Litho と etch の2/3比率配分で sqrt(2/3) 重みが適切か、2/sqrt(5)(:エラー比率で1:2) が適切か

6.5nm の配分: sqrt(2/3): Litho 5.31nm Etch 3.75nm 2/sqrt(5) : Litho 5.81nm Etch 2.91nm

ITRS2001おける Lithography と FEP(Etching)の整合性

Year of Production	2001	2002	2003	2004	2005	2006	2007	2010	2013	2016
DRAM ½ Pitch (nm)	130	115	100	90	80	70	65	45	32	22
MPU										
MPU gate in resist (nm)	90	75	65	53	45	40	35	25	18	13
MPU gate length after etch (nm)	65	53	45	37	32	28	25	18	13	9
Gate CD control (3 sigma) (nm) Lithography	5.3	4.3	3.7	3	2.6	2.4	2	1.5	1.1	0.7
After etch寸法の10%を 二乗和レベルでの効き率で Litho:2, Etch: 1 （具体的には 重み sqrt(2/3)を Lithoに) とした場合の配分										
Lithography (2/3) (3 sigma) (nm)	5.31	4.33	3.67	3.02	2.61	2.29	2.04	1.47	1.06	0.73
Etching (1/3) (3 sigma) (nm)	3.75	3.06	2.60	2.14	1.85	1.62	1.44	1.04	0.75	0.52
total (3sigma) (nm)	6.50	5.30	4.50	3.70	3.20	2.80	2.50	1.80	1.30	0.90
ITRS2001 P216 に記述されたtotal 3sigma(L_{gate}3sigma variation) と Lithography 相当分に関する記載										
Total maximum allowable lithography 3σ(nm) [D-2]	5.15	4.33	3.64	3.06	2.57	2.29	2.04	1.45	1.02	0.72
Total maximum allowable etch 3σ (nm), including photoresist trim and gate etch [D-2]	3.64	3.06	2.57	2.17	1.82	1.62	1.44	1.02	0.72	0.51
total 3sigma	6.31	5.30	4.46	3.75	3.15	2.81	2.50	1.77	1.25	0.88

ITRS 2001-P216

記載数値に一部整合性がないが、誤記の範疇

① FEP記述において，130nmノードでの Gate CD control (10%定義）と異なる

② Litho記述において，DRAM HP 70nmでの Gate CD controlの数値が定義と一致しない

STRJ WS: March 4, 2003, WG5 M.Kameyama

線幅制御：リソグラフィとエッチングの取り合い

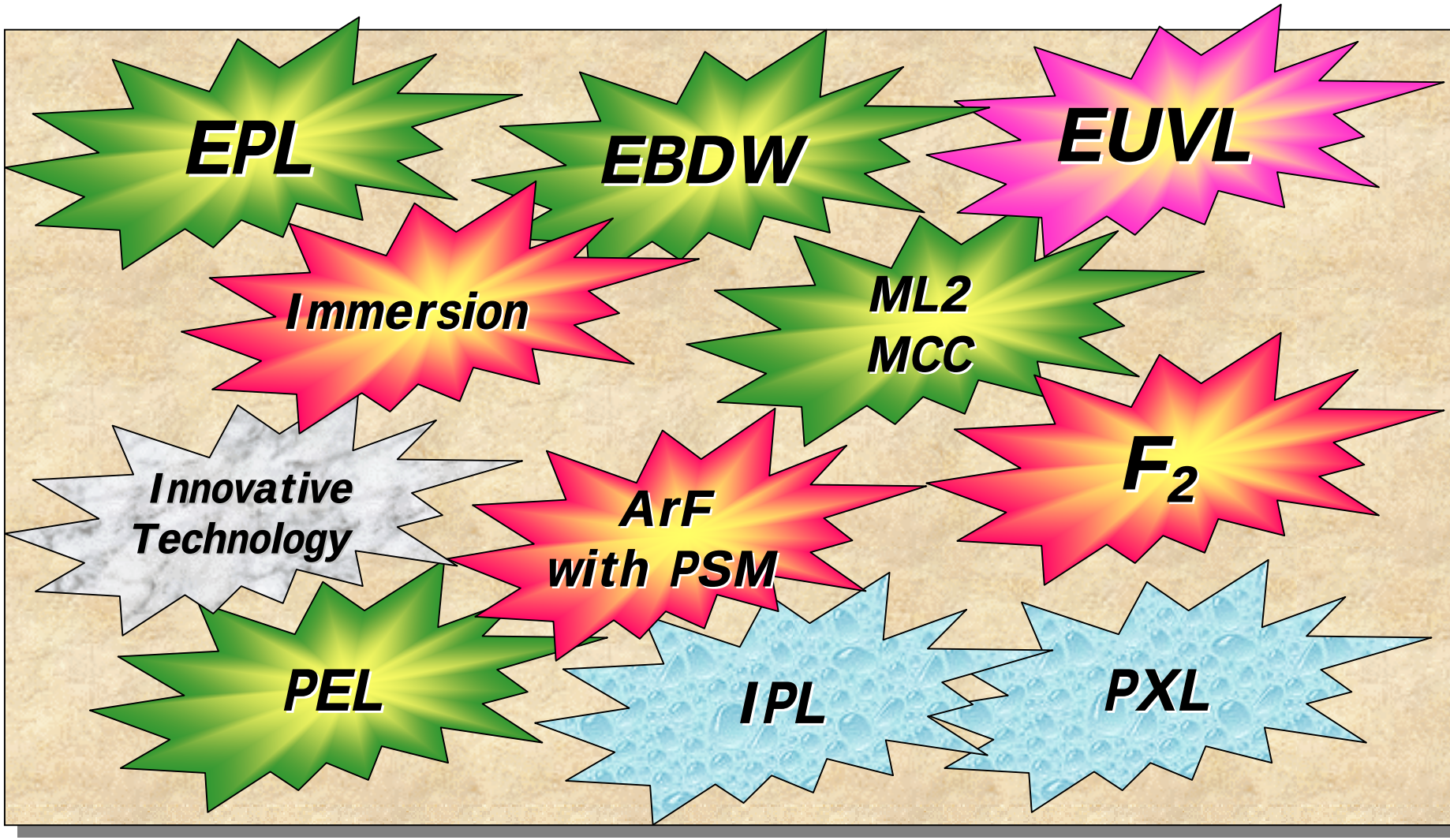
仮定

リソグラフィ２：エッチング １　→　リソグラフィ４：エッチング １

Year of Production	*2001*	*2002*	*2003*	*2004*	*2005*	*2006*	*2007*
MPU gate length after etch (nm)	65	53	45	37	32	28	25
Gate CD control (3 sigma) (nm) Lithography	5.8	4.7	4.0	3.3	2.9	2.5	2.2
Total maximum allowable etch 3s (nm), including photoresist trim and gate etch [D-2]	2.9	2.4	2.0	1.7	1.4	1.3	1.1

- リソグラフィとエッチングの取り合いを変更してもリソグラフィの線幅制御性はすぐに破綻する。
- ゲートの線幅制御の見直しは必須である。

次の本命は何か? そして間に合うか?



新顔、液浸リソグラフィ（Immersion）

解像度 ∝ λ／NA,　　NAの定義 ＝ n･sinθ　（nは 媒質屈折率）

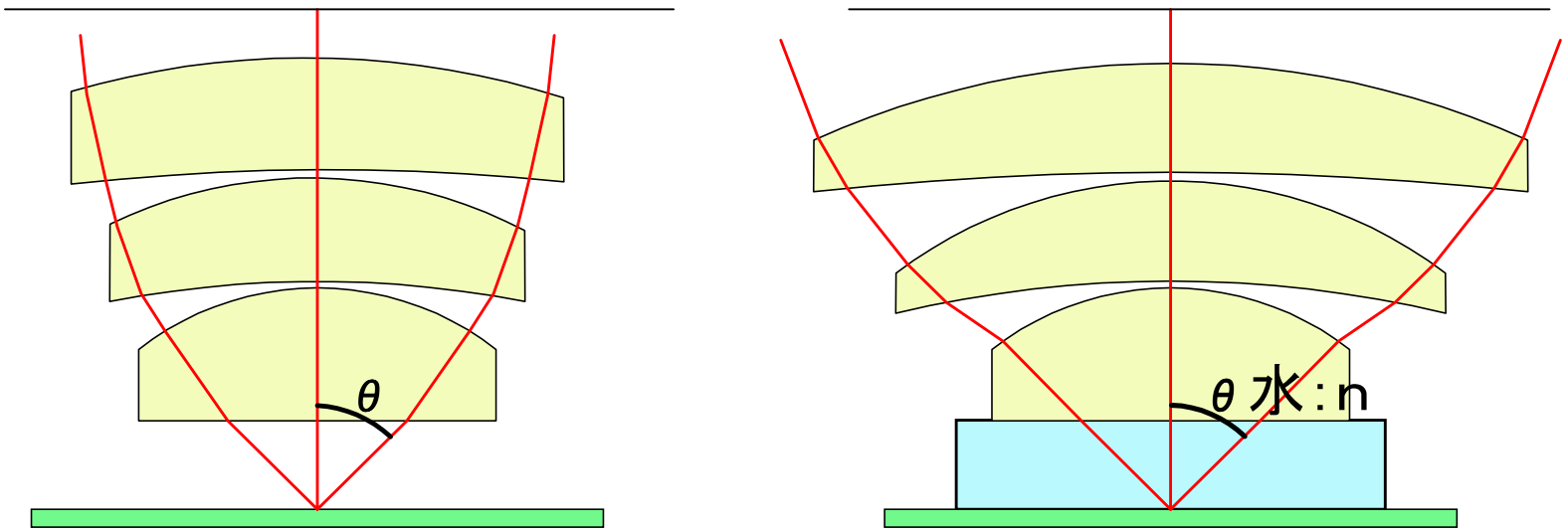
（ 解像度∝λ／sinθ とするなら、液浸の効果は λ → λ／n による 波長の縮小 ）

ドライ光学系：NA = sinθ

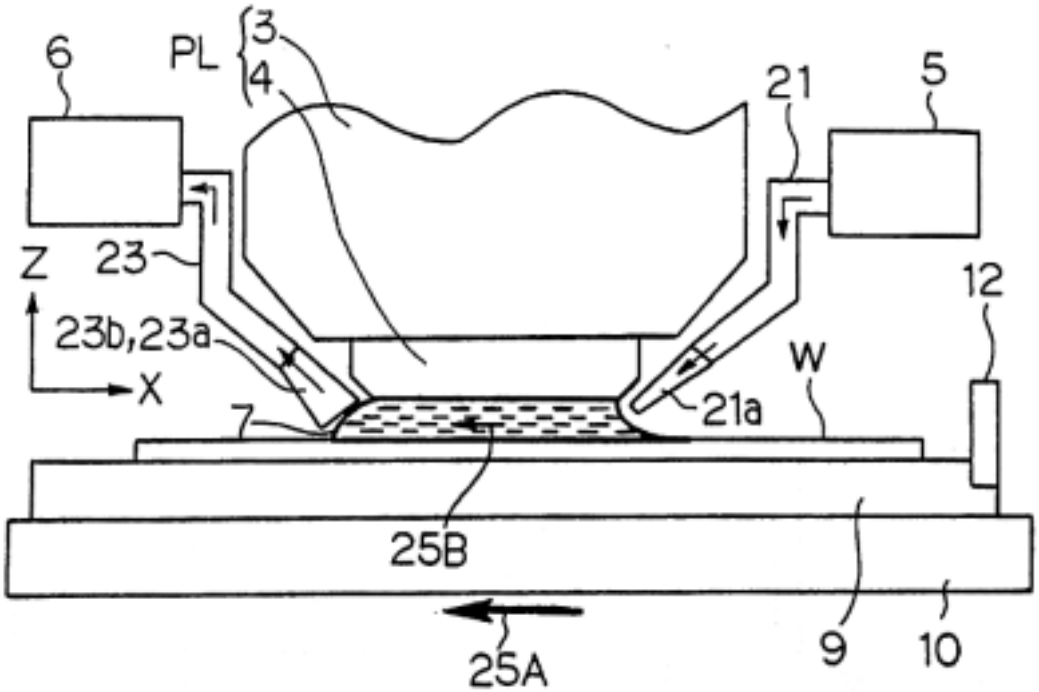
液浸光学系：NA = n･sinθ

ArF+水 では、NAが n=1.45倍 増大

ただし レンズサイズは増大！



液浸リソグラフィの優位点



NA = n sin θ

Resolution = k1 λ / NA
= k1 λ / (n sin θ)
= k1 (λ/n) / sin θ

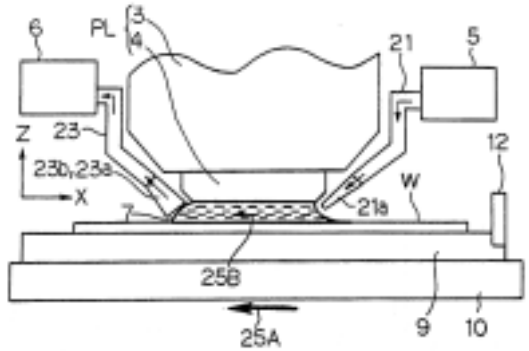
DOF = k2 (λ/n) / 2 (1-cos θ)
= k2 (λ/n) / 4 sin² (θ/2)
~ k2 (λ/n) / sin² θ
= k2 n λ / NA²

Exact DOF should be obtained by ED-tree simulation.

液浸の機構

Local immersion = local fill

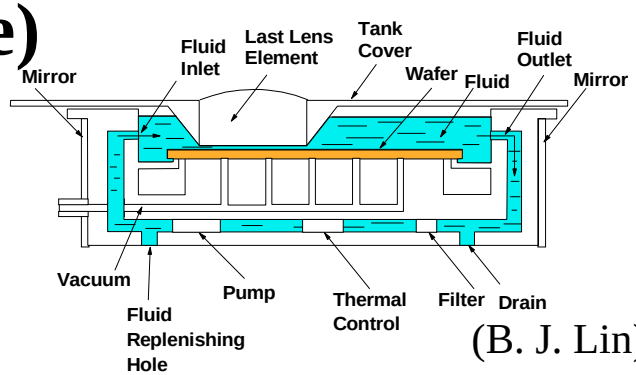
Adv: Minimum change from "dry"



Wafer immersion = moving pool (stage)

Adv: Uniform immersion condition for the whole wafer surface

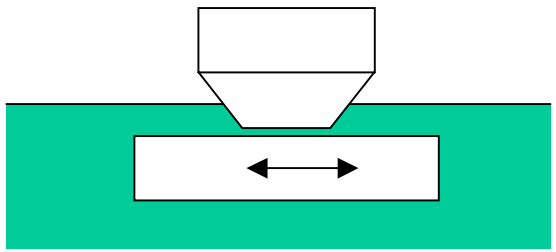
Disadvantage: Stage motion affected by liquid.



(B. J. Lin)

Stage immersion = "swimming stage"

Disadvantage: Too big a change.

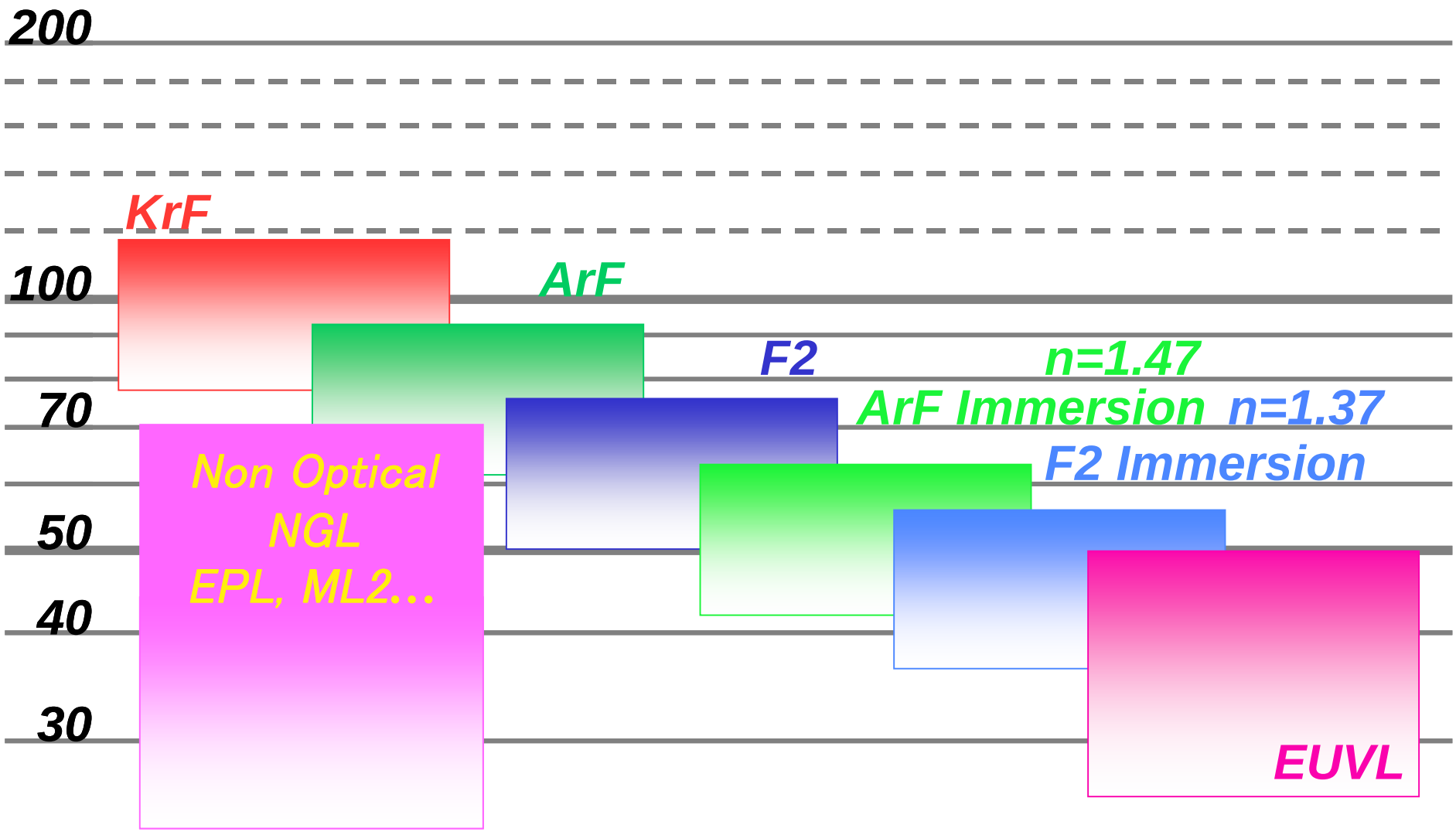


液浸における実効波長 (λ/n)
(Potential advantage)

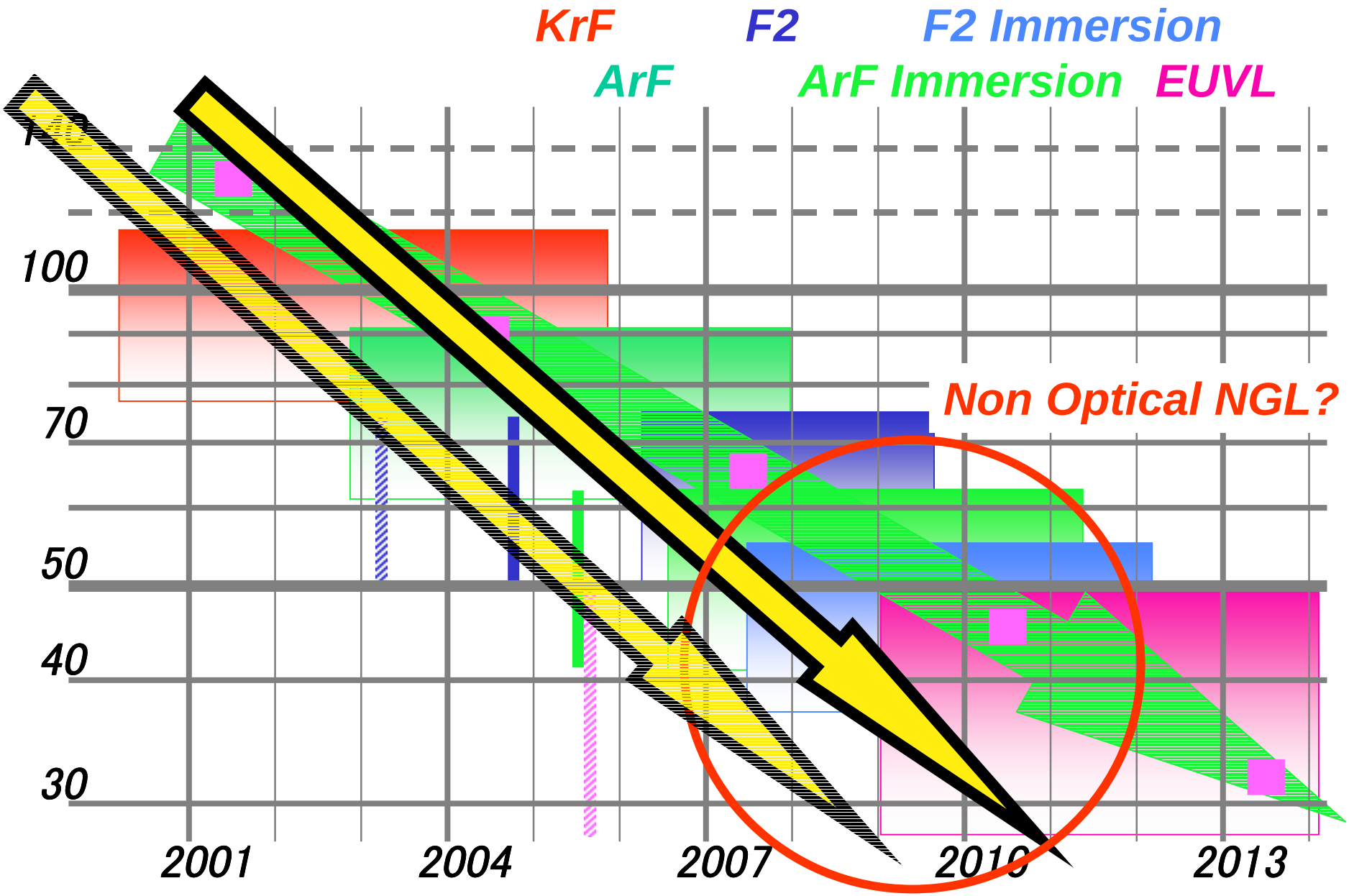
	medium	n	λ/n	ratio
193nm dry	Air	1.0	193nm	1.00
248nm immersion	H_2O	1.36	182nm	0.94
157nm dry	N_2	1.0	157nm	0.81
193nm immersion	H_2O	1.47	131nm	0.68
157nm immersion	PFPE	1.37	115nm	0.60

193nm immersion can be considered as 131nm lithography;
157nm immersion can be considered as 115nm lithography.

光の限界とNGL


200
100
70
50
40
30
KrF
ArF
F2
n=1.47
ArF Immersion n=1.37
F2 Immersion
Non Optical
NGL
EPL, ML2…
EUVL

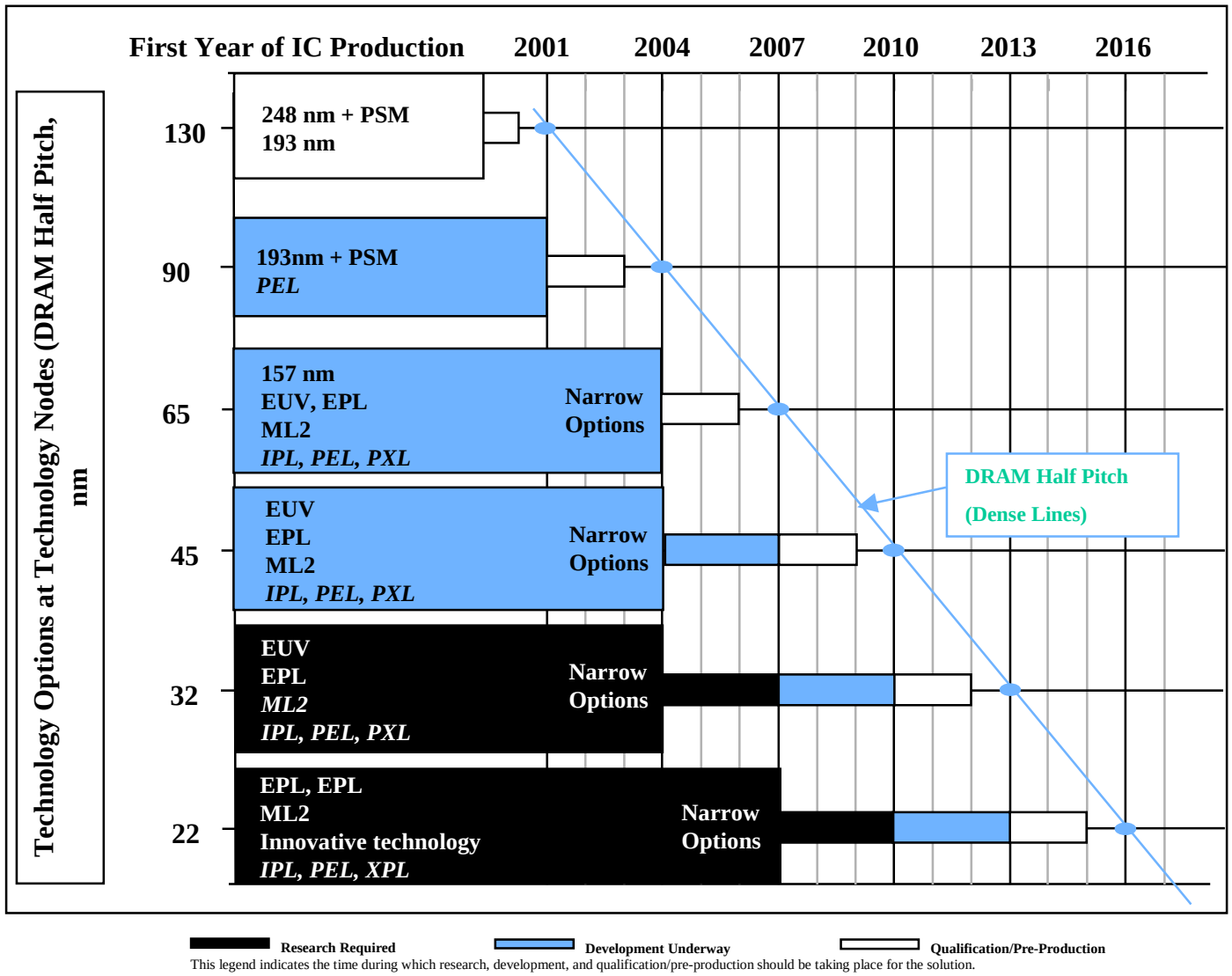
NGL、時間との戦い


KrF
F2
F2 Immersion
ArF
ArF Immersion
EUVL
100
70
50
40
30
2001
2004
2007
2010
2013
Non Optical NGL?

2 Year と 3 Year Cycle

- **2 year Cycle**
  - 難易度も高く高価なリソグラフィとなる。
  - 45nmノード達成のためEUVL或いは他のNGLの加速が必要。
  - 光の延命が必須であるが、装置導入の時期はその限界性能で始まる。 性能向上の余地は理論的に無く、すぐに次の波長に移る必要がある。
- **3 Year Cycle**
  - それでも難易度はまだ高いが、現実性はある。
  - 3年サイクルをとっても、波長ごとの寿命は極めて短い。
- **Issues**
  - マスクの可能性
  - 投資と回収

リソグラフィ技術候補



EUV = extreme ultraviolet

EPL = electron projection lithography

ML2 = maskless lithography

IPL = ion projection lithography

PXL = proximity x-ray lithography

PEL = proximity electron lithography

Technologies shown in italics have only single region support

ITRS Roadmapの変遷

Year	(nm)	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013
Technology Node Update		130			90			65			45			32
SIA 1994 Edition	Generation	180			130			100			70			50
	MPU Half Pitch	230			160			115			80			55
	Gate Length	140			100			70			50			30
SIA 1997 Edition	DRAM Half Pitch	150		130			100			70			50	
	MPU Half Pitch	180		160			115			80			55	
	Gate Length	120		100			70			50			30	
ITRS 1999 Edition	DRAM Half Pitch		130			100			70			50		
	MPU Half Pitch		160			115			80			55		
	Gate Length		85-90			65			45			30-32		
ITRS 2000 Edition	DRAM Half Pitch	130	115	100	90	80	70	65	60	50	45	40	37	33
	MPU/SoC Half Pitch	150	130	115	100	90		70			50			35
	Gate Length	80	70	60	55	50		40			28			20
ITRS2001 ITRS2002 Edition	DRAM Half Pitch	130	115	100	90	80	70	65	60	50	45	40	35	32
	MPU/SoC Half Pitch	150	130	107	90	80	70	65	60	50	45	40	35	32
	SoC Gate resist	130	107	90	75	65	53	45	40	35	32	30	25	22
	SoC Gate Length	90	75	65	53	45	37	32	30	25	22	20	18	16
	MPU Gate resist	90	75	65	53	45	40	35	32	30	25	22	20	18
	MPU Gate Length	65	53	45	37	32	28	25	22	20	18	16	15	13

まとめ

- ITRS 2001　ITRS2002への変更は最小
- ゲート線幅制御が限界に近づく
  - 定義の変更を含め議論を継続
  - マスクCD制御に厳しい要求
- 90nmのリソグラフィ技術候補は実質的に光の延長
  - 議論は65nmのリソグラフィ技術候補の選択へ

今後の課題

- 線幅制御の見直しを行なう
  - 線幅制御のモデルも考慮する
    - LERとレンズフレアーについても定義する
  - エッチングとリソグラフィ間のBudgetの取り合いも見直す
- Half-pitchの値の見直し
  - リソグラフィにとってHalf-pitchの定義は基本
- ２年/３年サイクルの議論
- LERの定義を明確化
- リソグラフィ技術候補の絞込み