MOSFETの特性ばらつき予測とコンパクトモデルの役割

STRJ-Workshop

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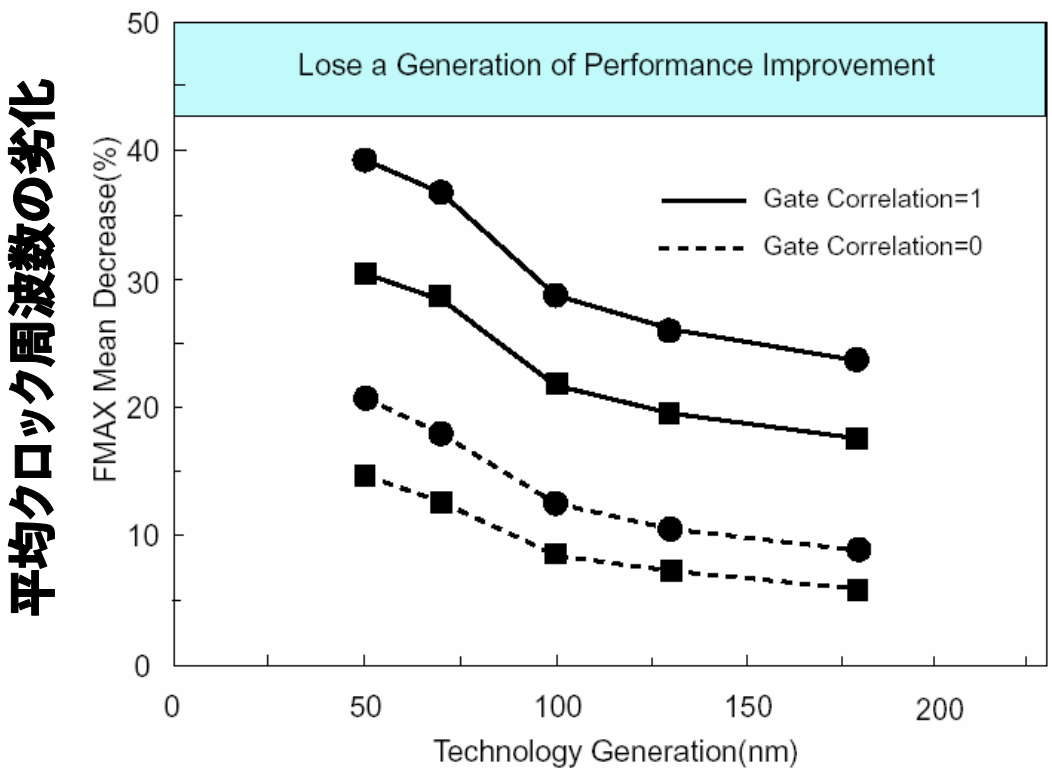
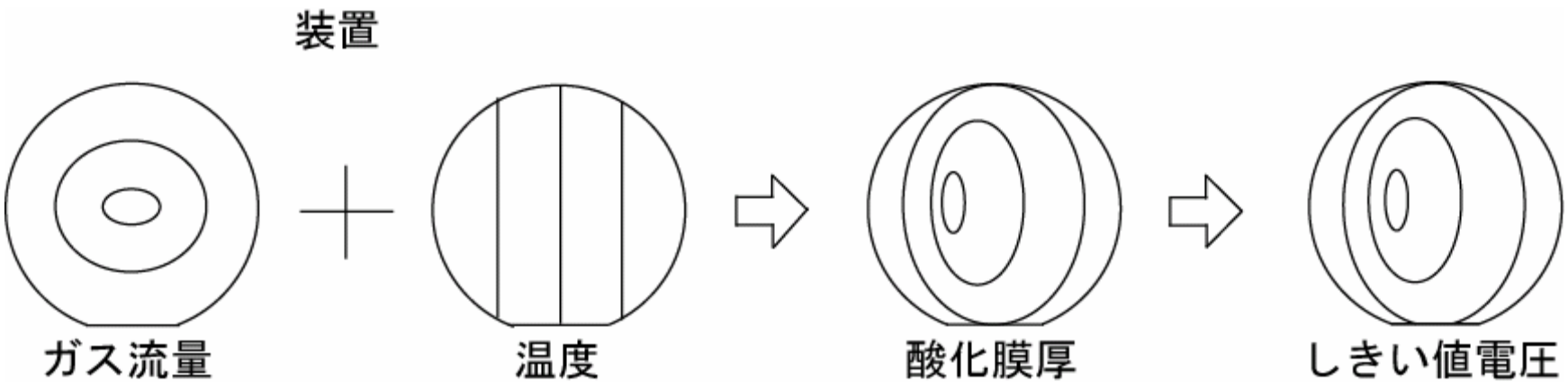
- **Intra-Chip (Die)ばらつき：** Random ⇨ Mismatch

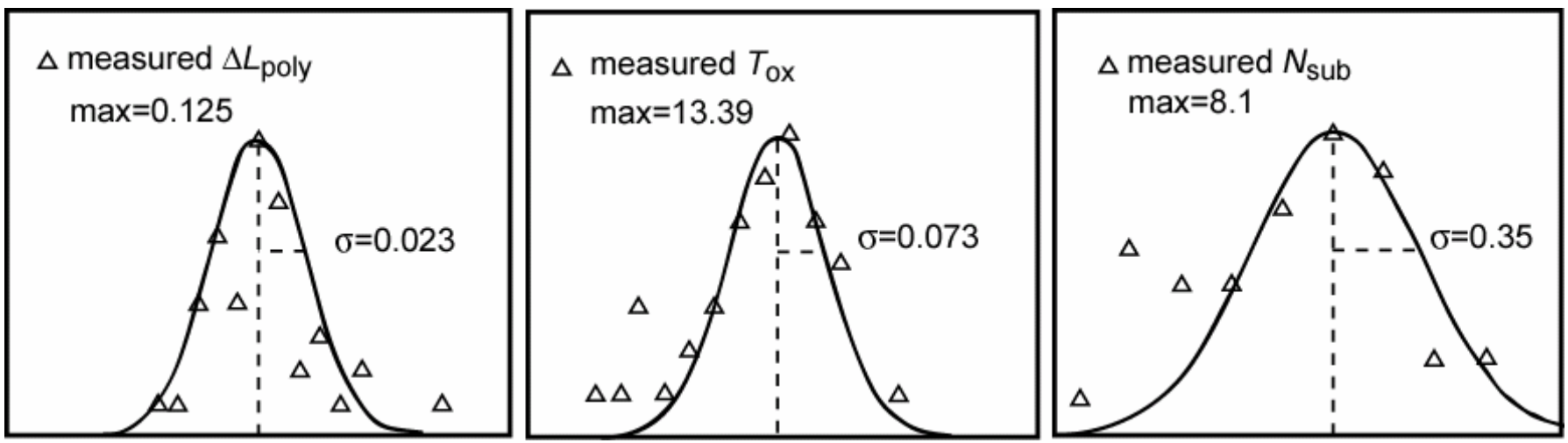


K. A. Bowman et al., IEEE J. SSC, 37, 183, 2002.

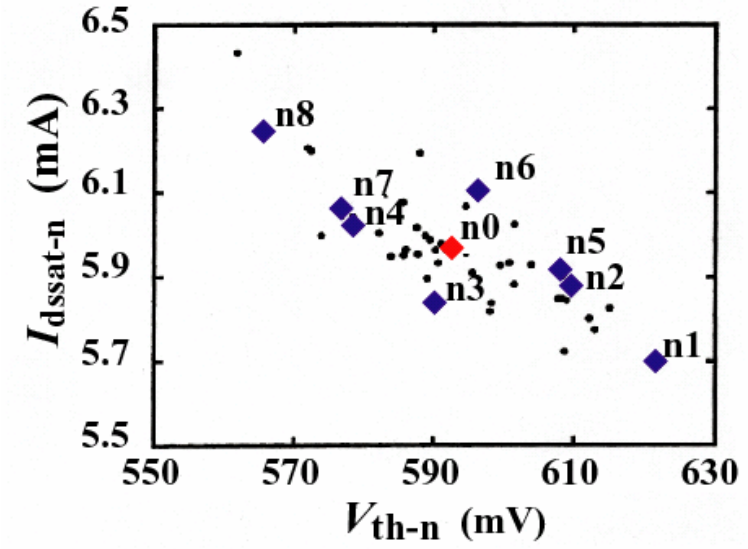
Inter-Chipばらつき

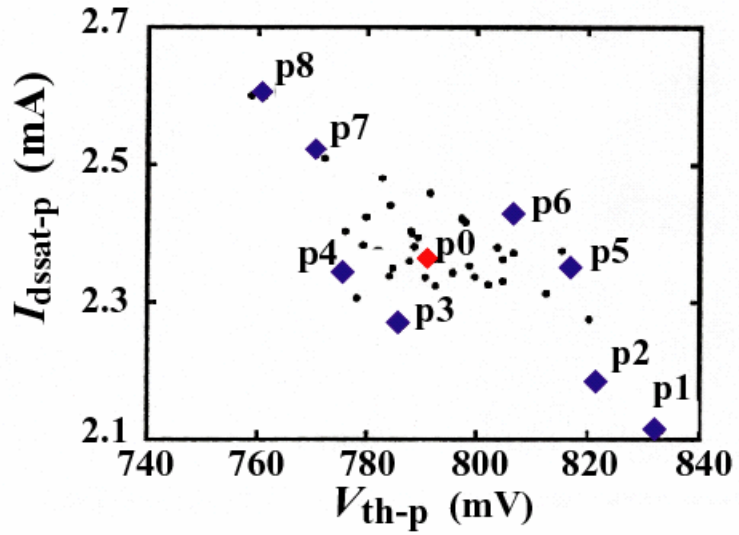


Wafer上のばらつき：In-Line測定からの抽出



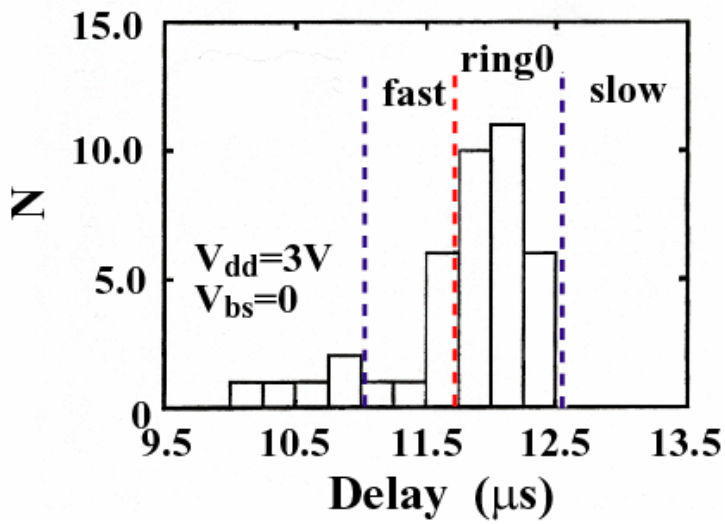
デバイスレベルのばらつき





回路レベルのばらつき

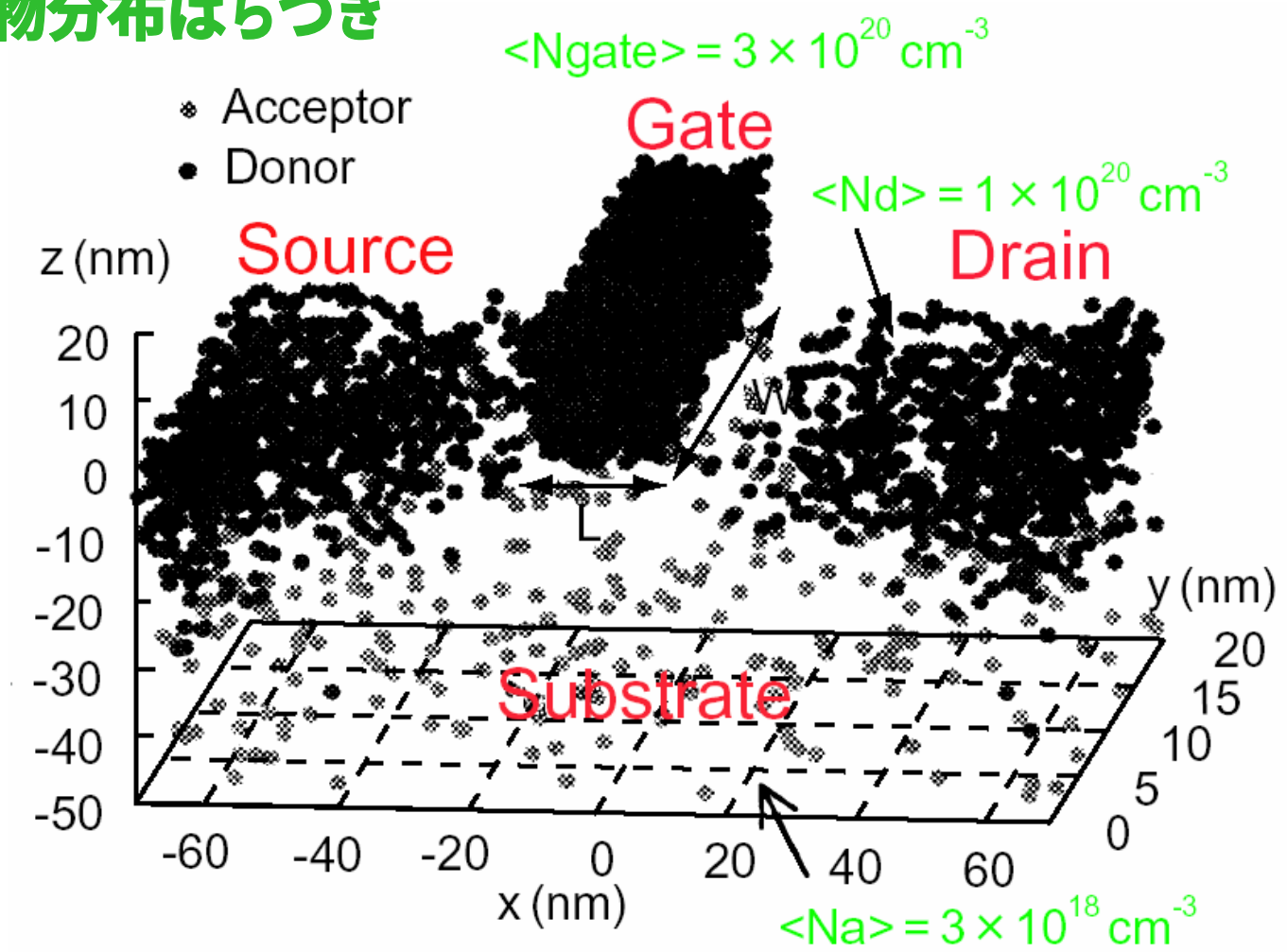
	ΔL	$\Delta N_{sub,n}$	$\Delta N_{sub,p}$	ΔT_{ox}
1	2σ	2σ	-2σ	2σ
2	2σ	2σ	-2σ	-2σ
3	2σ	-2σ	2σ	2σ
4	2σ	-2σ	2σ	-2σ
5	-2σ	2σ	-2σ	2σ
6	-2σ	2σ	-2σ	-2σ
7	-2σ	-2σ	2σ	2σ
8	-2σ	-2σ	2σ	-2σ



O. Prigge et al., IEICE, E82-C, p. 9107, 1999.

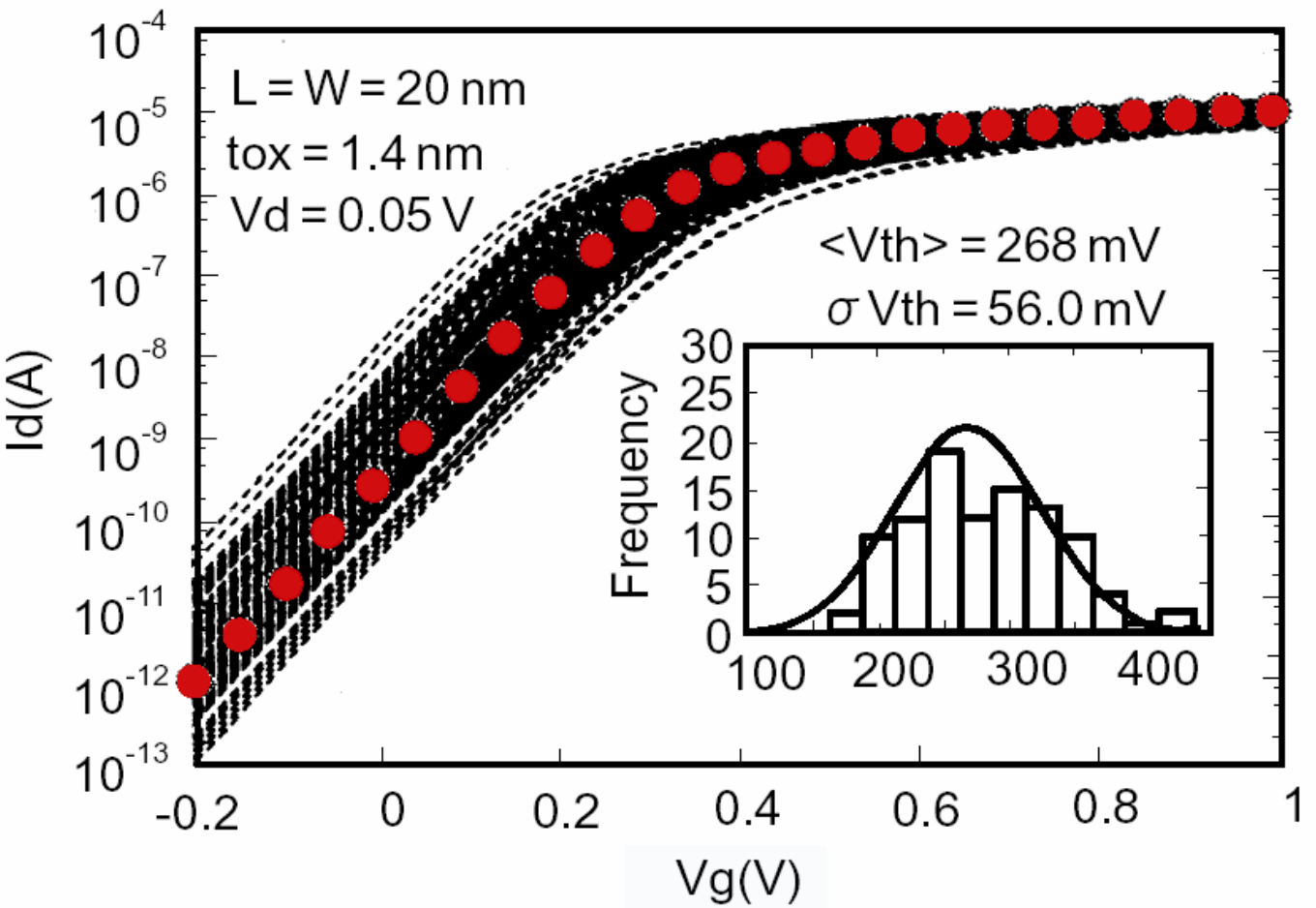
Intra-Chipばらつき

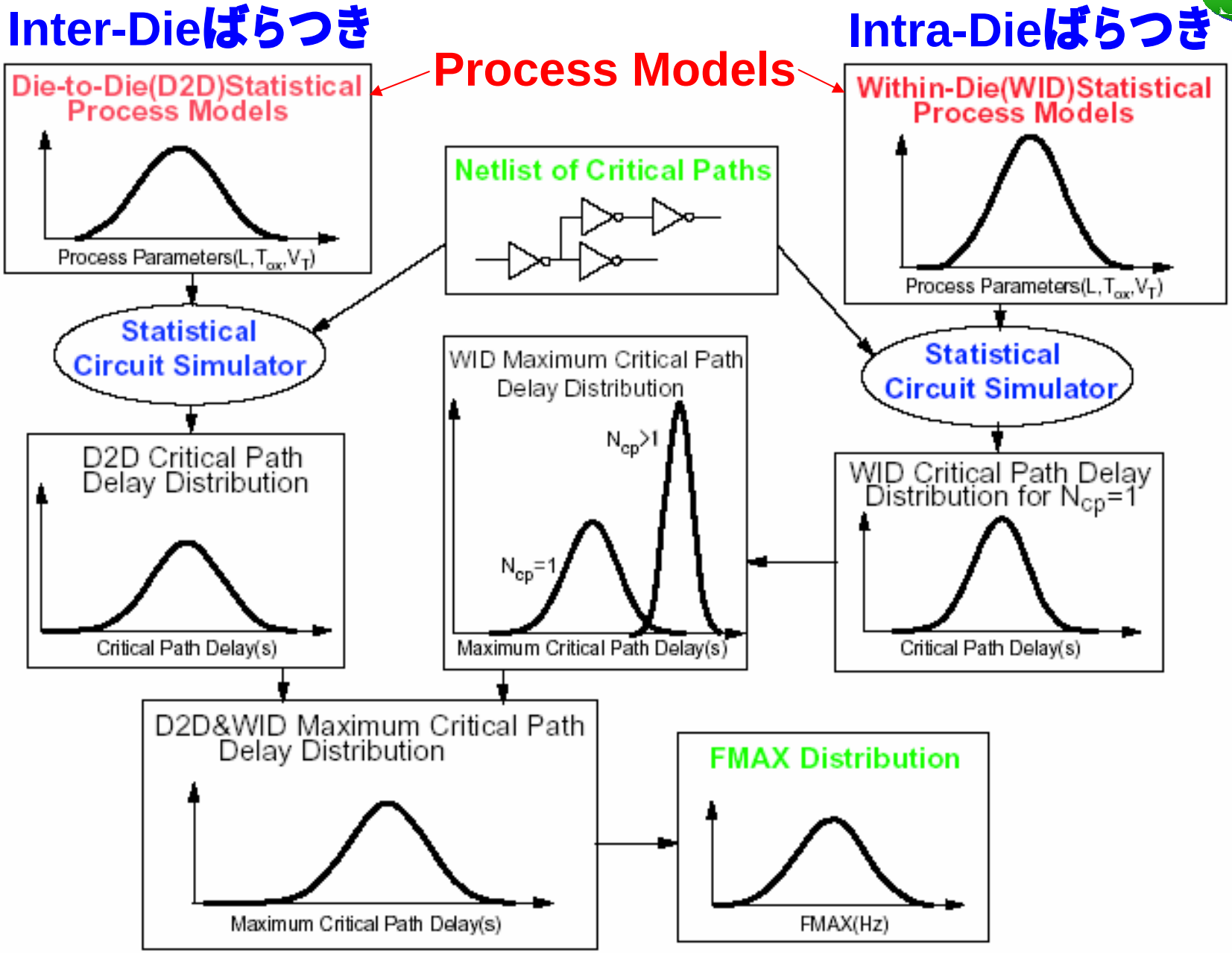
不純物分布ばらつき



S. Toriyama et al., Proc. SISPAD, 23, 2005.

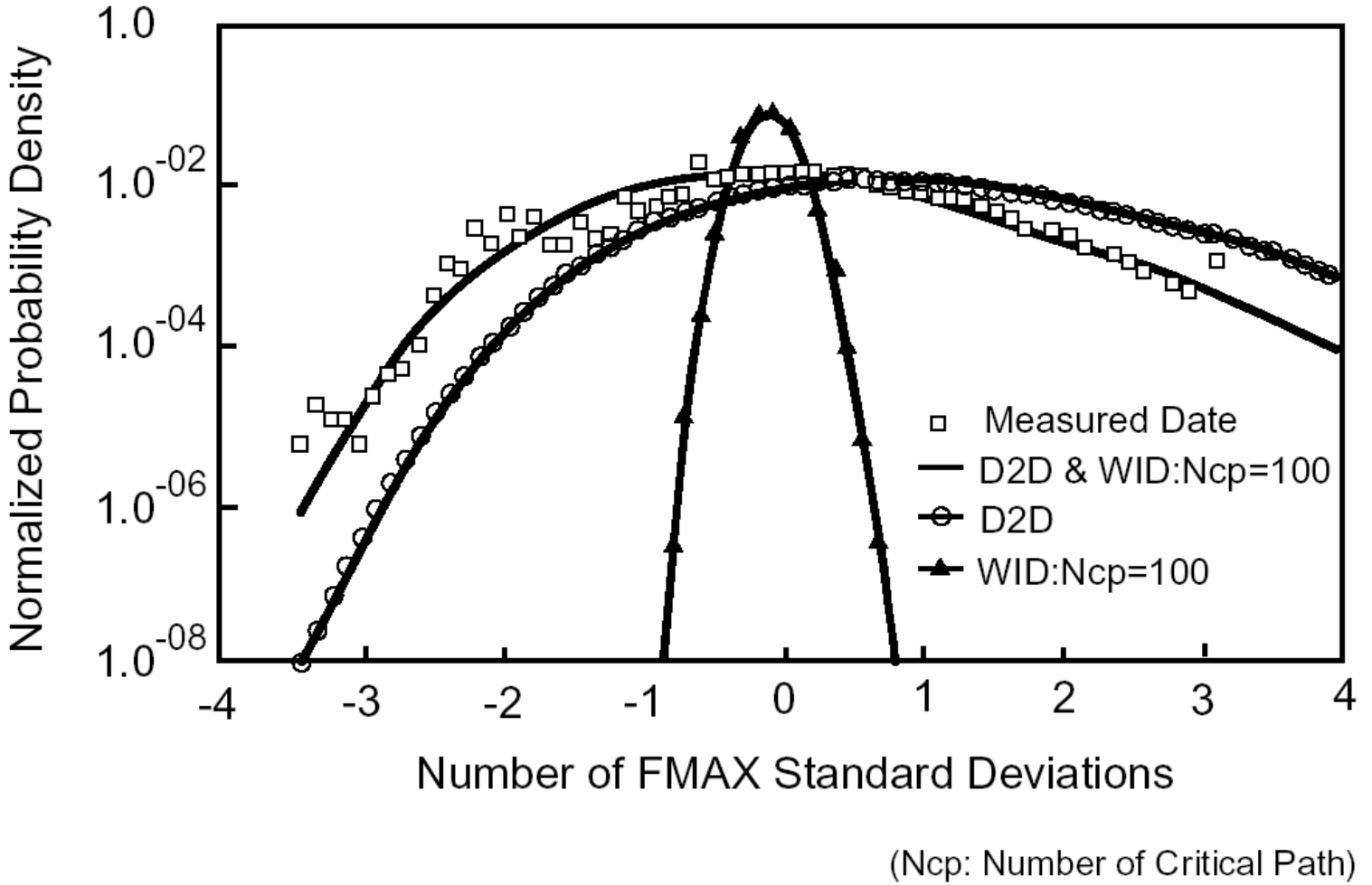
不純物ばらつきによって生じた電流ばらつき





K. A. Bowman et al., IEEE J. SSC, 37, 183, 2002.

不十分な特性（critical path)が回路全体の性能を損なう



性能ばらつきはInter-Dieばらつきと Intra-Dieばらつきから決まる

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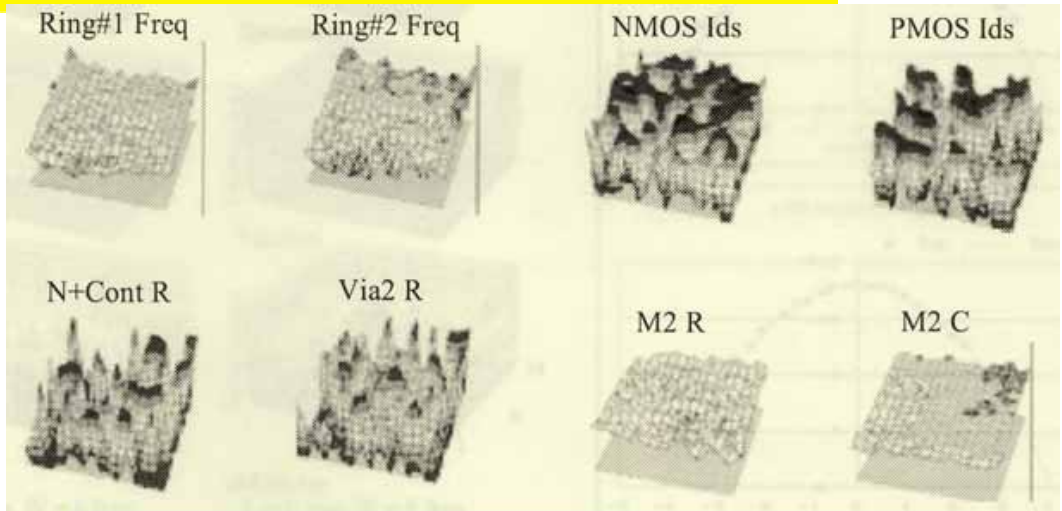
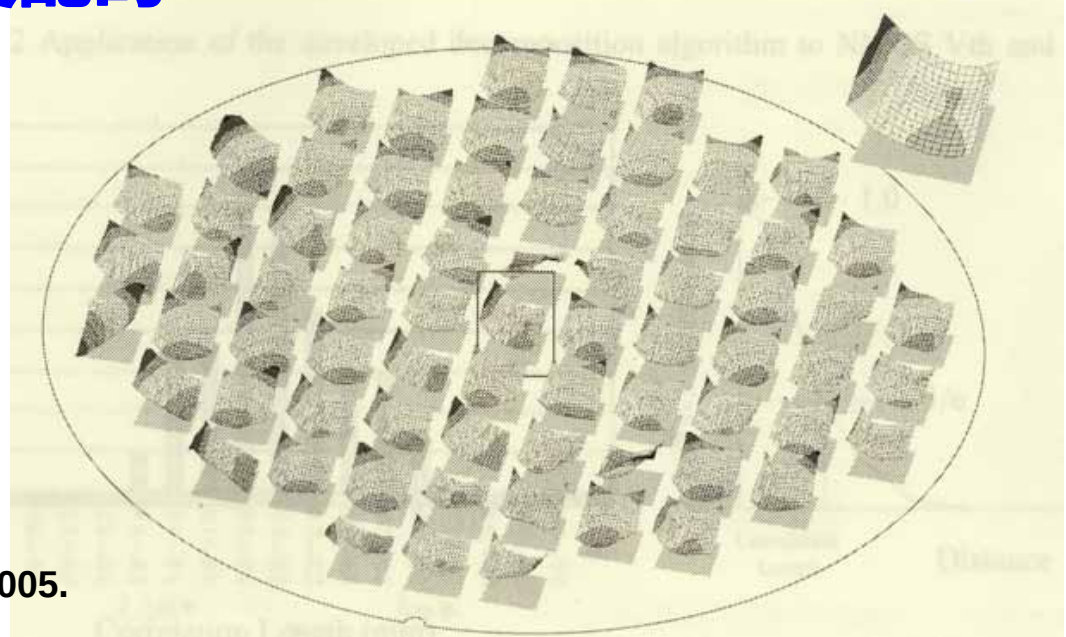
Stochasticな考察

I-2. ばらつきの見積もり

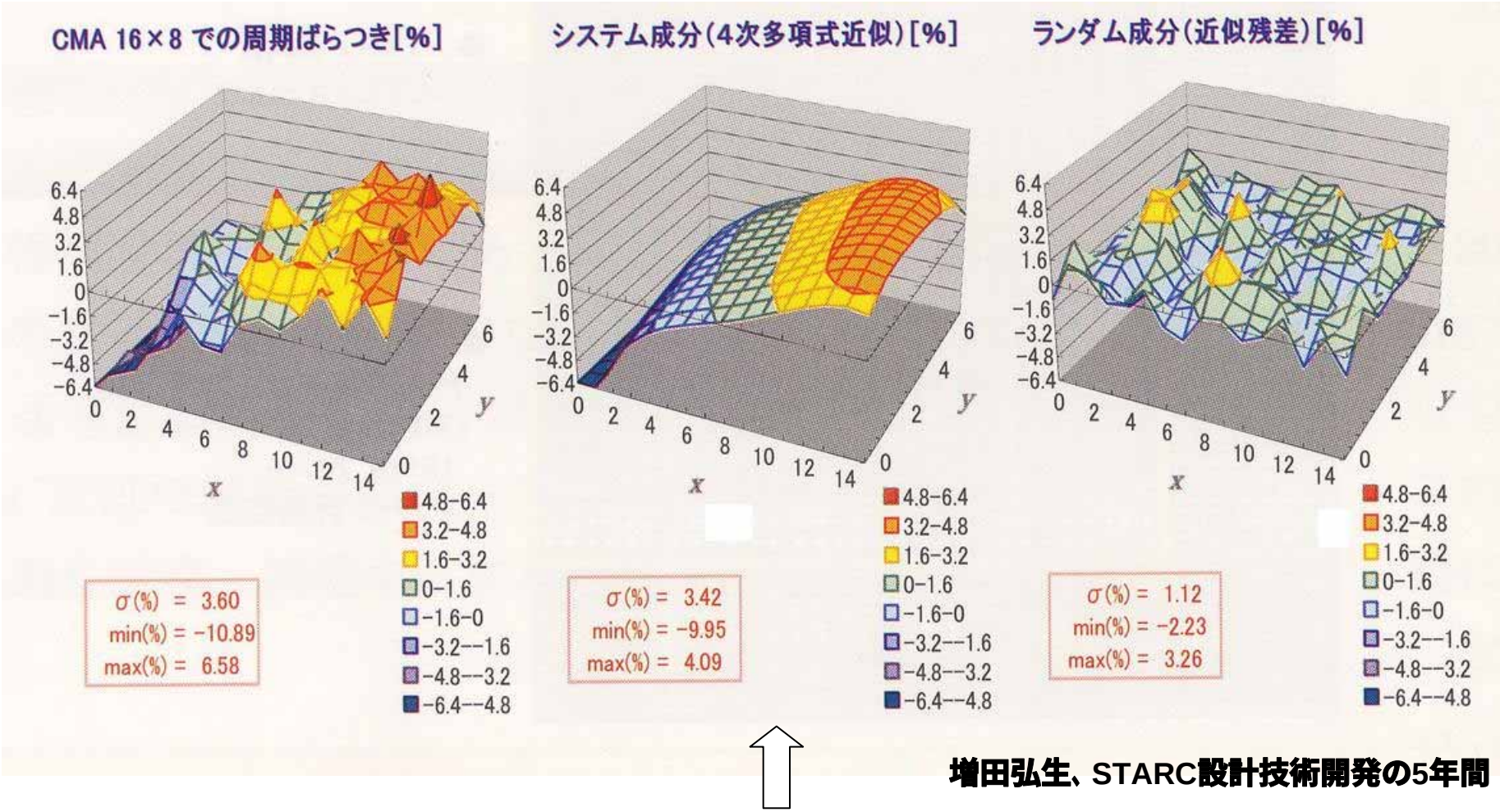


MOSFETばらつきが支配的



H. Masuda et al., CICC, p. 593, 2005.

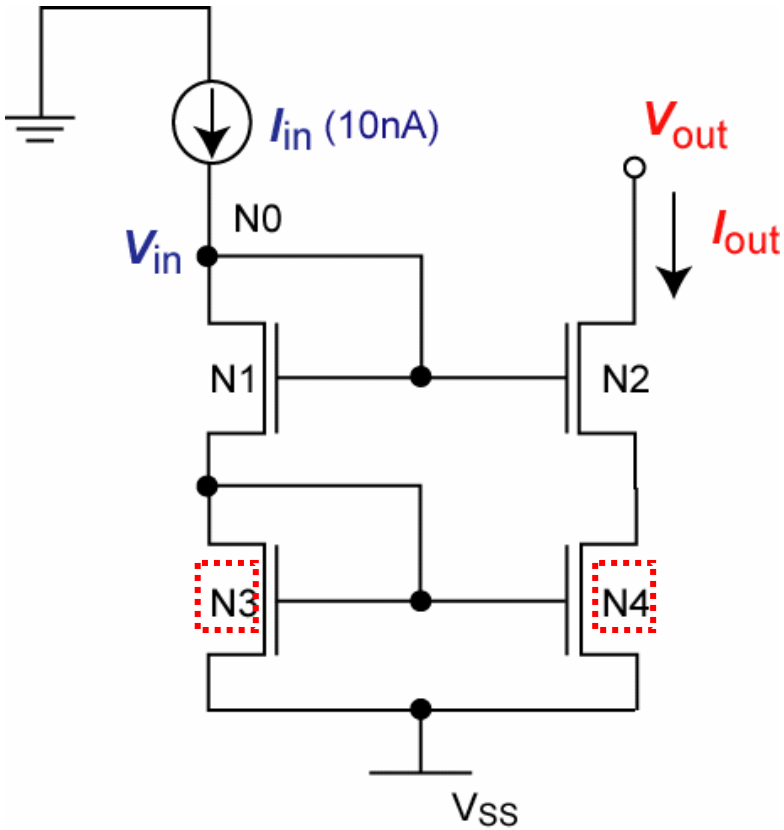
SystematicばらつきとRandomばらつきの分離

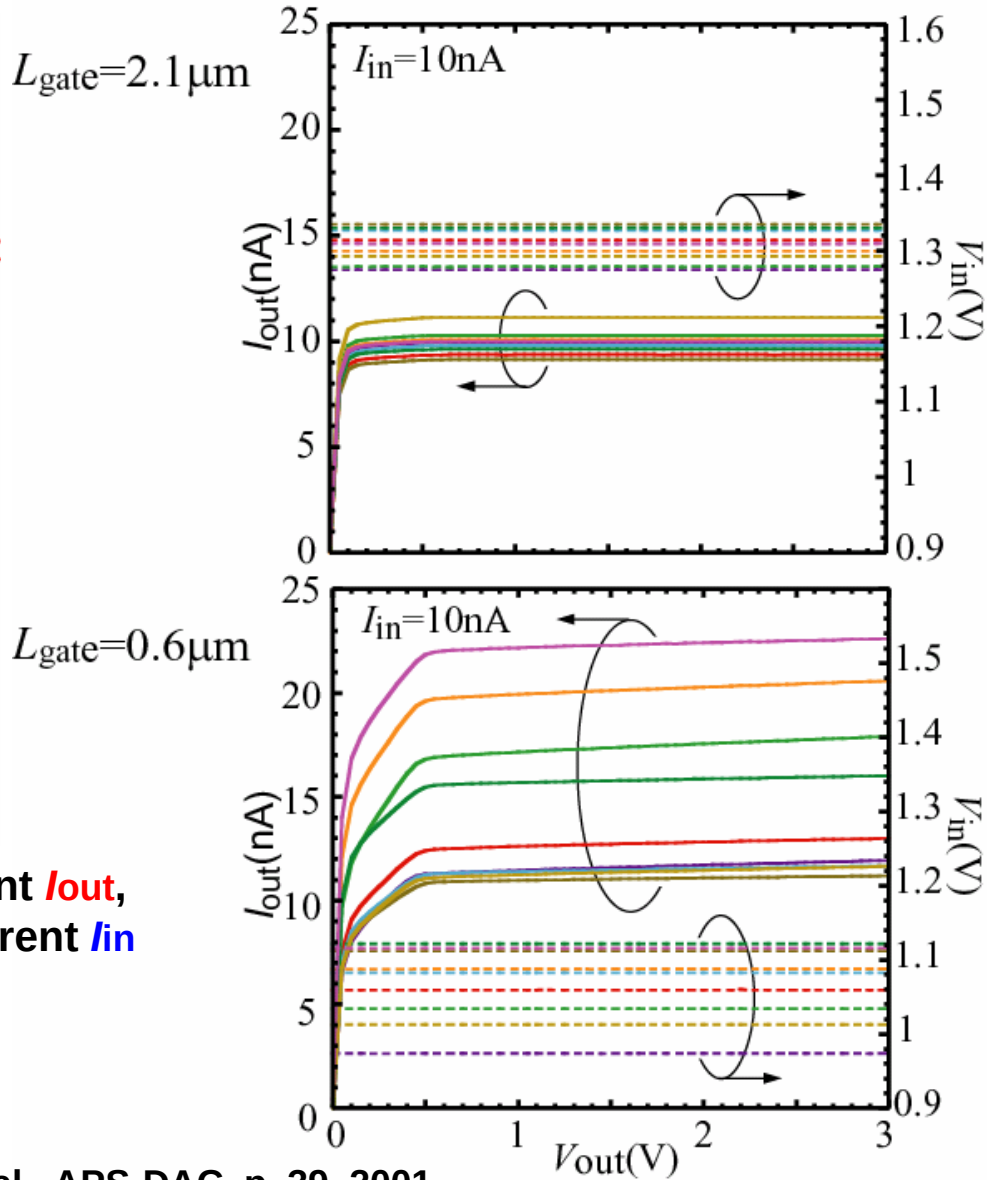


増田弘生、STARC設計技術開発の5年間

4次のpolynomial function近似

回路を用いた抽出：Cascode-Current Source





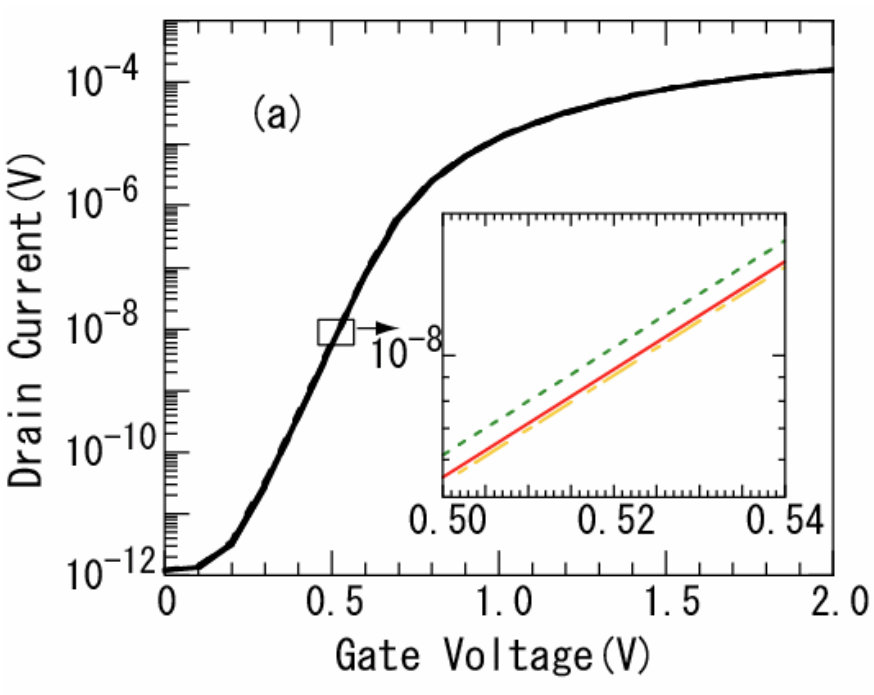
Function: to provide a constant current *I*out, which is proportional to the given current *I*in and independent of *V*out.

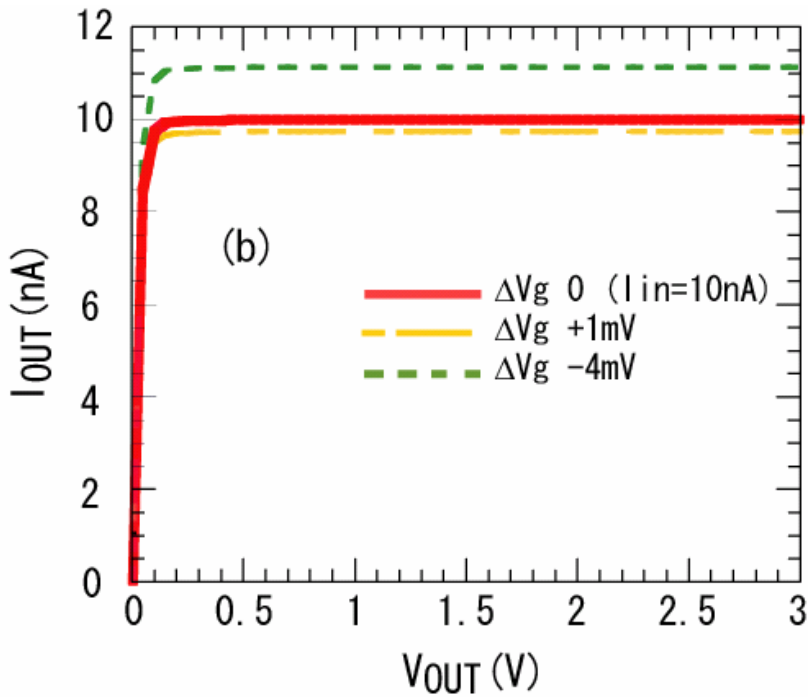
***I*in=10nA: technology variationが顕著**
resistanceなどの効果が抑圧

D. Miyawaki et al., APS-DAC, p. 39, 2001.

I_{out}のばらつきはN3とN4のmismatchが原因

N3 is fixed and N4 is varied.





I_{out}のばらつきを用いてΔV_gのMismatchを見積もることができる

簡単な見積もり方法

V_{in}のばらつきはN1とN3のばらつきの和が原因

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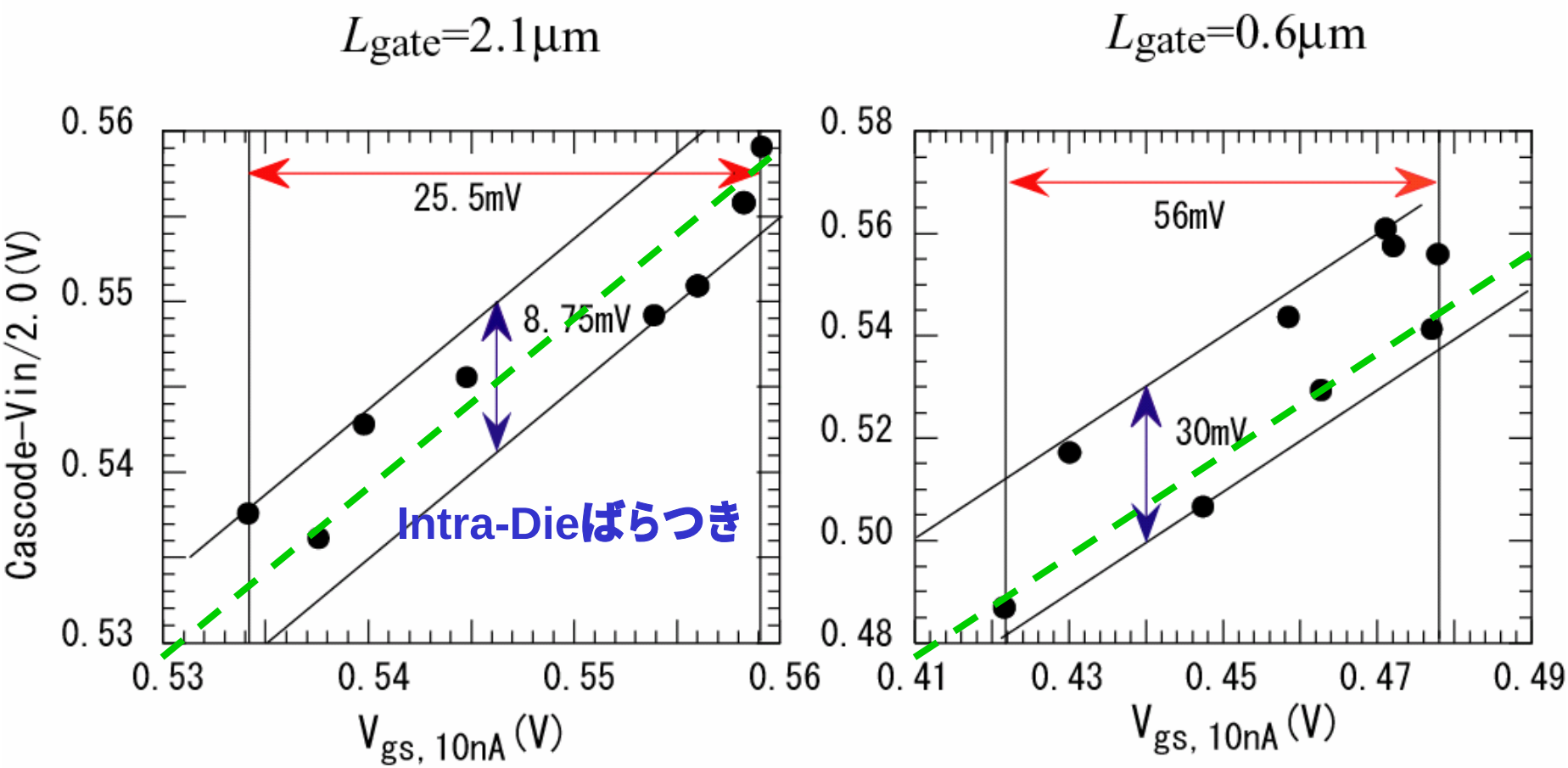
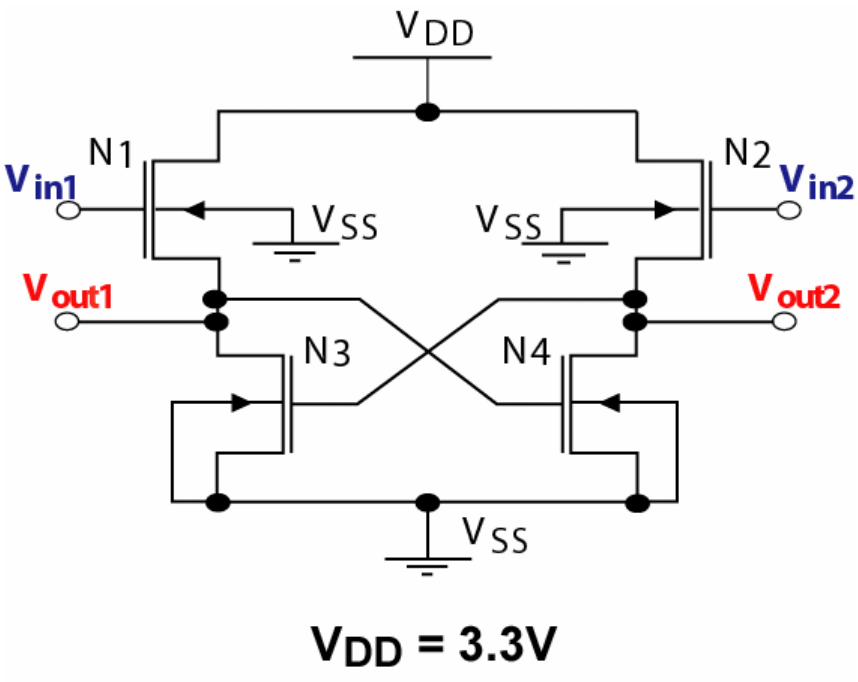
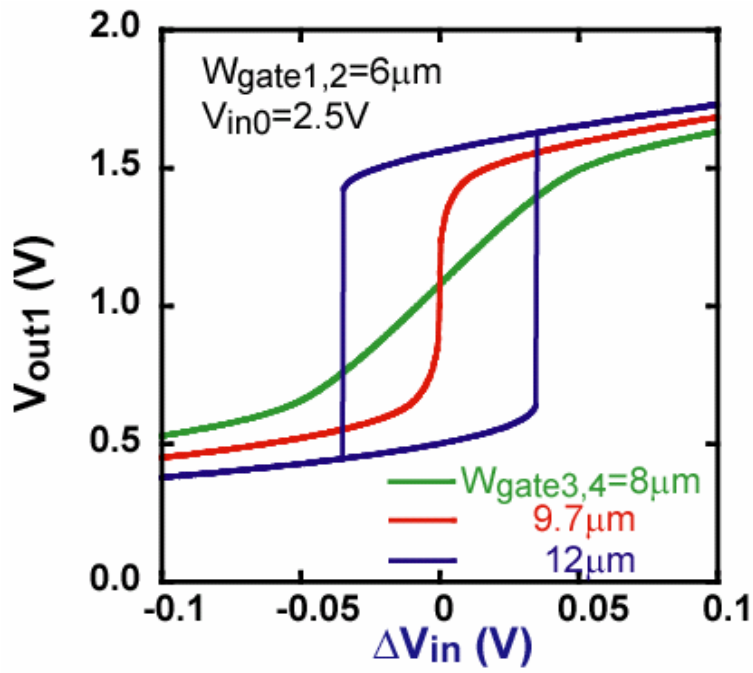
Vin/2: Inter-Dieばらつきと仮定

Vgs,10nA: 単体MOSFETのInter-Dieばらつき



Differential-Amplifier-Stage with Feed-back Coupling





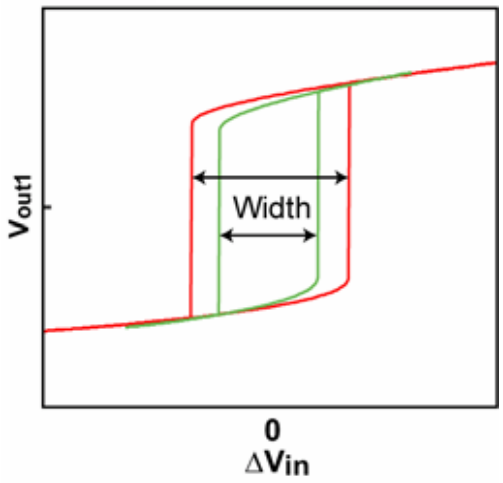
Function: to amplify *Vin* to *Vout*.

ΔVin= Vin1-Vin2

チャネル幅によってHysteresisが現れる

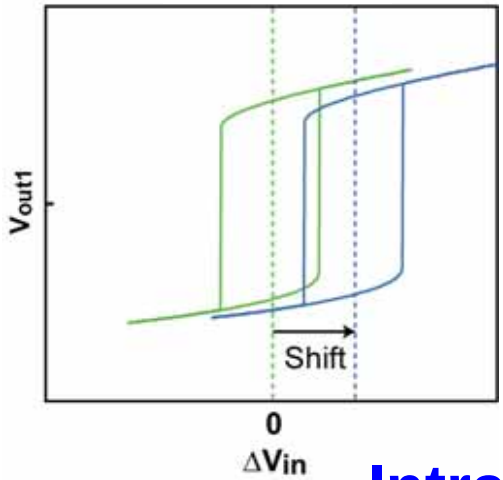
S. Matsumoto et al., CICC, p. 357, 2001.

4個のトランジスタ全部が同じように変化する場合

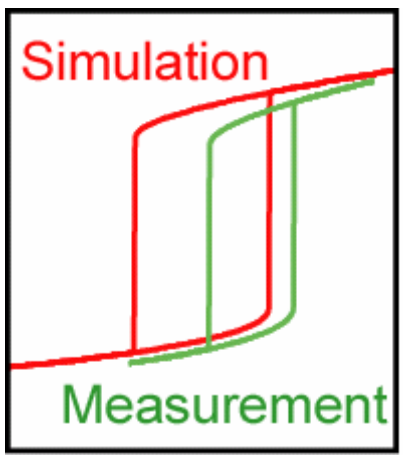


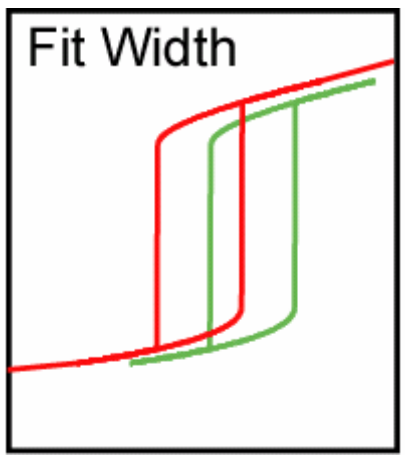
Inter-Dieばらつき

4個のトランジスタが別々に変化する場合

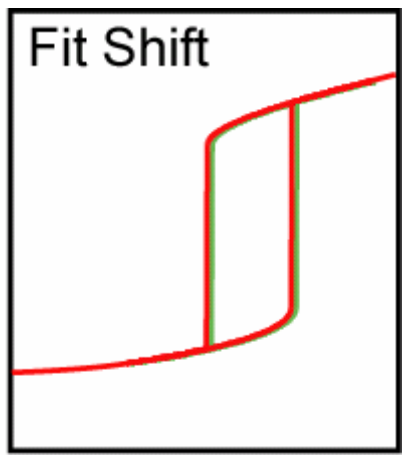


Intra-Dieばらつき





Inter-Dieばらつき抽出



Intra-Dieばらつき抽出

ばらつき見積もり結果

Cascode-Current Source

	ΔN_{sub}	$\Delta L_{gate}/0.6\mu m$
Inter	7%	6.7%
Intra	1%	3.8%

Differential-Amplifier-Stage with Feed-Back-Coupling

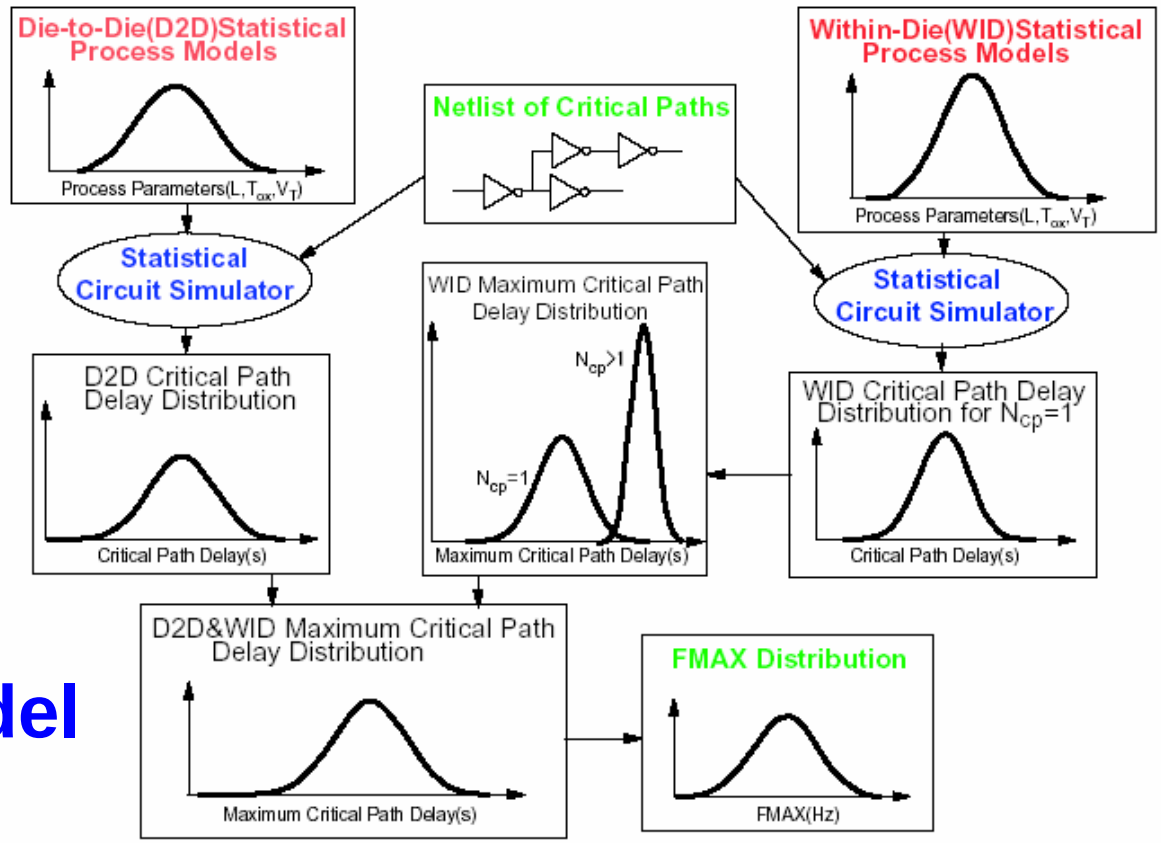
	ΔN_{sub}	$\Delta L_{gate}/0.6\mu m$
Inter	5.9%	6.2%
Intra	2.3%	3.2%

I-3. ばらつき予測

1. Process Model

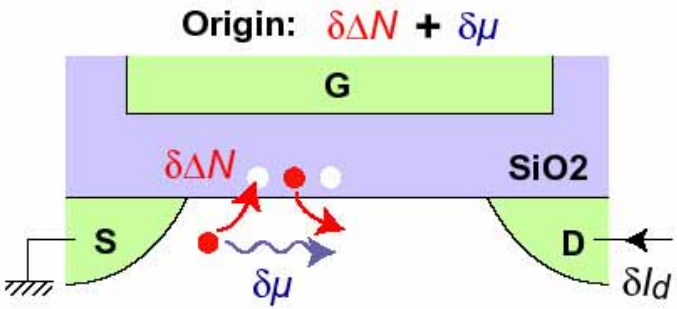
- Inter-Chipばらつき
  - 温度分布
  - 濃度分布
  - プラズマ分布
- Intra-Chipばらつき
  - 濃度ばらつき
  - 欠陥分布 (1/fノイズ)
  - Layout依存性

2. Stochastic Model

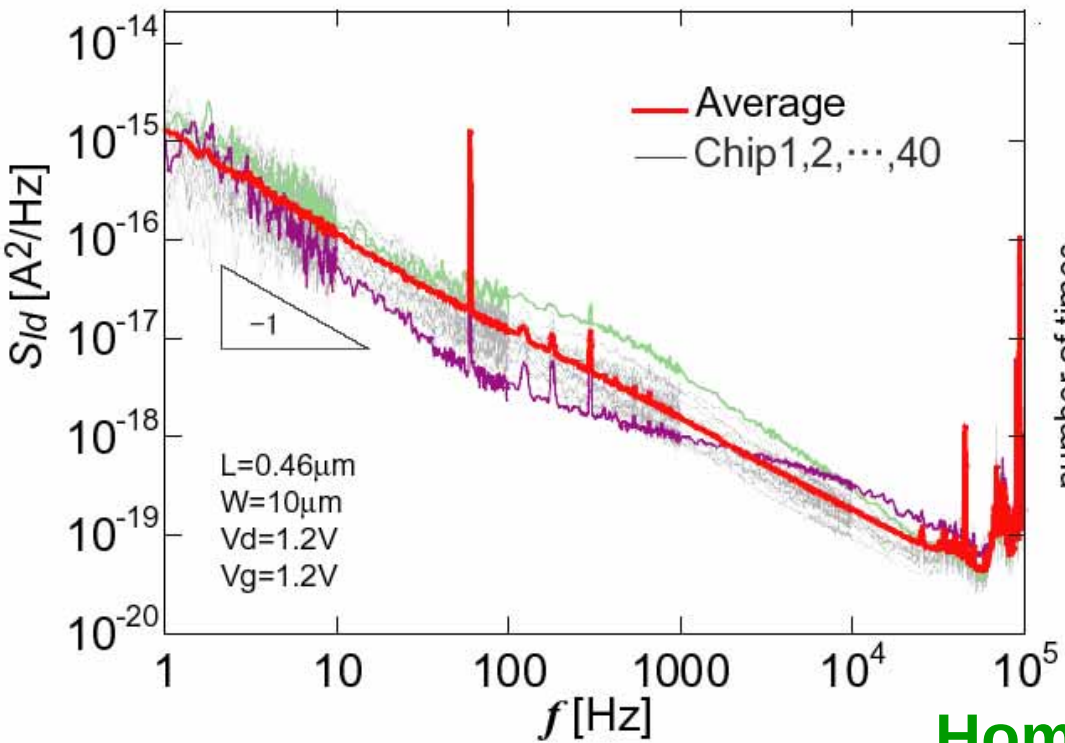


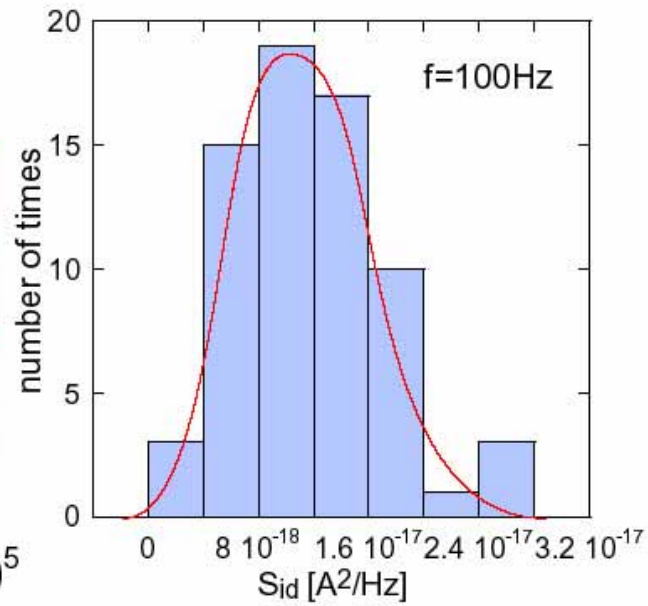
1/fノイズ特性

1/fノイズの起源



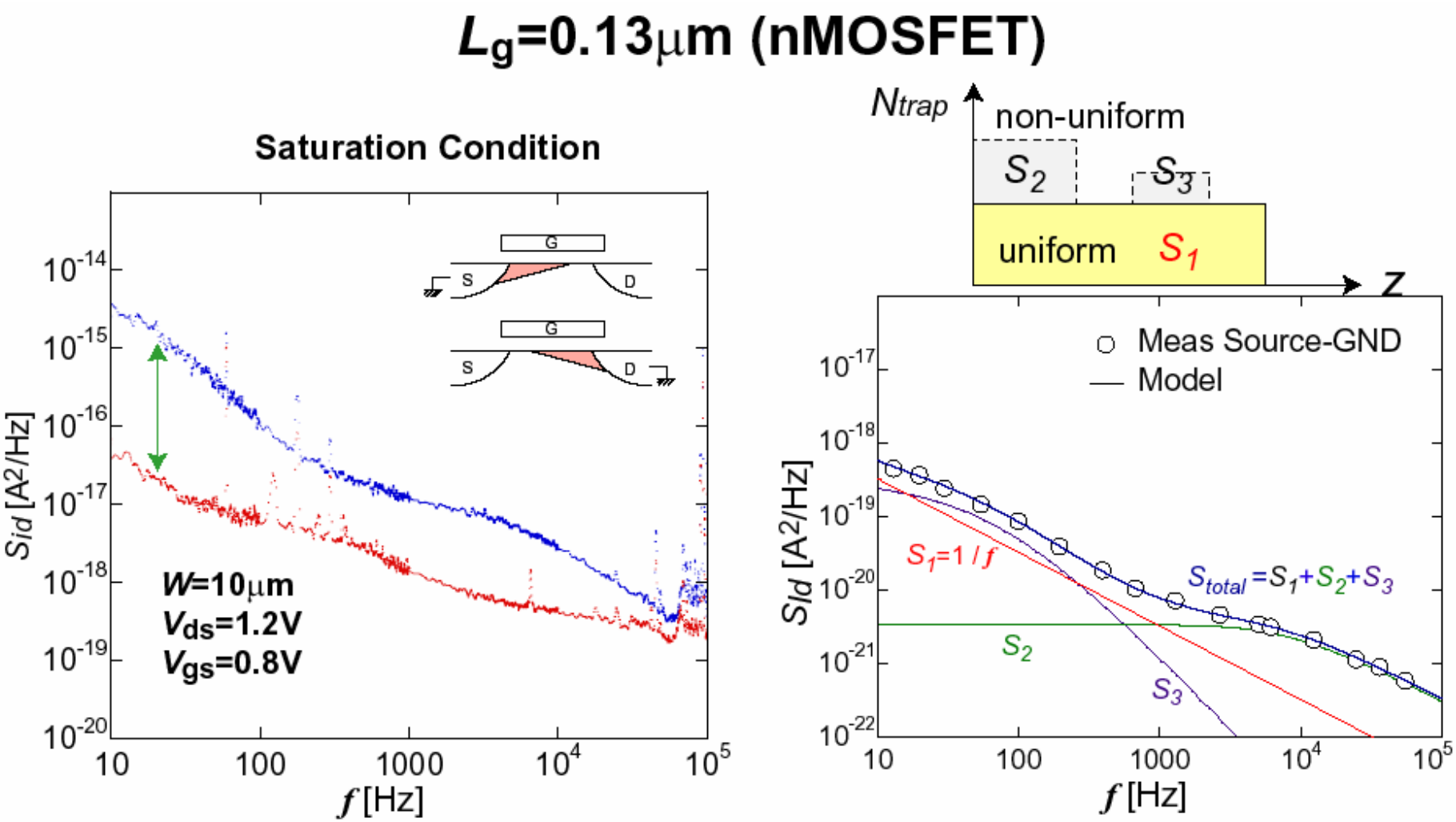
Statistics on a Wafer





Homogeneous Distribution

1/fノイズ特性からのずれ



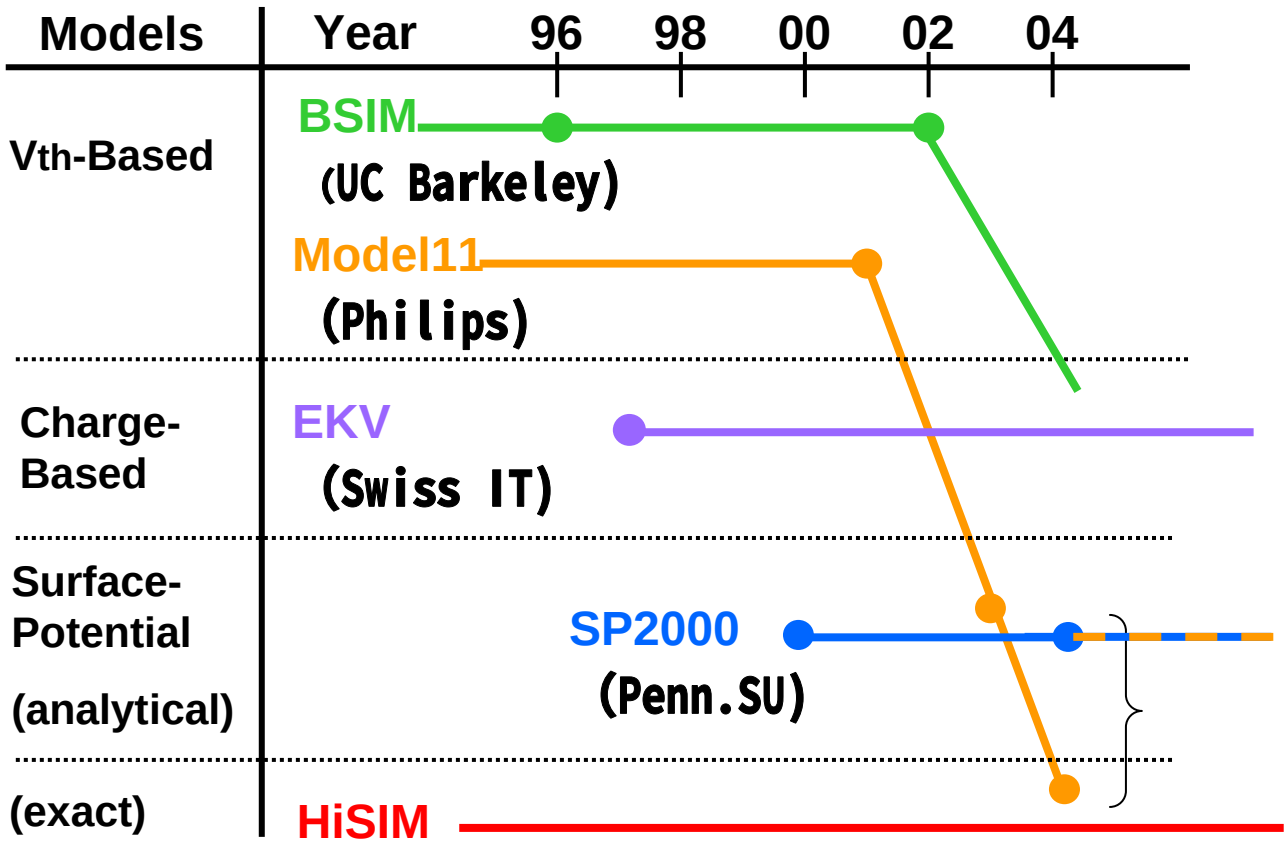
目次

II-1. コンパクトモデル

デバイス ⟷ 回路モデル ⟷ 集積回路

- 回路モデルはデバイスと集積回路をつなぐ要
- 回路モデルの精度が回路予測精度を決定

代表的なモデル



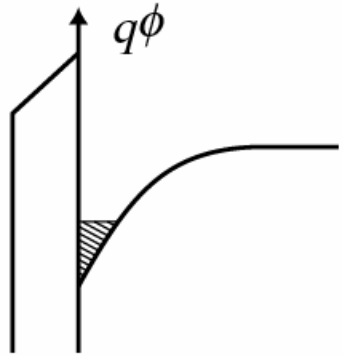
デバイスの基本方程式

-Poisson:

$$\nabla^2\phi = -\frac{q}{\varepsilon_{Si}}(N_D - N_A + p - n)$$

$$n = n_i \exp\frac{q(\phi - \phi_n)}{kT}$$

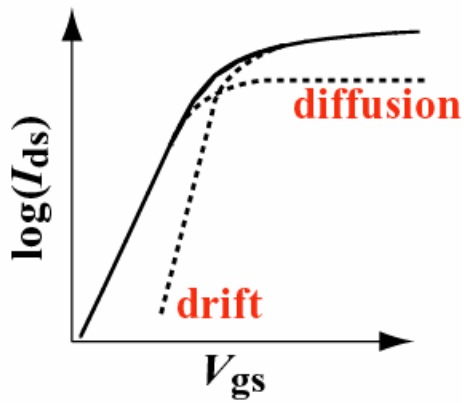
$$p = n_i \exp\frac{q(\phi_p - \phi)}{kT}$$



-Current Density:

$$j_n = q\mu_n n\frac{\phi}{y} + qD_n\nabla n$$

$$j_p = q\mu_p p\frac{\phi}{y} - qD_p\nabla p$$

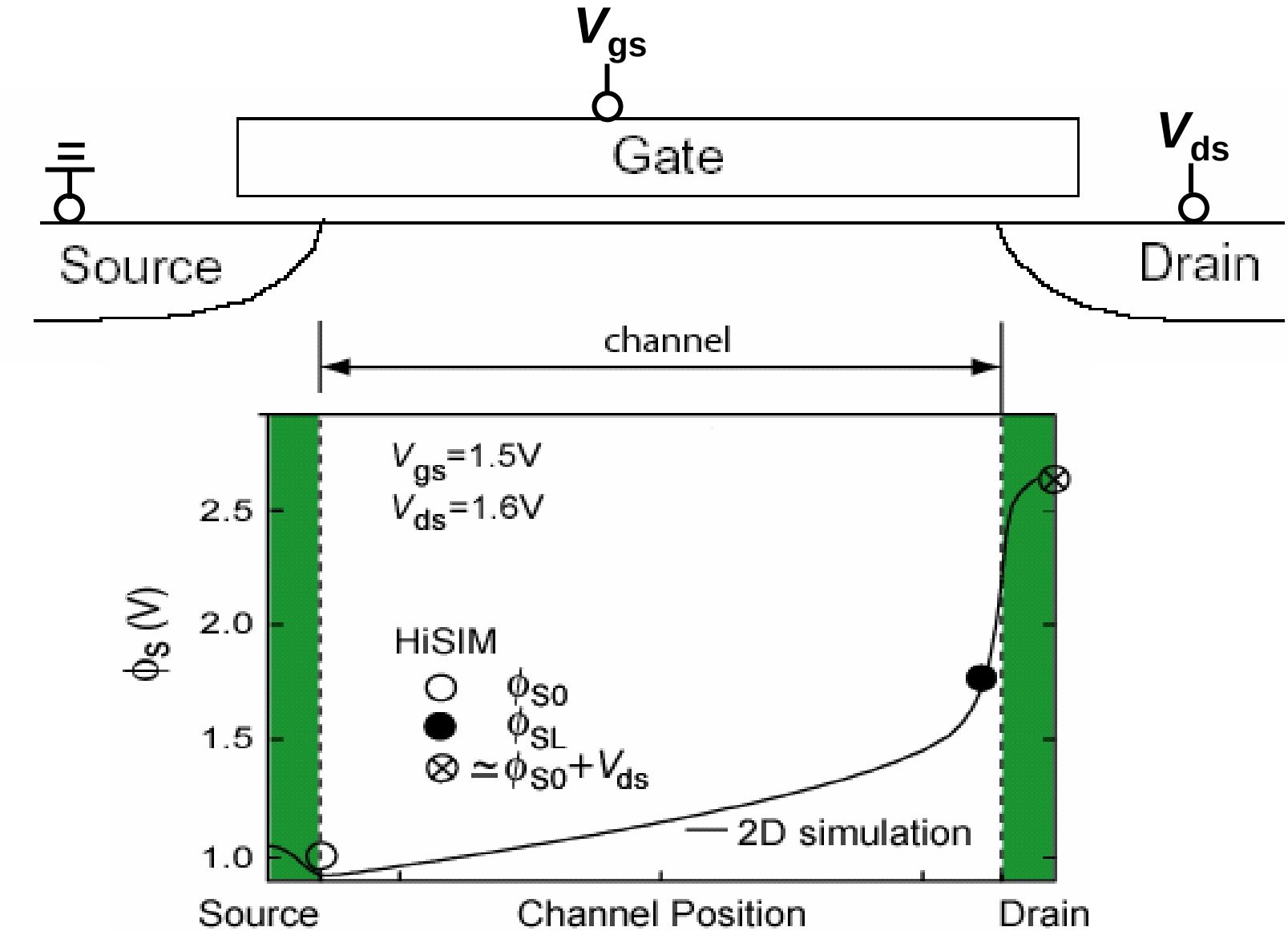


-Continuity: $I(t) = I_0(t) + \frac{dQ}{dt}$

(solved by circuit simulator)

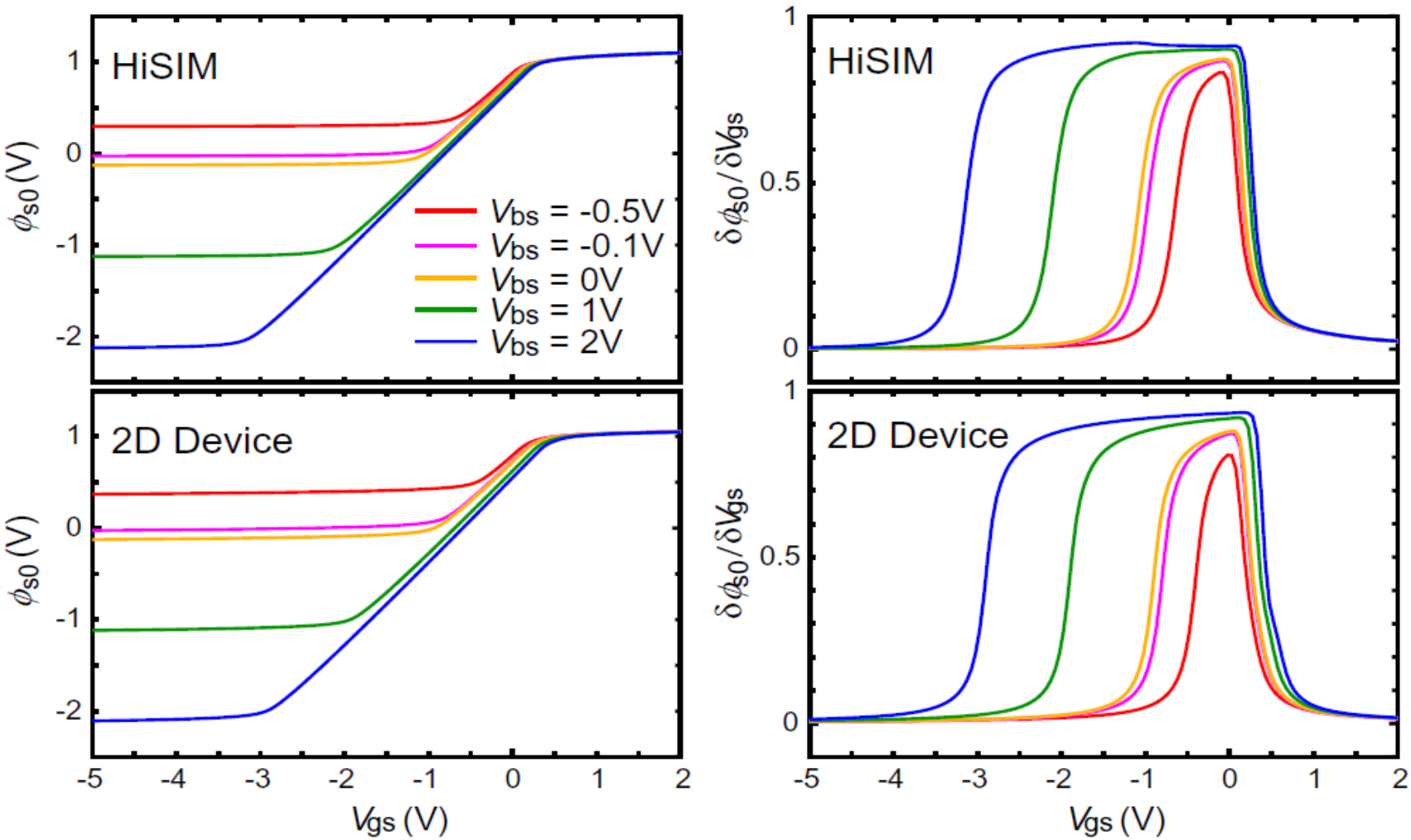
-Quantum Mechanical Effect
-Ballistic Effect

表面ポテンシャル

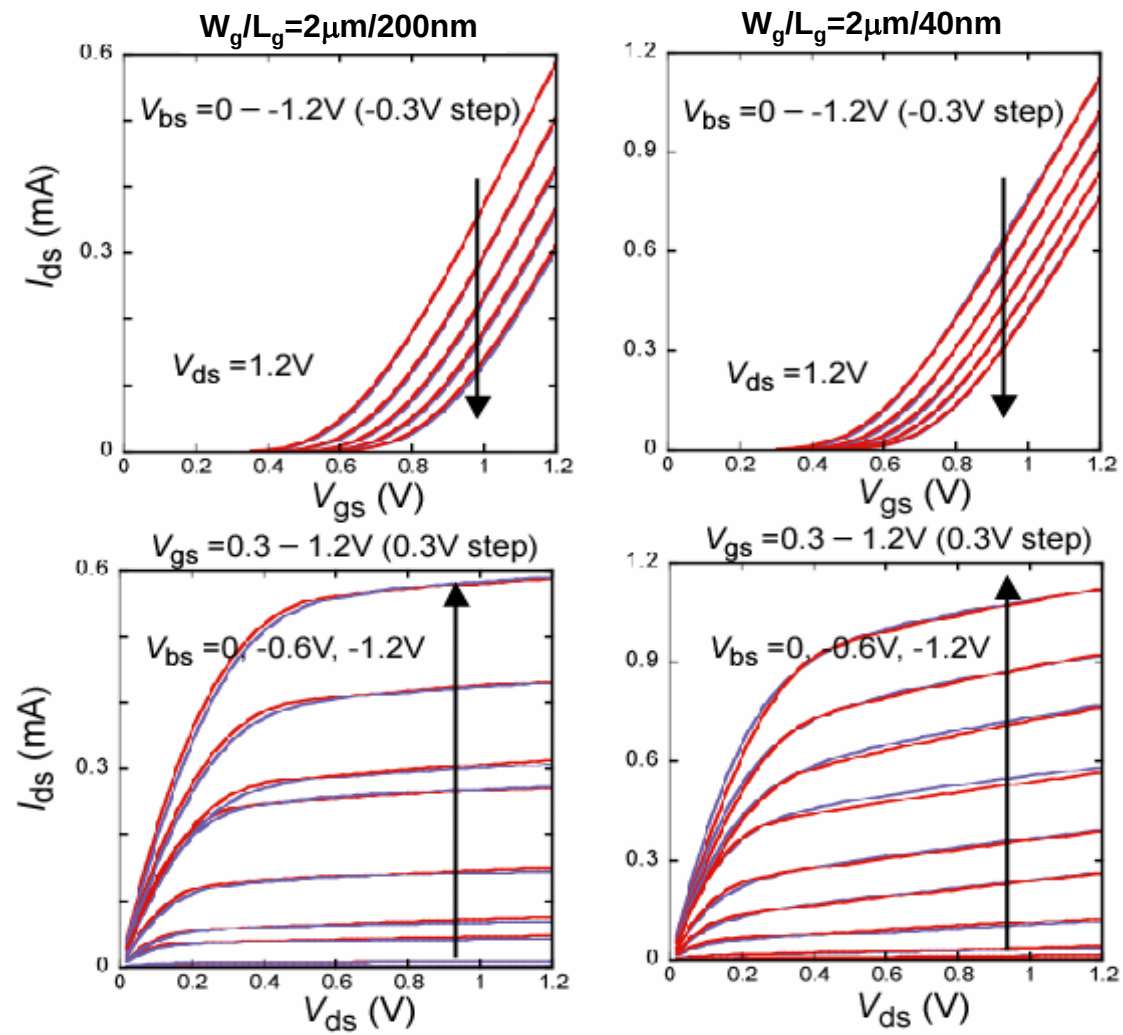

V_{gs}
Gate
V_{ds}
Source
Drain
channel
V_{gs}=1.5V
V_{ds}=1.6V
HiSIM
ϕ_{S0}
ϕ_{SL}
$\otimes \simeq \phi_{S0}+V_{ds}$
2D simulation
ϕ_S (V)
2.5
2.0
1.5
1.0
Source
Channel Position
Drain

II-2. コンパクトモデルの精度

表面ポテンシャルの比較

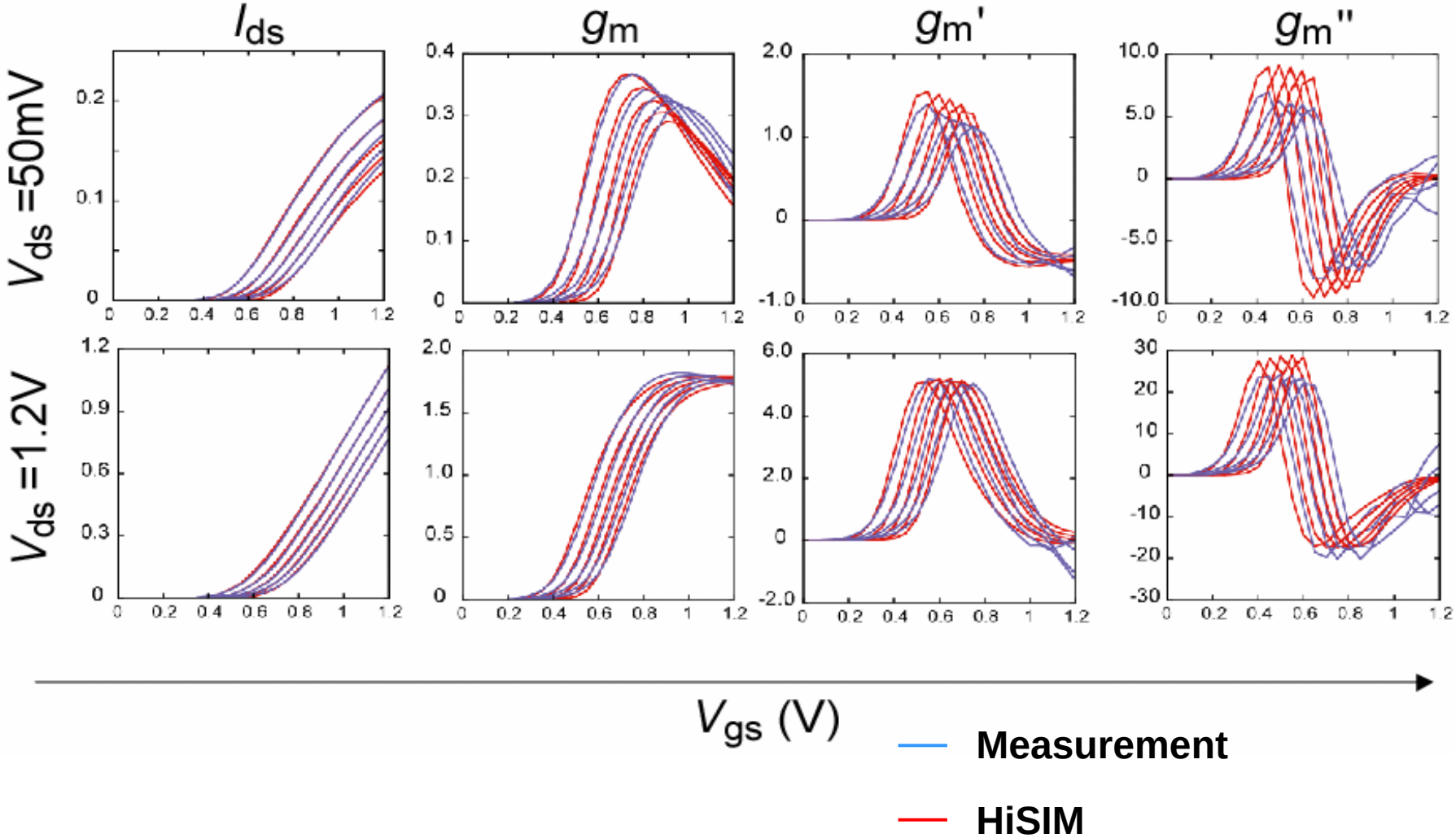


45nmノードにおける電流の再現性

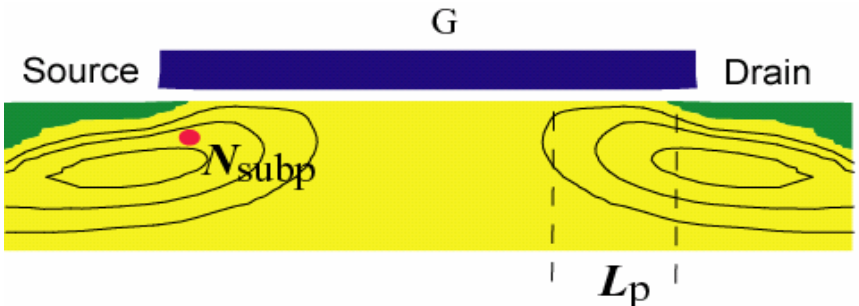


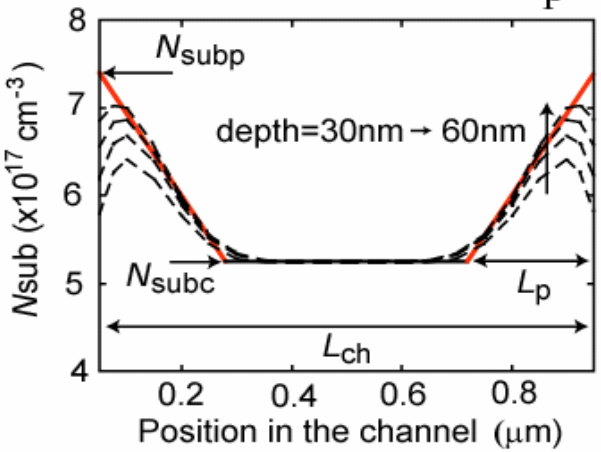
微分値の再現性

W_g/L_g=2μm/40nm

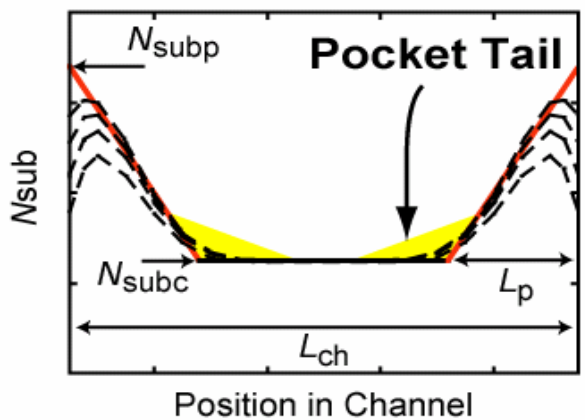


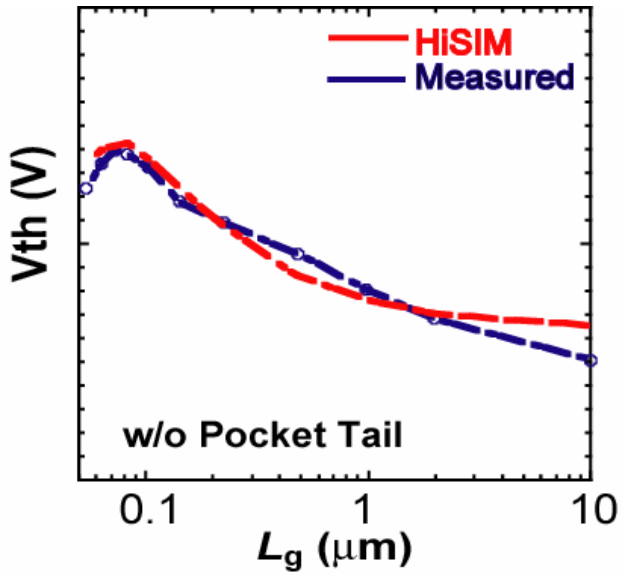
ポケット注入の場合

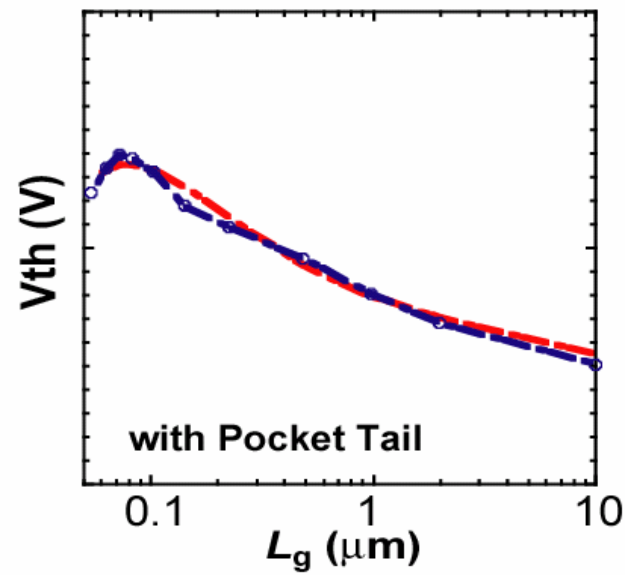




ポケットの近似

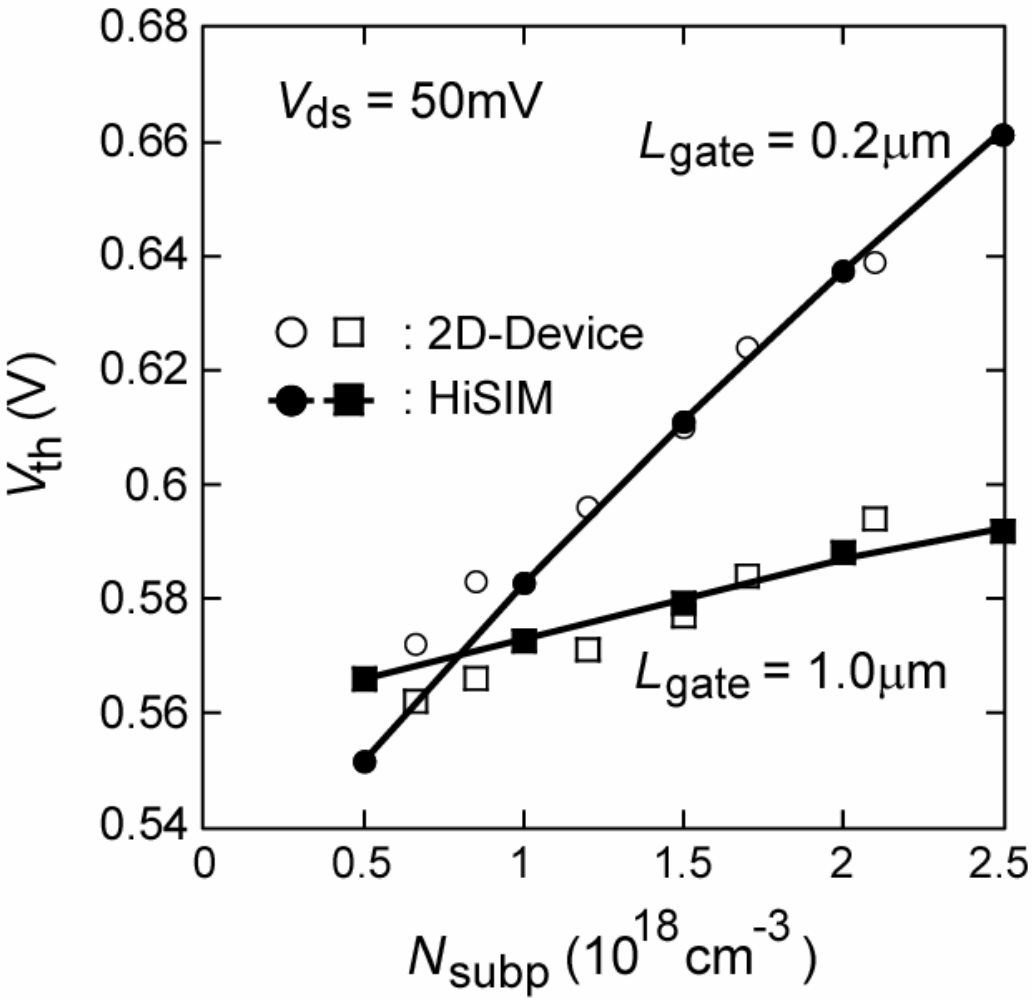






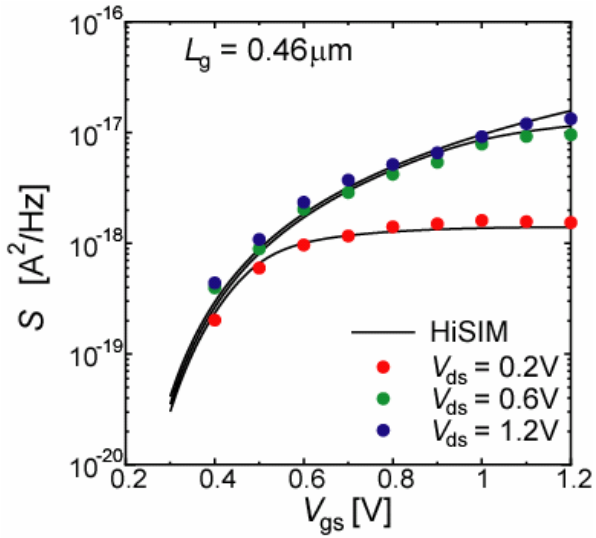
II-3. コンパクトモデルの可能性

モデルパラメタの予測性

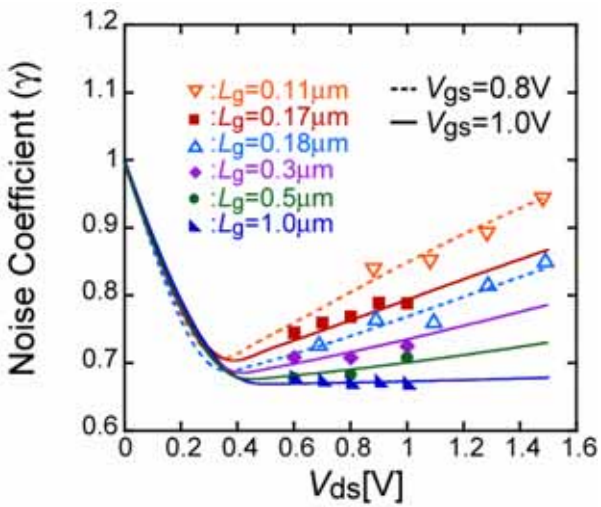


RF特性の予測性

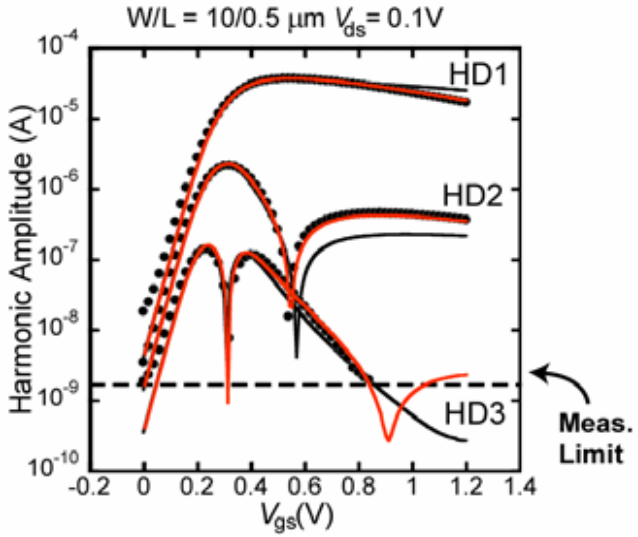
1/*f* Noise



Thermal Noise



Harmonic Distortion



- **No model parameters are required.**
- **Features are determined only by *I-V* characteristics.**

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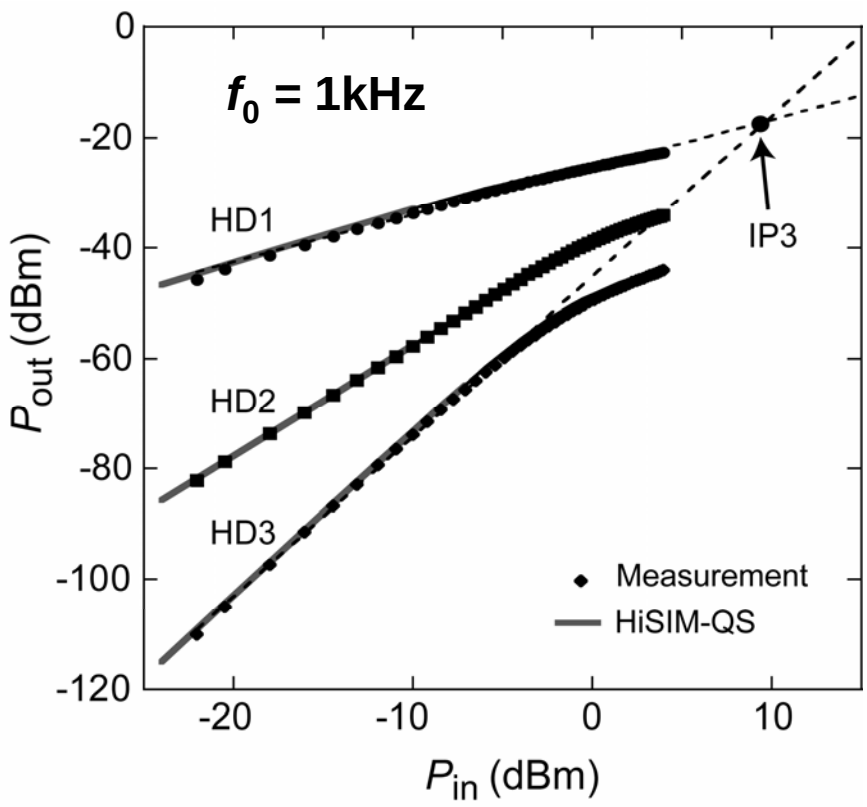
Electrostatic effect is still dominating.

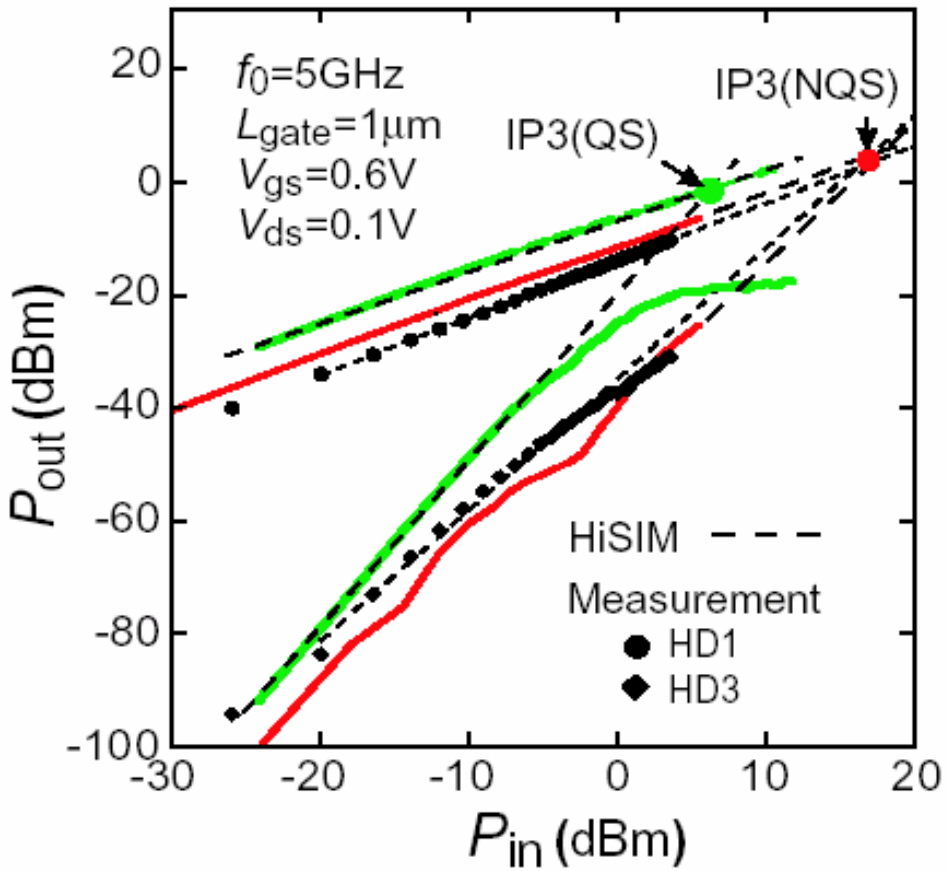
⇩

Surface potential is important.

IP3 Prediction

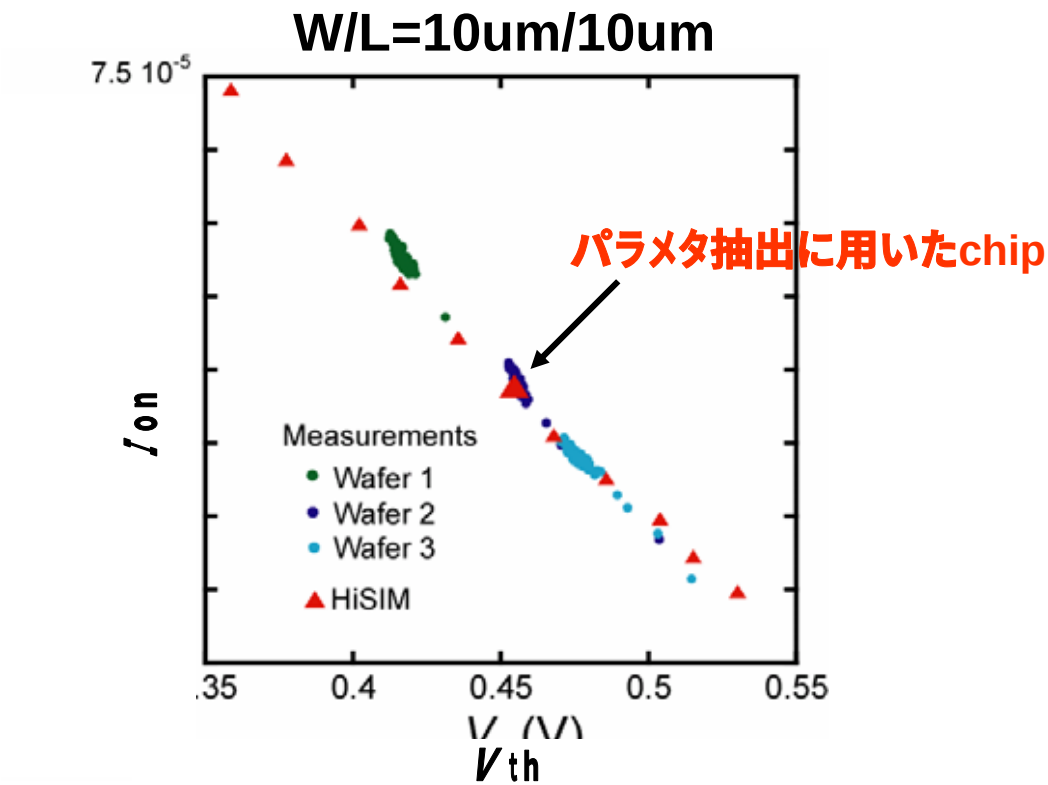
キャリアの遅延効果





Y. Takeda et al., CICC, p. 827, 2005.
D. Navarro et al., IEEE MWC Lett., p. 125, 2006.

基板濃度Nsubを振ったwaferの特性予測



I_{on}は基本的にはV_{th}に支配されている

プロセスばらつきモデルがあればデバイス特性のばらつき予測可能

まとめ

- Intra-Chipばらつきの増大
- Intra-Chipばらつきの原因
  - 不純物分布
  - 欠陥分布
  - Layout依存性
- 各種ばらつきモデルの構築が必須
- Stochasticモデルの構築も大事
  - Inter- & Intra-Chipばらつきの考慮
  - 回路ではばらつきが抑制
  - クリティカルパスの影響