コストへの挑戦
- 多重露光からEUVLへ -

STRJ WG5(Lithography)

March 7 2008

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(Toshiba Corp.)

内容

- はじめに
- ITRS 2007におけるリソグラフィ章
- リソグラフィ技術の現状
  - ArF液浸露光
    - NA>1.35の可能性
    - k1<0.25、DE/DP
  - EUV露光技術
  - NGL
    - ML2
    - Imprint
    - DSA
- 2008年度の活動方針
- まとめ

2007年度 WG5メンバー

- JEITA半導体部会/関連会社　11名

  東川 巌/リーダー (東芝) 、内山 貴之/サブリーダー (NECEL) 、羽入 勇/国際担当 (富士通)、須向 一行 (ルネサステクノロジ) 、笹子 勝 (松下電器産業) 、守屋 茂 (ソニー) 、田口 隆 (沖電気工業)、和田 恵治 (ローム) 、田中 秀仁 (シャープ) 、岡崎 信次 (日立製作所) 、山口敦子 (日立製作所)

- コンソーシアム　2名

  山部 正樹/事務局 (ASET-D2I)、寺澤 恒男 (Selete)

- 特別委員（大学・独立行政法人）　1名

  戸所 義博 (奈良先端大)

- 特別委員（SEAJ、他）　10名

  森 晋 (SEAJ:ニコン) 、山田 雄一 (SEAJ:キヤノン) 、山口 忠之 (SEAJ:TEL)、山口哲男 (SEAJ:ニューフレアテクノロジィ)、龜山 雅臣/国際担当 (ニコン) 、大久保 靖 (HOYA) 、林 直也 (大日本印刷) 、奥田 能充 (凸版印刷)、小野寺 純一(東京応化工業)、栗原 啓志郎 (アライアンスコア)

活動方針

[WG5] “Lithography技術ロードマップの提案” ← ITRS + α

[STRJ] : 半導体技術の15年先までの姿を、国際半導体技術ロードマップ（ITRS）委員会と連携し、詳細技術項目にブレークダウンして予測する。

略語説明

NA	Numerical Aperture
CD	Critical Dimension, CDU (CD Uniformity)
DOF	Depth of Focus
LER/LWR	Line Edge Roughness/Line Width Roughness
RET	Resolution Enhancement Techniques
OAI	Off-Axis Illumination
PSM	Phase Shifting Mask, cPSM (complementary PSM), APSM (Alternating PSM), EPSM (Embedded PSM)
EDA	Electronic Design Automation
OPC	Optical Proximity Corrections, MBOPC (Model Based OPC)
DFM	Design for Manufacturing
SB	Scattering Bar
NGL	Next-Generation Lithography
EUVL	Extreme Ultraviolet Lithography
ML2	Maskless Lithography
NIL	NanoImprint Lithography, UV-NIL (Ultraviolet NIL), SFIL (Step & Flash Imprint Lithography)
DSA	Directed Self Assembly
MEEF	Mask Error Enhancement Factor
ARC	Anti-Reflection Coating, BARC (Bottom ARC), TARC (Top ARC)
AMC	Airborne Molecular Contamination
DE/DP	Double Exposure/Double Patterning
ESD	Electrostatic Discharge
LuAG	Lutetium aluminum garnet: Lu3Al5O12

ITRS Lithography chapter

Potential Solutions

- Figure 67 Lithography Exposure Tool Potential Solutions
- Table 74 Various Techniques for Achieving Desired CD Control and Overlay with Optical Projection Lithography

Difficult Challenges

- Table 75 Lithography Difficult Challenges

Technology Requirements Tables

- Table 76a, b — Lithography Technology
- Table 77a, b — Resist
- Table 77c — Resist Sensitivities
- Table 78a, b — Optical Mask Requirements
- Table 78c, d — EUVL Mask
- Table 78e, f — Imprint Template Requirements
- (Table ML2) — Maskless Lithography Technology Requirements

•Mask design grid slightly updated with new requirements for 16nm HP and beyond
•Resist sensitivity (table 77c) update with higher values

Requirements

DRAM, Flash & MPU has individual TWG tables on 2008 version

Year of Production	*2005*	*2006*	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*
DRAM ½ pitch (nm) (contacted)	*80*	*70*	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*
DRAM and Flash										
DRAM ½ pitch (nm)	80	70	65	57	50	45	40	36	32	28
Flash ½ pitch (nm) (un-contacted poly)	76	63	53	45	40	36	32	28	25	22
Contact in resist (nm)	94	79	70	63	56	50	44	39	35	30.8
Contact after etch (nm)	85	72	64	57	51	45	40	36	32	28
Overlay [A] (3 sigma) (nm)	16	14	13	11.4	10	9	8	7.2	6.4	5.7
CD control (3 sigma) (nm) [B]	7.9	6.6	5.6	4.7	4.2	3.7	3.3	2.9	2.6	2.3
MPU										
MPU/ASIC Metal 1 (M1) ½ pitch (nm)	90	78	68	59	52	45	40	36	32	28
MPU gate in resist (nm)	54	48	42	38	34	30	27	24	21	13
*MPU physical gate length (nm) **	32	28	25	22	20	18	16	14	13	11
Contact in resist (nm)	111	97	84	73	64	56	50	45	40	35
Contact after etch (nm)	101	88	77	66	59	51	45	41	36	32
*Gate CD control (3 sigma) (nm) [B] ***	3.3	2.9	2.6	2.3	2.1	1.9	1.7	1.5	1.4	1.1

Low frequency LWR: (nm, 3 sigma) <8% of CD

ITRS 2007 Update Potential Solutions

Potential Solutions

2003 Edition | 2004 Update | 2005 Edition | 2006 Update | 2007 Edition

100
90
80
70
60
50
40
30
20

90@2004
65@2007
45@2010
32@2013
22@2016
16@2019

2003 Edition: ArF + LFD + Imm. | F_2 RET+LFD+Imm | PEL | ML2 | EPL | EUV RET | Imprint | Innovation

2004 Update: PEL | ArF + LFD + Imm. | F_2 RET+LFD+Imm | Innovative Immersion | EUV RET | ML2 | Imprint | Innovation

2005 Edition: 193nm | 193nm Immersion | 193i w/ other fluids | Innovateve | EUV (innovative) | Imprint | ML2 | Innovation

2006 Update: 193nm | 193i w/ water | 193i w/ DP | 193i+ | 193i++ | Innovateve | EUV (innovative) | ML2 | Imprint | Innovation

2007 Edition: 193nm | 193i w/ water | 193i w/ DP | 193i++ | Innovateve | EUV (innovative) | ML2 | Imprint | Innovation | DSA

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ITRS Lithography TWG Activities Potential solutions

- Potential solutions table 2007
  - 45nm HP: only 193i and 193DE/DP
  - 32nm HP: order 193DE/DP, EUVL, 193i+, ML2, Imprint
  - NA chart will be included covering both logic/memory and single/double exposure but only a footnote to cover required fluid refractive index
- Potential solutions table discuss potential solutions table for flash
- Study on what EUVL for 16nm would look like / EUVL extendibility requirements beyond 22nm HP
- Consider how to handle different timing requirements for logic and memory (drive potential solutions table by timing instead of node?)
- Critical reviews (ML2, Nanoimprint, DSA, others)

Still no known solution for current required CD uniformity for MPU gate

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ITRS Lithography TWG Activities Tables

- Separate lithography requirements table into sections for logic, DRAM, and flash + Color in table, DP/DE
  - Achievable CDU / CDU component from LWR, CDU budget
    - PIDS / FEP / Design / Litho Discussion, What is the right physical gate size?
    - LWR/LER / Correlation length?, Etch or litho or both?
  - Achievable overlay (color in table, double patterning)
  - Focus budget
    - Patterned reticle flatness requirement (for optical litho)
    - Blank flatness scaling (linear in 2007, might need to be faster than linear)
- Mask Specification / Double patterning, Computational lithography, Inverse lithography
  - 3D / 3D mask specifications
  - Pellicle thickness uniformity requirement will be included but recommend that the scaling be reinvestigated in 2008
- Process control requirements for double patterning, double spacer or multiple exposure processes
- Requirements for OPC
  - Through-pitch stability, etc
  - OPC residual error
- Small lot factory requirements (in conjunction with factory TWG)
- 450mm impact to litho
- Consider updates to Maskless litho table, Nanoimprint table

Still no known solution for current required CD uniformity for MPU gate

Cross-TWG

- Yield TWG
  - Reticle storage requirements
    - Survey of fabs?
  - Immersion water TOC requirements (and other requirements)
- ESH
  - Low power EUV source requirements?
- Factory
  - Small lot size requirements
  - Process control requirements document

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Lithography: Which Direction ?

5000 lots/month → ~ 20 high end exposure tool

Litho cluster
Litho cluster
Litho cluster

$ > ~50 % ?

CR Design

Where it's going !

Where lithography headed ?

Innovative ?
HIL
DPT
EUV
ML2
NIL
DSA
Ion beam

Cost of Lithography

Scanner
Track
Design
Mask
Litho. Process
.....

Cost

- Exposure tool -

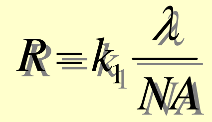
Lithography cost

Track 7%
Supply 0%
Mask 7%
Expendable 2%
Laser 8%
Exposure tool 76%

Cost

100
10
1
Cost
10
100
1000
Resolution [nm]
Litho cluster
Exp.

Optical extension



$$R = k_1 \frac{\lambda}{NA}$$

	half pitch [nm]	130	100	90	65	45	32	22	16	11
	year	*DRAM/Logic*			*2007*	*2010*	*2013*	*2016*	*2019*	*2022*
λ [nm]	NA	*Flash*			*2006*	*2008*	*2011*	*2014*	*2017*	*2020*
248	0.82	0.43	0.33	0.30	0.21					
	0.93	0.49	0.38	0.34	0.24	0.17				
193	0.93	0.63	0.48	0.43	0.31	0.22				
	1.2		0.62	0.56	0.40	0.28	0.20			
	1.3		0.67	0.61	0.44	0.30	0.22			
	1.35			0.63	0.45	0.31	0.22	0.15		
	1.55			0.72	0.52	0.36	0.26	0.18		
	1.7				0.57	0.40	0.28	0.19	0.14	
13.5	0.25					0.83	0.59	0.41	0.30	
	0.35						0.83	0.57	0.41	0.29
	0.45							0.73	0.53	0.37

Low k1 → OPC, RET, PSM,…

2007

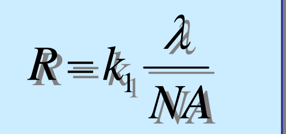
λ NA k1

λ、NA、k1 Challenges

$$R = k_1 \frac{\lambda}{NA}$$

NA, k1, λ Challenges

- 32 nm hp -



NA	k1	λ
ArF Immersion 1.7 NA (k1=0.28) Single exposure	ArF Water Immersion with Double Patterning 1.35 NA (k1=0.22)	EUVL 0.25 NA (k1=0.59) Single exposure

Challenges

NA	k1	λ
Lens complexity New liquid (n > 1.8) New resist (n > 1.8) New optical material (n>1.9)	Overlay requirement Process integration TAT Throughput CoO	P.O., Illu., SoCoMo Source power Lifetime/CoO Resist Mask, Pellicle_less

Water (Wet) vs. Air (Dry)

NA = 1.35

NA = **n** sin θ

NA = 0.93

θ

lens	n~1.56
water	n=1.44
resist	n=1.60

θ

lens	n~1.56
air	n=1.0
resist	n=1.60

36.59°
59.93°
67.38°
67.38°
36.59°
n~1.56
39.87°
Water
69.64°
40.23°
n=1.44
DoF up
68.43°
Air
n=1.0

NA = 1.35 NA = 0.93 NA = 0.93

High Index Materials

NA = $n \sin \theta$

θ

lens n = 1.56

water n = 1.44

resist n = 1.60

NA = 1.35

NA = 1.70

High Index Glass
+
High Index Fluid
+
High Index Resist
(TC, BARC)

θ

lens n = 2.14 LuAG

fluid n = > 1.8 Nano Particle

resist n = > 1.8 Nano Particle

Only 20% up of resolution
Pool system,…

EUVL Technical Issues

Pitch～7nm
Mo
Si
＞40 Multi-layers

Defect free

多層膜反射マスク
・超平坦化、無欠陥マスクブランクス
・無欠陥多層膜スパッタ技術
・欠陥検査・修正技術
・EUVL固有パターンデータ処理
（斜入射、フレア）

真空露光システム
・スキャンステージ
・アライメント
・コンタミ、パーティクル
・温度制御技術

静電チャックステージ
ペリクルレスマスクハンドリング

Mask stage
Mask

Polish **熱**

ミラー光学系
・超平坦化技術、高反射率
・コンタミ、クリーニング
・熱（反射率～70%）
・収差（Wavefront<0.5nm rms）
・フレア（MSFR<0.1nm rms）
・波面計測

ML

照明光学系
・クリーニング/光学系寿命
・熱
・高反射率、OoB、SPF

LPP
DPP

Power W@IF:
3 → 50 → 115 → 180 → >300

Power

EUV 光源（λ=13.5nm）
・高出力、低エタンデュー、出力安定性
・低デブリ
・寿命(集光光学系、光源)
・エネルギー効率(CE)
・熱

Wafer
Wafer Stage

Sensitivity
Resolution **LER/LWR**

レジスト
・高感度・高解像力・低LER
・低アウトガス

ADT EUV1
2008 Scan exposure

日本のEUVリソグラフィ技術開発経緯と計画

‘98 | ‘99 | ‘00 | ‘01 | ‘02 | ‘03 | ‘04 | ‘05 | ‘06 | ‘07 | ‘08 | ‘09 | ‘10

hp180nm hp130nm hp90nm hp65nm hp45nm

α機 β機 量産機

文科省リーディングPJ 光源開発 ‘02 -’07

METI新規事業/
H15年度より/NEDO

EUVA
- 光源技術 ギガフォトン、コマツ、ウシオ ‘02 -’07
- 露光装置技術 ニコン、キヤノン ‘03 -’07
- 絶対波面計測技術 ‘01 -’05 ニコン、キヤノン
- NEDO継続研究 ニコン・キヤノン

光源

ASET
NEDO
EUVの要素技術開発
デバイスメーカー：国内10社＋海外2社
装置メーカー：ニコン、島田理化

（基盤促事業）
02/01に発足

H15年度から
EUVAに移管

NEDO加速資金
レジスト評価

マスク・レジスト技術 ‘02 -’06
デバイスメーカー：国内10社＋海外2社

（NEDO継続研究）
ASET自主研究
半導体業界出資
H14年度に発足

MIRAI
リソグラフィ関連
マスク＆計測技術 ‘01 -’05

SFET EUV1

Selete
次世代マスク基盤技術 ‘06 -’10
次世代リソグラフィ・マスク実用化技術

EUVL

$k1=HP * NA/\lambda$

方式	NA	DRAM Half-Pitch							
		2007	2010	2013		2016		2019	
		65nm	45nm	32 / SE	32 / DP	22 / SE	22 / DP	16 / SE	16 / DP
193i	0.92	0.31	0.21	0.15	0.31	0.10	0.21	0.08	0.15
	1	0.34	0.23	0.17	0.33	0.11	0.23	0.08	0.17
	1.07	0.36	0.25	0.18	0.35	0.12	0.24	0.09	0.18
	1.2	0.40	0.28	0.20	0.40	0.14	0.27	0.10	0.20
	1.3	0.44	0.30	0.22	0.43	0.15	0.30	0.11	0.22
	1.35	0.45	0.31	0.22	0.45	0.15	0.31	0.11	0.22
	1.45	0.49	0.34	0.24	0.48	0.17	0.33	0.12	0.24
	1.5	0.51	0.35	0.25	0.50	0.17	0.34	0.12	0.25
	1.6	0.54	0.37	0.27	0.53	0.18	0.36	0.13	0.27
	1.7	0.57	0.40	0.28	0.56	0.19	0.39	0.14	0.28
EUV	0.25	1.20	0.83	0.59		0.41		0.30	
	0.3	1.44	1.00	0.71		0.49		0.36	
	0.35	1.69	1.17	0.83		0.57		0.41	
	0.4	1.93	1.33	0.95		0.65		0.47	

高NA-EUVにより16nm-hpも視野に！

Multiple Exposure
- DE, DP -

- k1 - 0.35 0.30 0.25 0.2 0.15 0.1

- Current DP -

Pitch doubling

Alt.PSM + Trim

DDL_x + DDL_y

Tip to Tip

Cross Point

DP_LELE

DP_Track_only (ex. Resist freeze)

DE_Magic_material (ex. Ultra_CEL)

Spacer

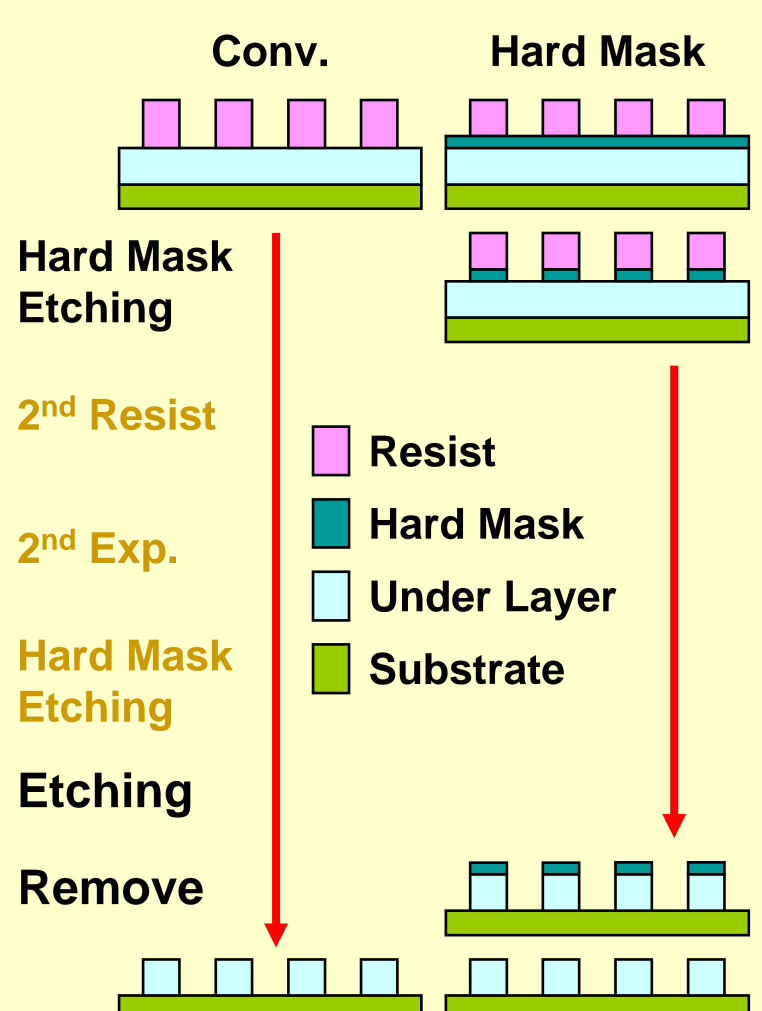
Double Spacer

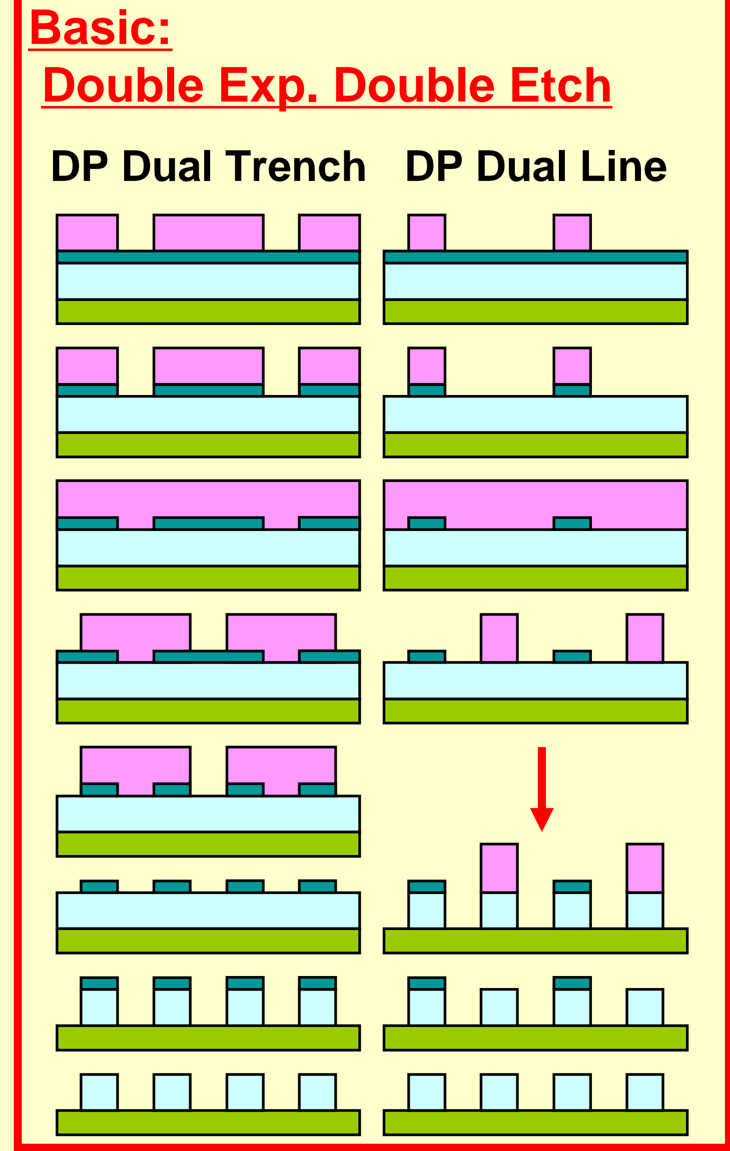
Resist slimming

Contact shrink

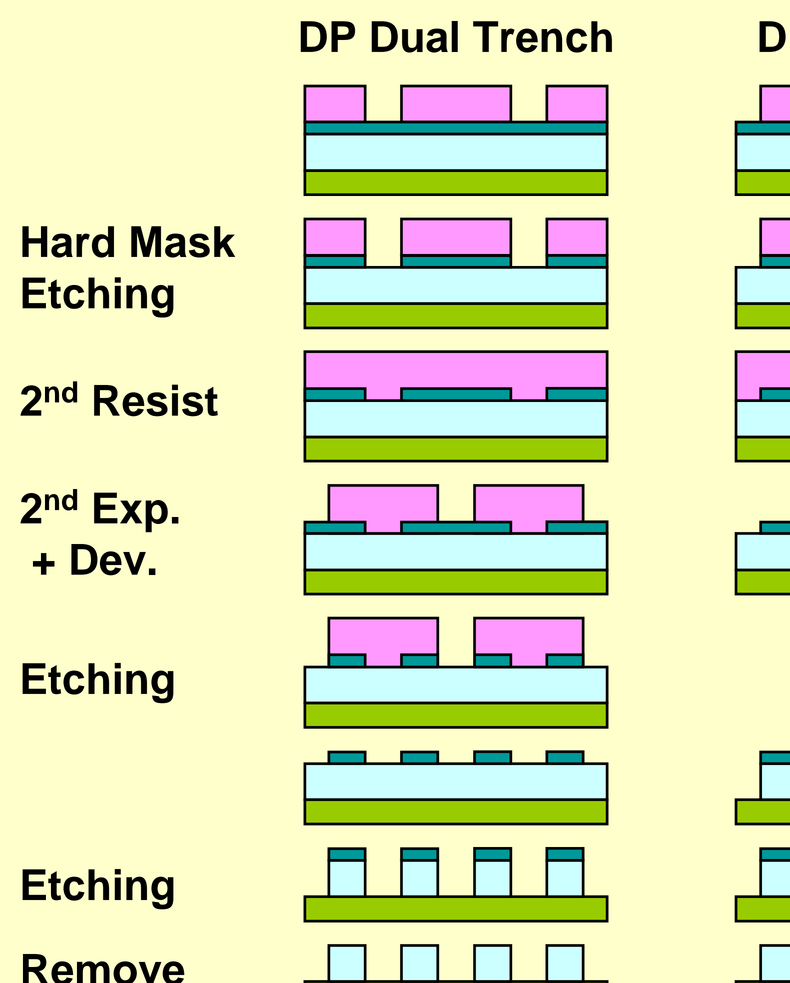
- Post Process -

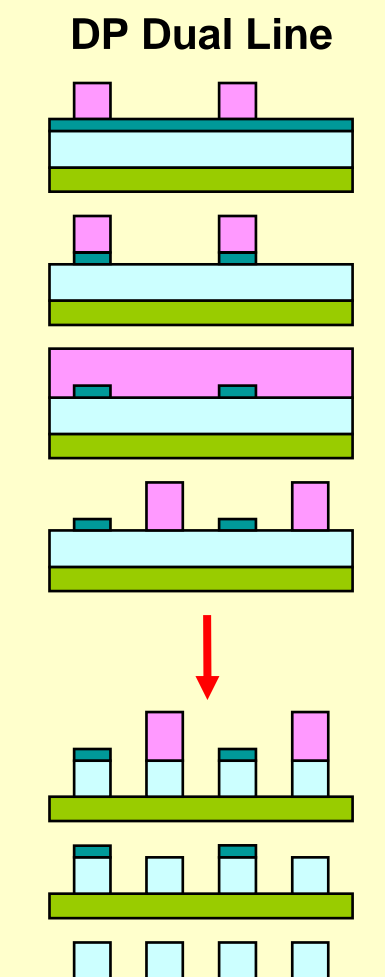
DPT

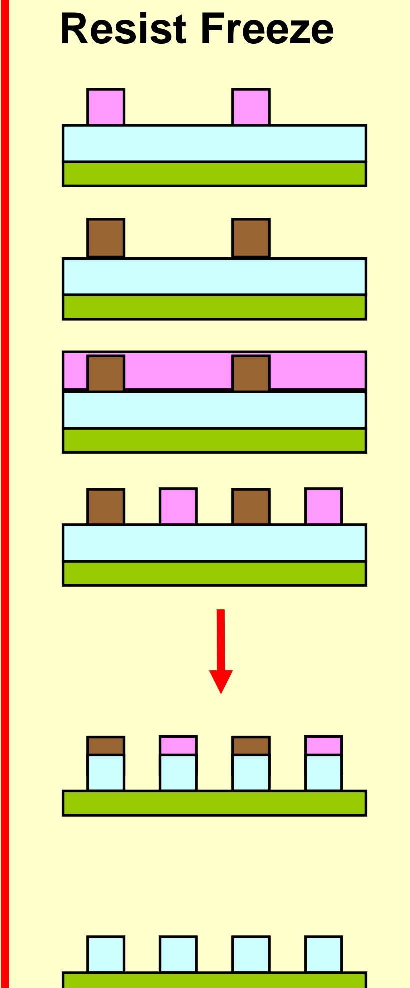




Resist
Hard mask
Under Layer







Resist Freeze

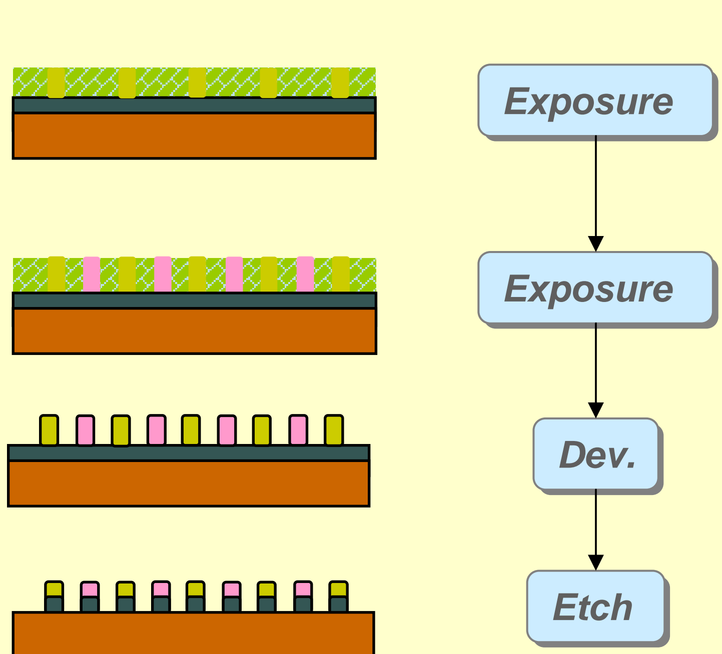
2nd Resist

Deposition
UV, e-beam, ion
Chemical

UV Cure
/Thermal/Chemical
Crosslink
Surface modification,
Developer protection
Surface coating

Magic Material

Magic CEL
Resist
Under Layer
Substrate



Exposure → Exposure → Dev. → Etch

Non-Linear Material

Two Photon Reaction

Exposure → CEL recovering Short time delay → Exposure → Dev. → Etch

Memory less CEL
(Ultra CEL)

Spacer, Double Spacer

×2

DE/DP CDU issues

Double Exposure	Double Patterning	Spacer double patterning
Mask 1	Mask 1	Mask 1
Expose trenches	Print trenches and etch hardmask	Top hardmasketch Spacer formation
Mask 2	Mask 2	Oxide deposition CMP
Expose trenches	Coat and expose second resist	Spacer removal Oxide removal Bottom hardmasketch
Develop and etch	Etch hardmask and device layer	

Uncorrelated

Mask 1

Mask 2

Space is critical feature

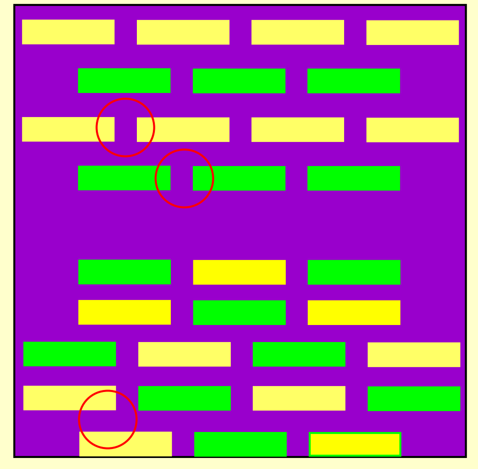
Correlated

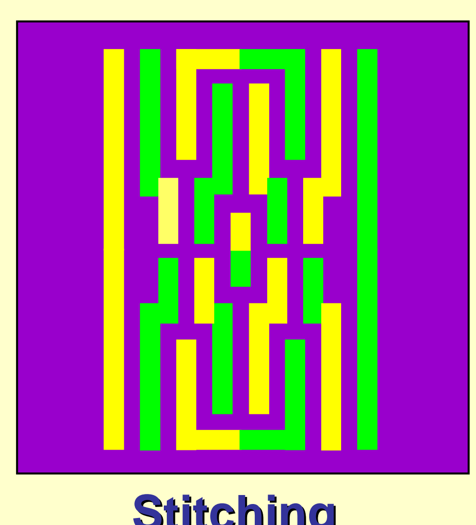
Mask 1

Mask 2

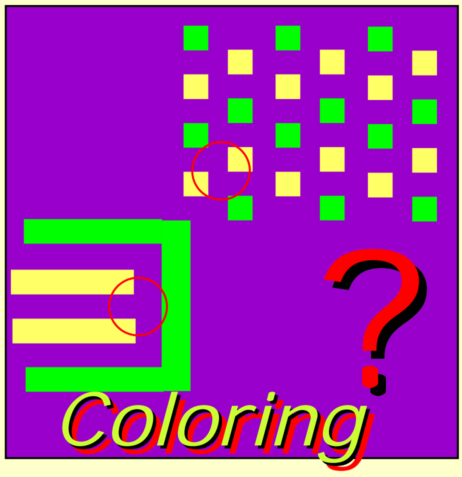
Line is critical feature

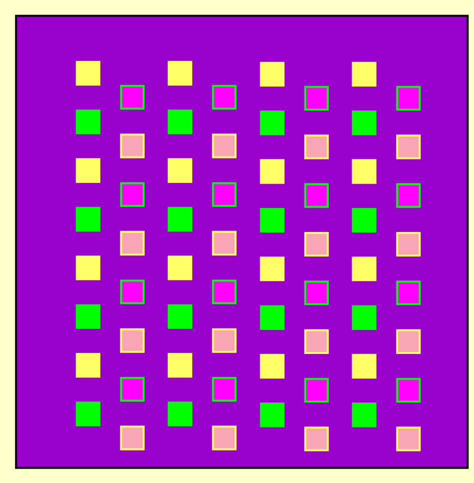
Restricted Design Rule
Coloring Confliction & Area Penalty

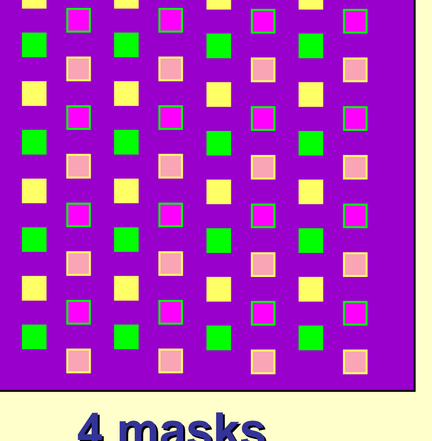




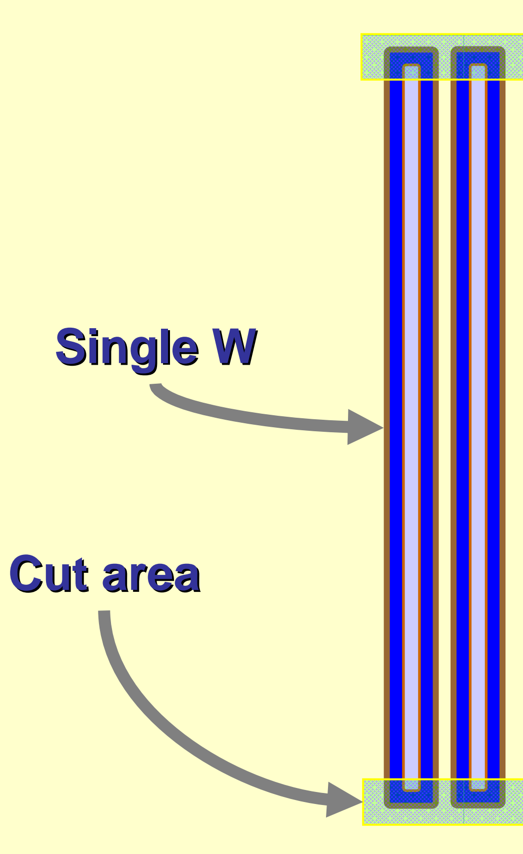
Stitching







4 masks



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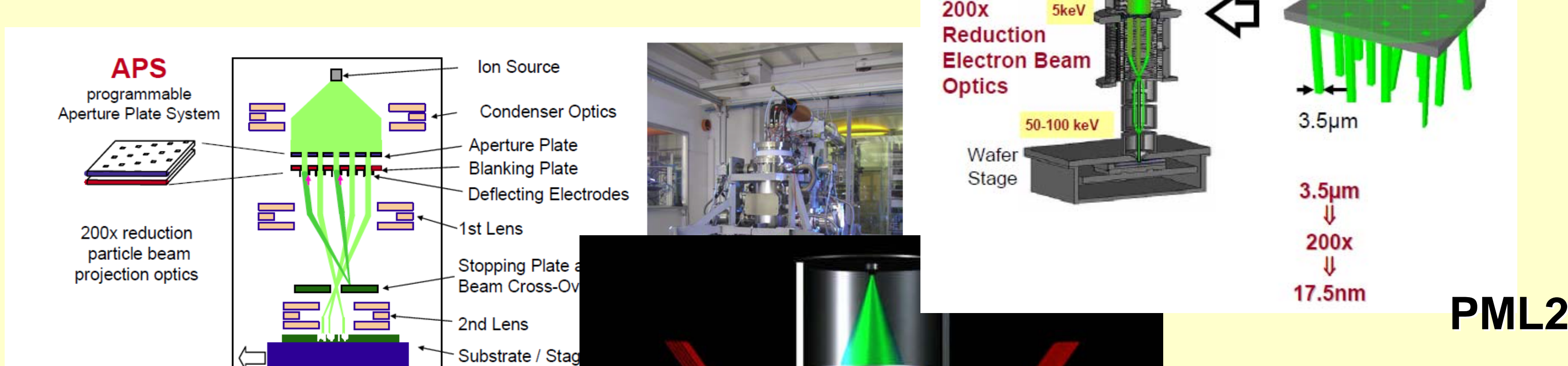
ML2 (Mask Less Lithography)

- E-beam, Photo, Ion-beam



PML2

PMLP/IMS Nanofabrication

Multibeam Systems

ZPAL/LumArray

OML/Micronic, ASML

MAPPER

DARPA **DIVA** ***MAGIC***

Marching of the microlithography horses: Electron, ion, and photon: Past, present, and future
Burn J. LinProc. of SPIE Vol. 6520 652002-1

Nanoimprint

High resolution quartz template, coated with release layer

S-FIL fluid dispenser

Low viscosity fluid (Si-containing)

Template

Planarization layer

Substrate

Step 1: Dispense drops

Step 2: Lower template and fill pattern

very low pressure < 1/20 atmosphere at room temp

Step 3: Polymerize S-FIL fluid with UV exposure

Step & Repeat!

Step 4: Separate template from substrate

LER/LWR, 3D (DD)

http://www.molecularimprints.com/NewsEvents/techarticles.html

DSA (Directed Self Assembly)

Guided/Aligned directed self assembly

Align on under mark

Guided by side wall

k1<0.25: Ultra-Low k1 Lithography

Design Rule Degree of Restrictions
DFM, Data splitting
Process Steps / Complexity
Cycle time / Mask Layers / Line capacity
Tool/Overlay, CDU
Metrology
Yield, Chip size

CoO

LELE
2 Critical Exposure with
Overlay Challenges +
Non Critical Trimming

Spacer
1 Non Critical Exposure
with CDU Challenges +
Non Critical Trimming

Cost
Others
Lithography
DP
SE
Other process
Material handling
Metrology
DP
High end/Immersion
ArF_Dry
KrF
i-line
DP+, & process+
Δ TAT
Δ Cost
Δ CR
Yield
Chip size

内容

- はじめに
- ITRS 2007におけるリソグラフィ章
- リソグラフィ技術の現状
  - ArF液浸露光
    - NA>1.35の可能性
    - k1<0.25、DE/DP
  - EUV露光技術
  - NGL
    - ML2
    - Imprint
    - DSA
- 2008年度の活動方針
- まとめ

2008 Discussions

- Spacer / sidewall double patterning requirements
- Double spacer, Triple exposure requirements
- Double patterning – revisit mask specifications?
- Inverse lithography requirements (especially for the mask)
- Should any aspects of computational lithography be included in roadmap?
- Mask requirements, phase control, through-pitch CD, MEF
- Requirements for OPC
  - Through-pitch stability, etc
  - OPC residual error
- Consider reducing size of litho chapter to emphasize most critical issues (2009)

2008 Discussions / Preparations

- Potential solutions table
  - Study on what EUVL for 16nm would look like
  - Consider how to handle different timing requirements for logic and memory (drive potential solutions table by timing instead of node?)
  - Critical reviews (ML2, Nanoimprint, DSA, others)
- Consider patterned reticle flatness requirement (for optical litho)
  - Consider change to blank flatness scaling (linear in 2007, might need to be faster than linear)
  - Overall depth-of-focus budget
- Consider updates to maskless litho table
- Consider process control requirements document (in conjunction with factory TWG)
- Consider adding 3D mask specifications
- Small lot factory requirements (in conjunction with factory TWG)
- 450mm impact to litho
- Other ideas???

450 mm wafer

Critical Judge Point

- LuAG
  - 2008.3.31. SEMATECH Funding Judge
- EUVL
  - 2008.5.12~14. SEMATECH Lithography Forum
  - 2008.9 29.~10.1. EUVL Symp.

まとめ

- 光
  - 多重露光技術で32nm-hp以降への適用可能性
  - 高屈折率液浸(~NA 1.7)は材料開発遅延

  <多重露光の課題>
    - RDR & DATA splitting: パターン分割(ソフト)
    - Process & Material： Magic Material、Spacer、Resist Freeze
    - Scanner： 重ね合せ(装置/マスク)、スループット
- EUV
  - EUV のHVM機のリリース時期は2011以降
    - 高NA化により16nm-hpも視野

  <EUVLの課題>
    - 高出力光源，集光ミラー寿命，レジスト感度&LER、ペリクルレス…
- **共通の課題 ＝ コスト**