ITRS 2008の概要

半導体技術ロードマップ専門委員会（STRJ） 委員長

石内秀美 （東芝）

主要略語一覧（アルファベット順）

- ERD: Emerging Research Devices　新探究デバイス
- ERM: Emerging Research Materials 新探究材料
- EUV:　Extreme Ultra Violet
- FEP:　Front End Process (ITRSの章の名前でもある）
- High-k:　高誘電率（比誘電率の記号としてkを使うことから）絶縁膜。MOSFET用のゲート絶縁膜
- ITRS:　International Technology Roadmap for Semiconductors　国際半導体技術ロードマップ
- JEITA:　社団法人　電子情報技術産業協会（Japan Electronics and Information Technology Industries Association）
- Low-k:　低誘電率（比誘電率の記号としてkを使うから）絶縁膜。多層金属配線用絶縁膜
- M1:　Metal-1　最下層（第1）の金属配線層
- MPU: Micro Processor Unit マイクロプロセッサ
- NTRS: National Technology Roadmap for Semiconductors 米国のSIAが編集した半導体技術ロードマップ
- PIDS: Process Integration, Devices and Structures (ITRSの章の名前）
- SIA:　Semiconductor Industry Association　米国半導体工業会
- STRJ:　Semiconductor Technology Roadmap committee of Japan 半導体技術ロードマップ専門委員会。JEITA半導体部会　半導体技術委員会　の専門委員会

STRJ, ITRSの歴史と現状

1990 1998 1999 2000 2001 2002 2003 2004 2005 2006 2007

1991 MicroTech 2000 Workshop Report

1992NTRS

1994NTRS

1997NTRS

SIA Roadmap

Europe

Japan

Korea

Taiwan

USA

ITRS

1998 Update

1999 ITRS

2000 Update

2001 ITRS

2002 Update

2003 ITRS

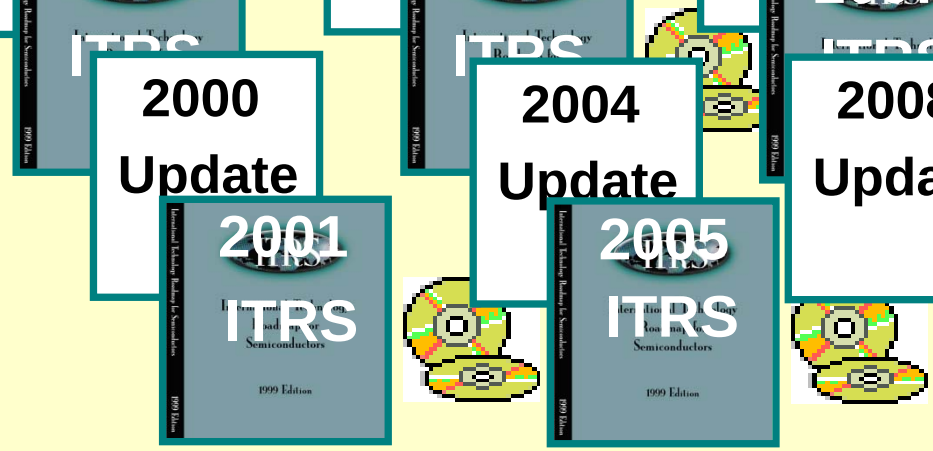
2004 Update

2005 ITRS

2006 Update

2007 ITRS

2008 Update



STRJ

1998年発足

タスクフォース、クロスカット活動

半導体産業・技術開発の経済性委員会

1999	2000	2001	2002	2003	2004	2005	2006	2007
STRJ報告	STRJ報告	STRJ報告	STRJ報告	STRJ報告	STRJ報告	STRJ報告	STRJ報告	STRJ報告

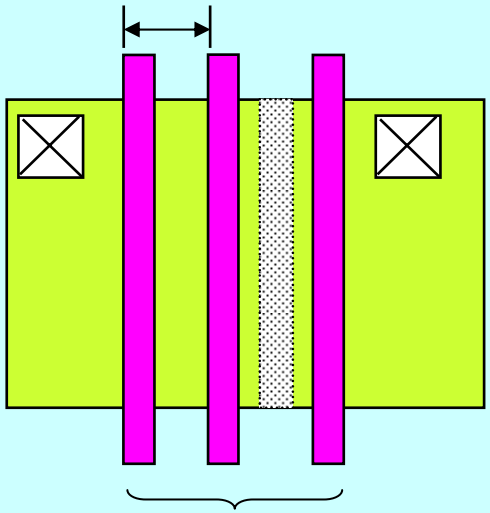
ITRS 2008 Update の概要

- 2008年の改訂は全面改訂ではなく、基本的には表の数字の見直しのみ。
- 各章ごとに改訂内容の要約を作成し、公開
- NAND Flashメモリの微細化トレンドについて議論中。微細化トレンドをさらに前倒しするかどうかがポイントであるが、今回は改訂を見送る。
- MPUとロジックLSIのMOSトランジスタの微細化トレンドを遅らせる。特に、HP（High Performance，高性能）用途のゲート長の微細化はITRS 2007年版より遅れており、2007年以降、0.7倍／3.8年のスケーリングトレンドを採用する。LOP （Low Operating Power，低動作電力）やLSTP （Low Standby Power，低スタンバイ電力）のゲート長との差は、縮まる方向。
- 上記に伴い、FD-SOI(完全空乏型のSOI基板）とFinFET（フィン型のトランジスタ）の導入時期も遅らせる
- ERD（新探究デバイス）WGでは新探究デバイスの候補を7つに絞り込み、カーボン系の材料（グラフェン、カーボンナノチューブ）を有望とする。

2007 Definition of the Half Pitch - unchanged

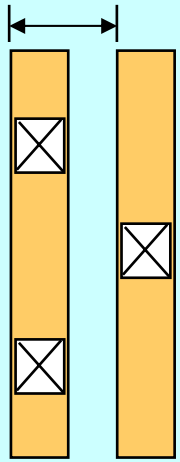
[No single-product "node" designation; DRAM half-pitch still litho driver; however, other product technology trends may be drivers on individual TWG tables]

FLASH Poly Silicon ½ Pitch
= Flash Poly Pitch/2



Typical flash
Un-contacted Poly

DRAM ½ Pitch
= DRAM Metal Pitch/2
MPU/ASIC M1 ½ Pitch
= MPU/ASIC M1 Pitch/2

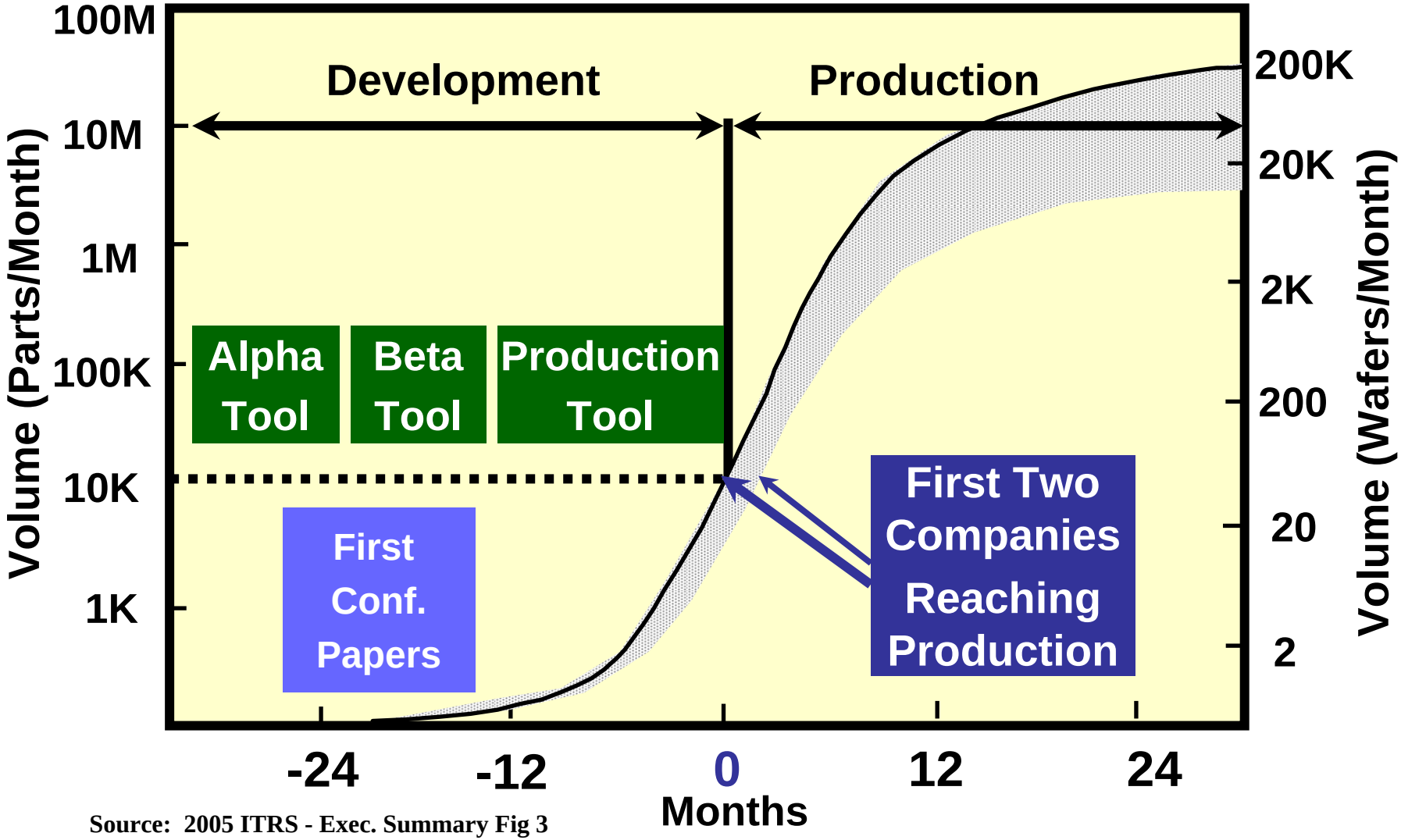


Typical DRAM/MPU/ASIC
Metal Bit Line

Source: 2005 ITRS - Exec. Summary Fig 2

Fig 3

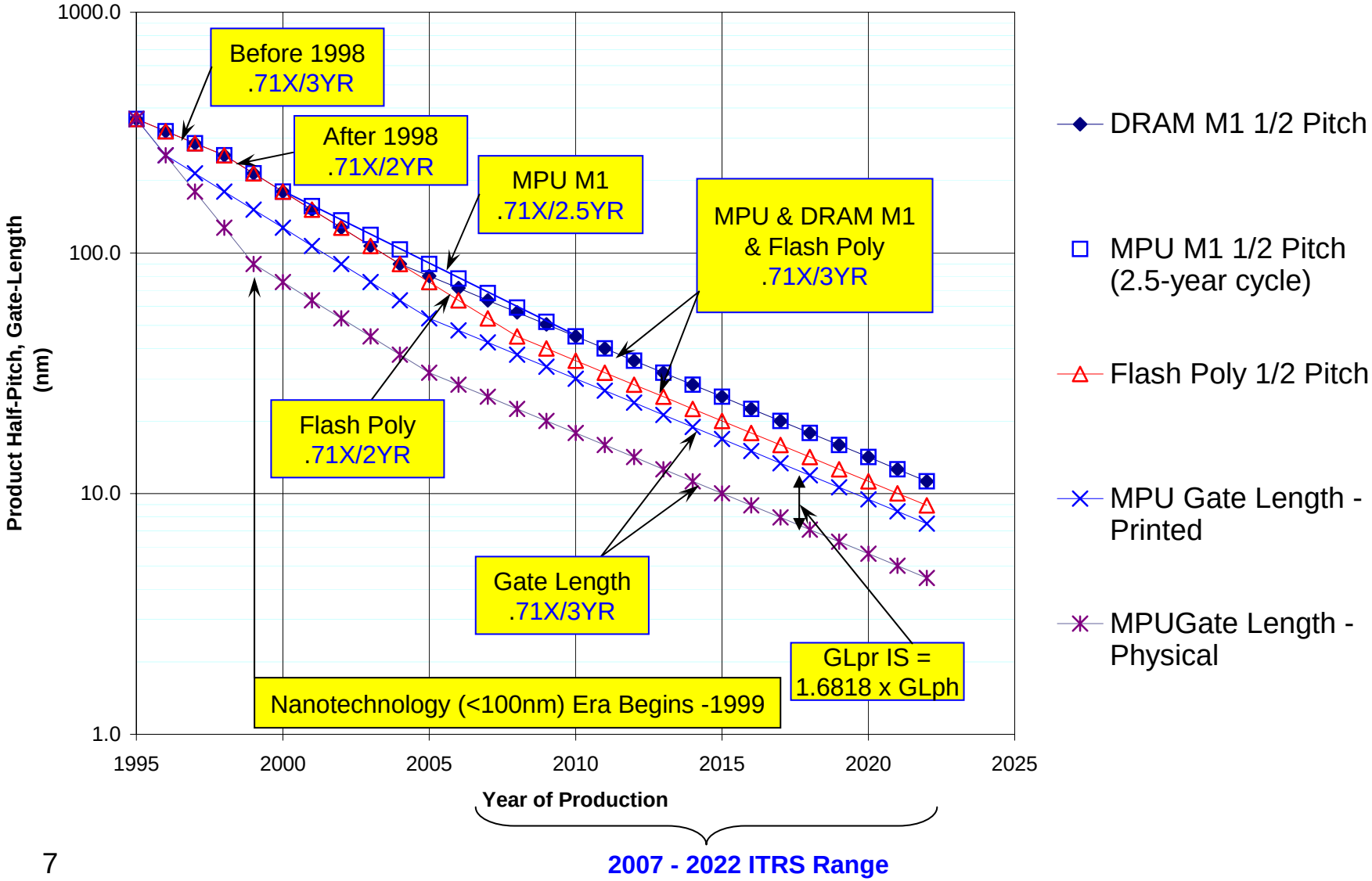
Production Ramp-up Model and Technology Cycle Timing

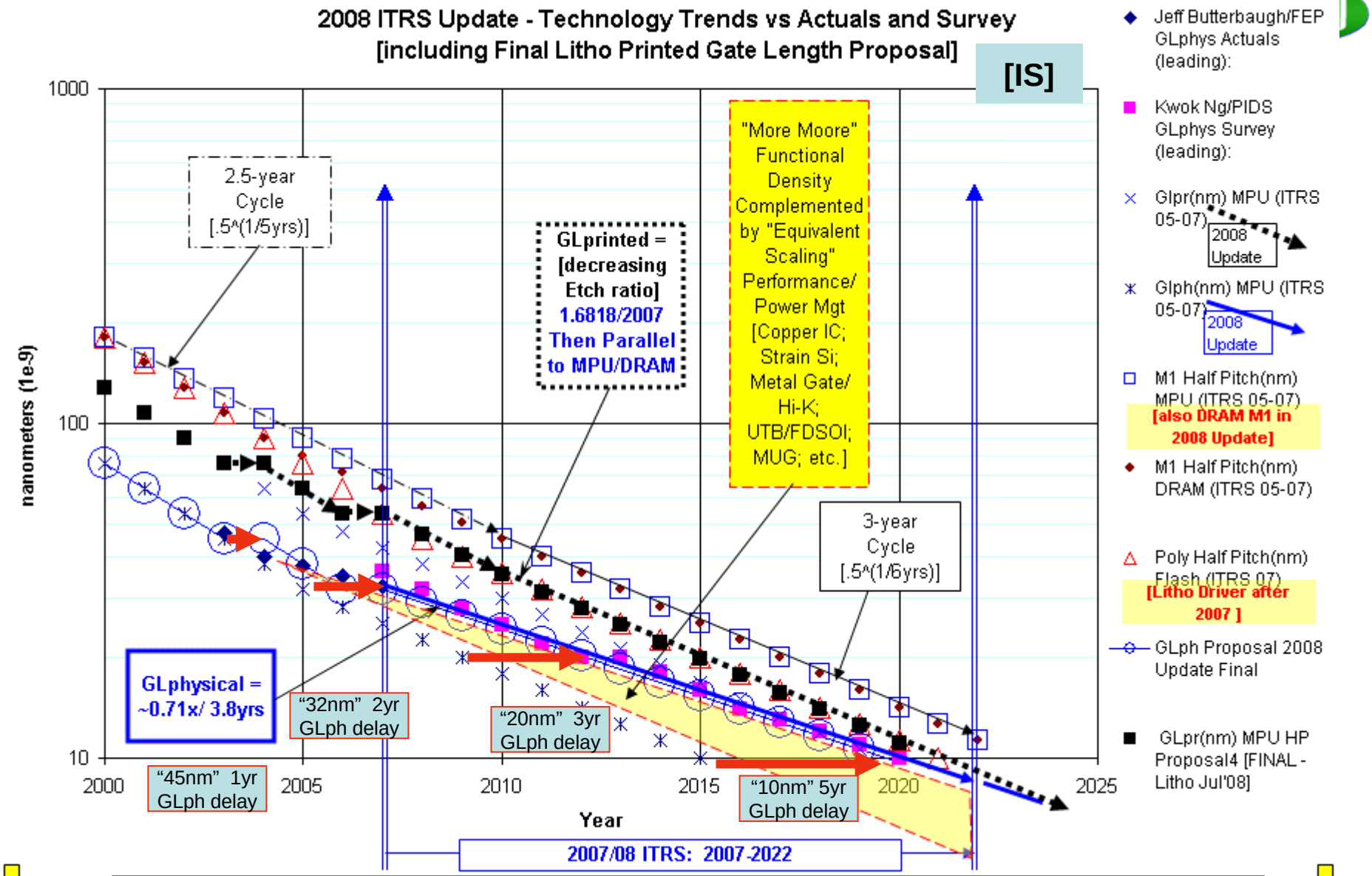


Source: 2005 ITRS - Exec. Summary Fig 3

2007 ITRS Product Technology Trends - Half-Pitch, Gate-Length

[WAS]





- GLphysical 2008 Update IS: 3.8yr cycle after 2007; enabled by "Equiv. Scaling"
- FEP and PIDS have proposed shifted/interpolated tables; full model redo in '09
- GLprinted parallel to MPU/DRAM M1 Half-Pitch; shrinking etch ratio to GLphy

Figure 9['07] ITRS Product Function Size

2008 Update:
[NO CHANGE to MPU and Flash; Small change '07-'09 to DRAM]

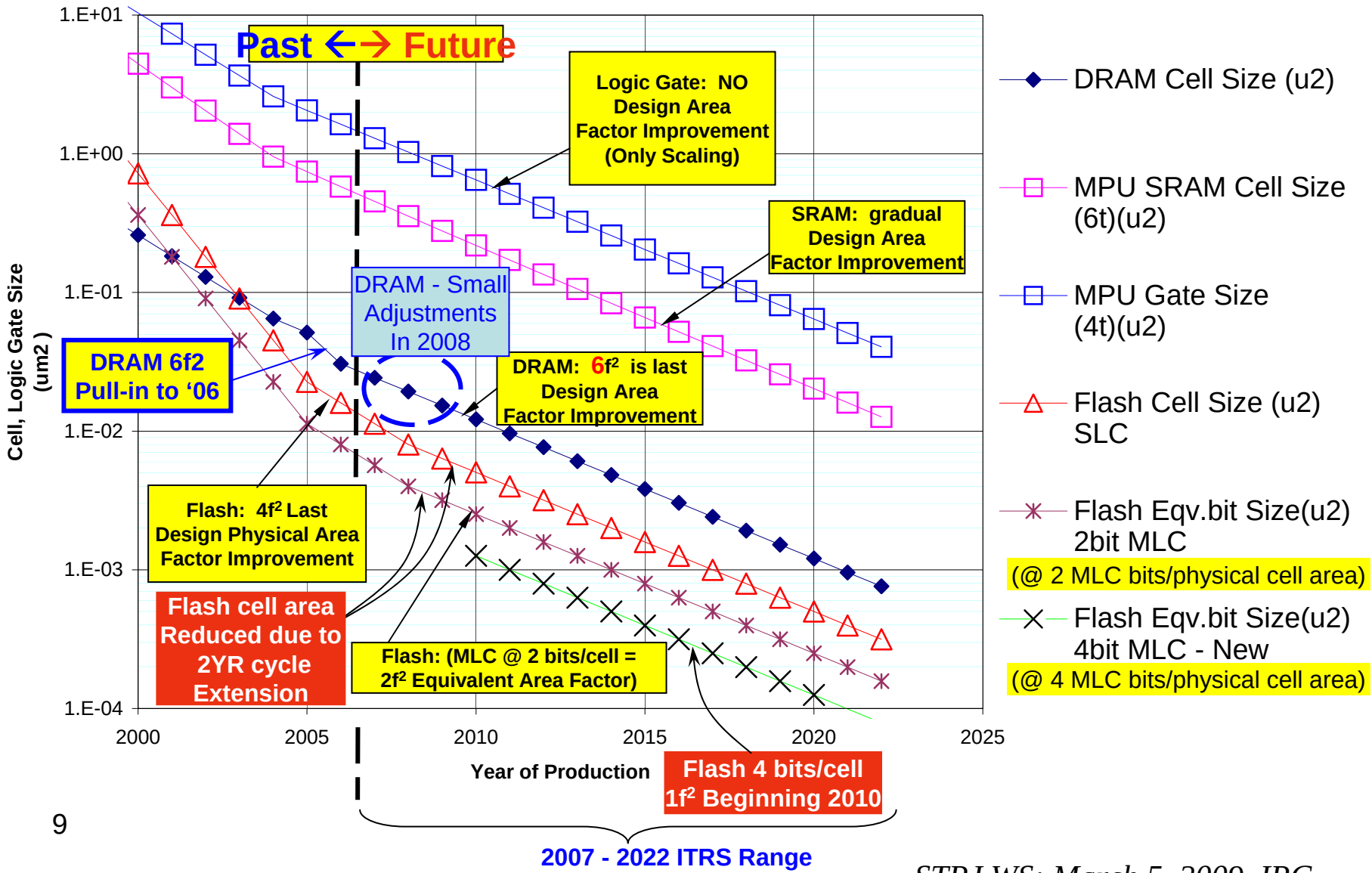
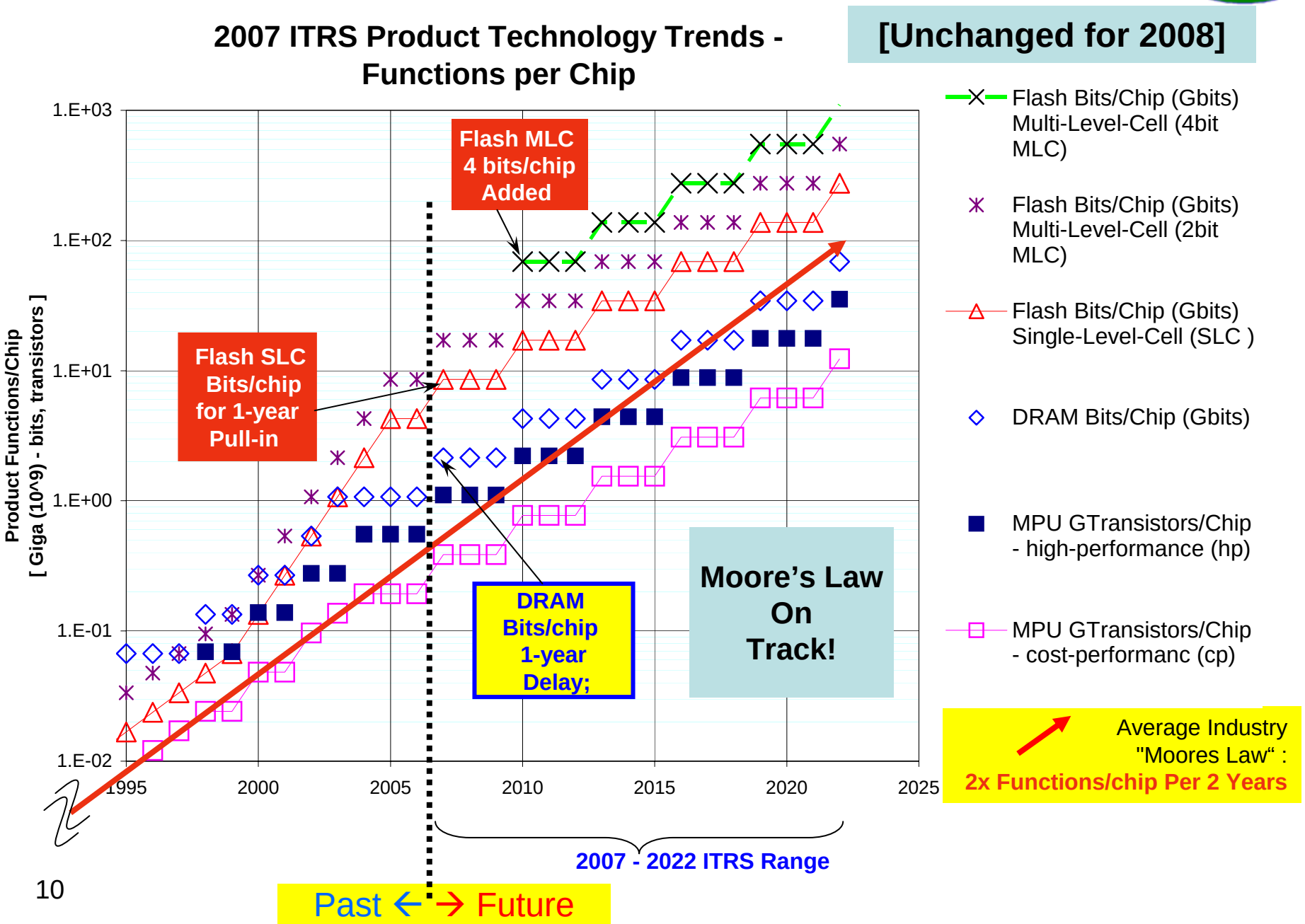
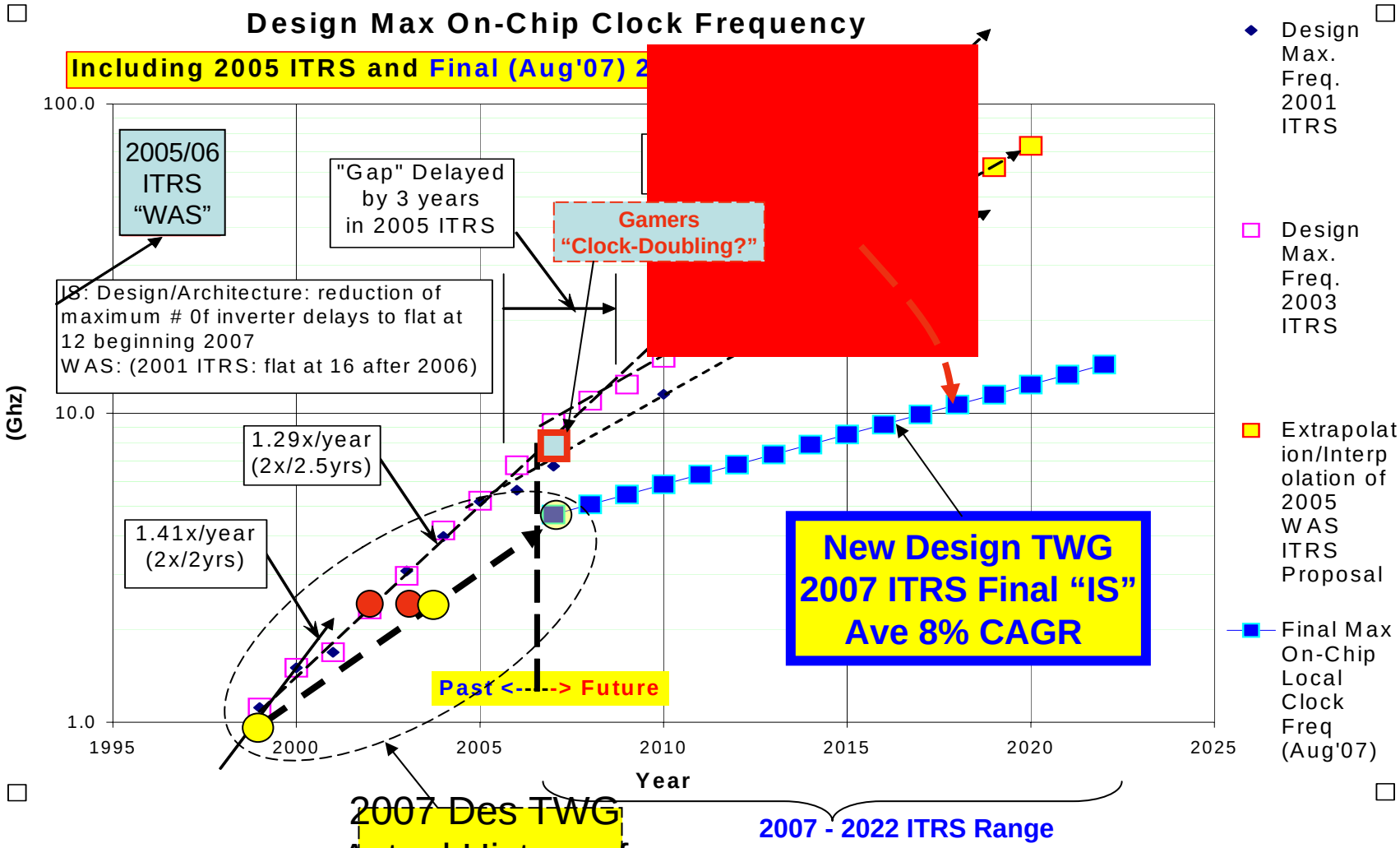


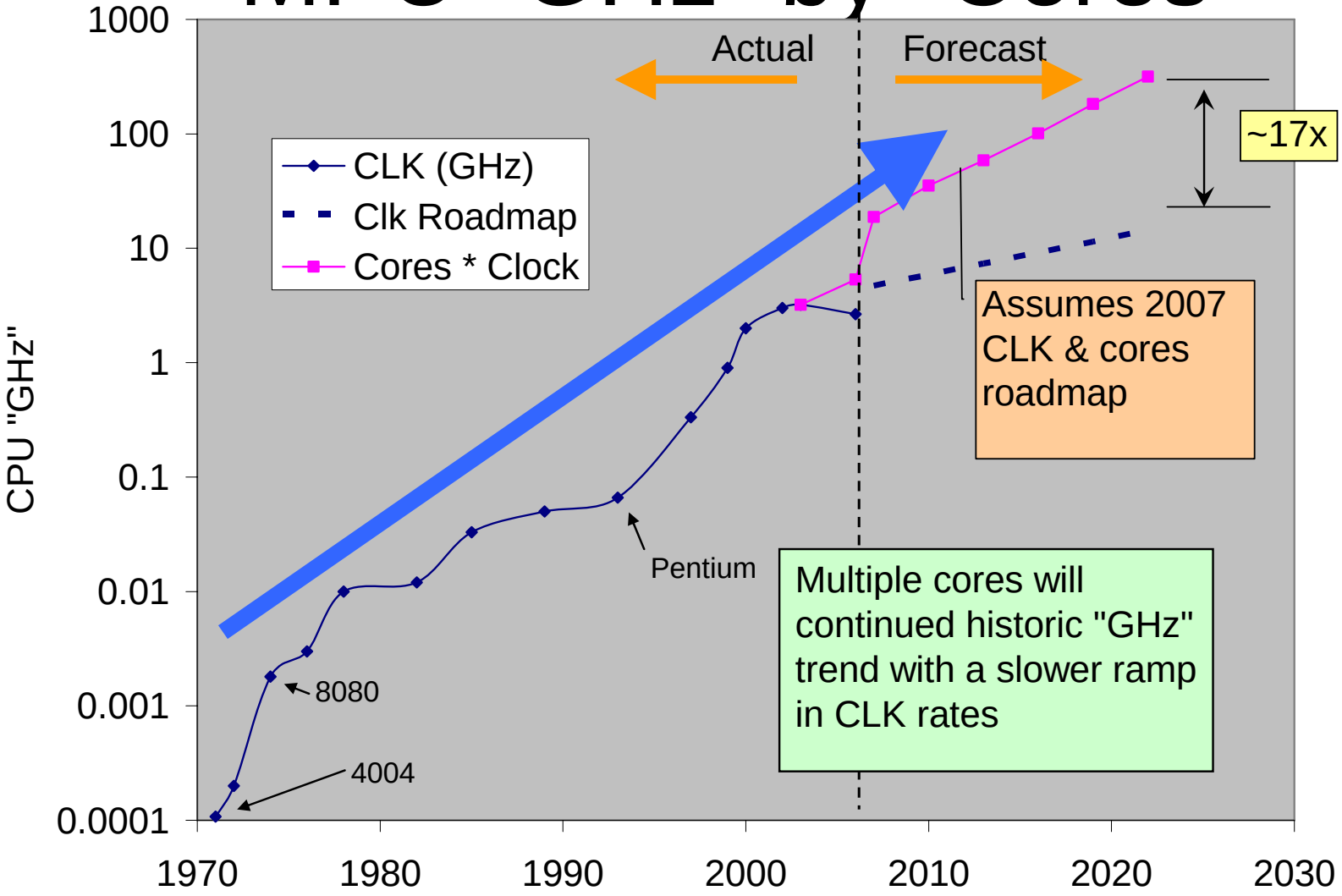
Figure 10 ITRS Product Functions per Chip



Performance and Power Management Enabled by "Equivalent Scaling"

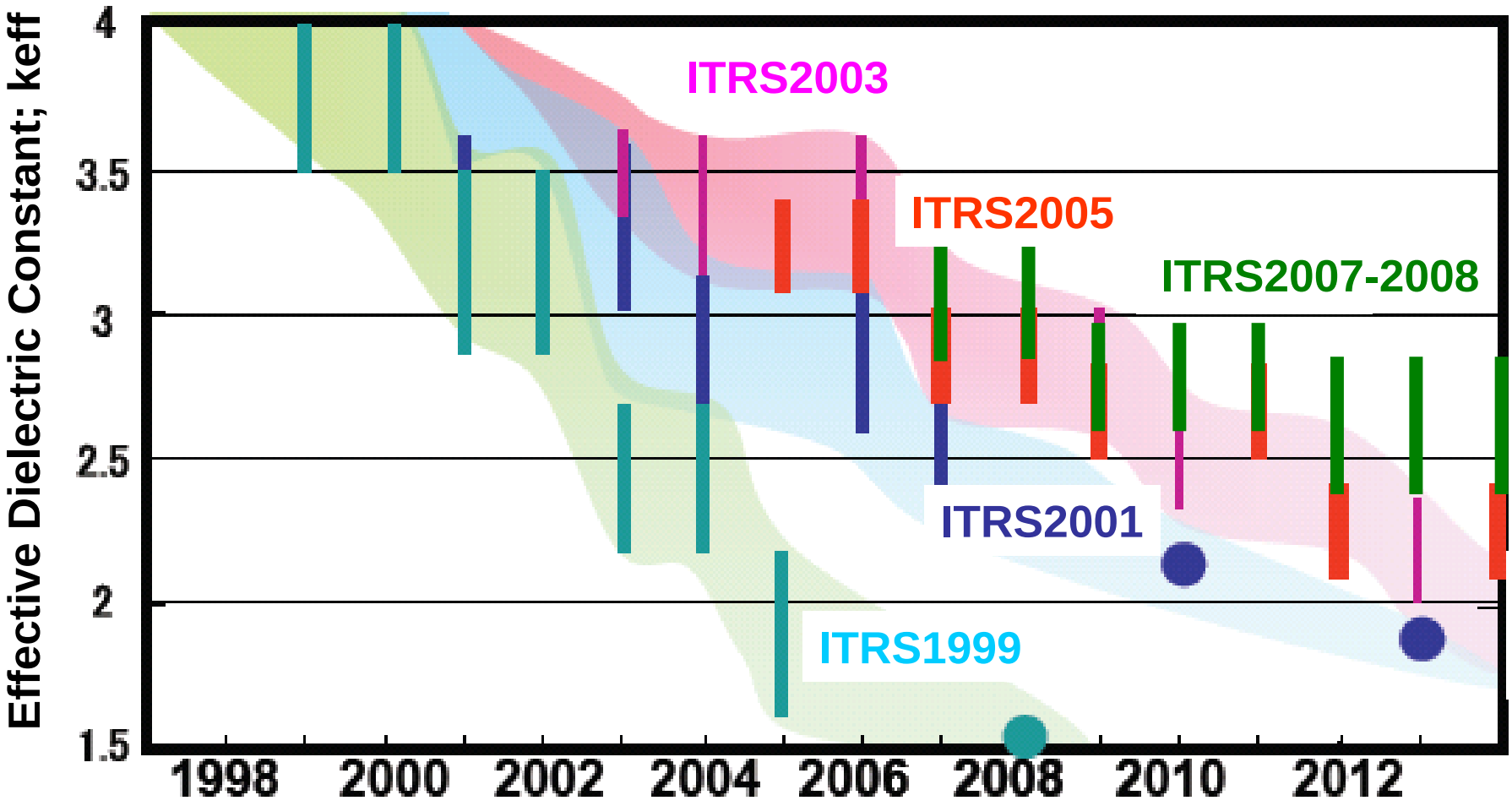


MPU “GHz” by “Cores”



Source: ITRS Public Conference in Seoul, Dec. 2008

ITRS Low-k Roadmap



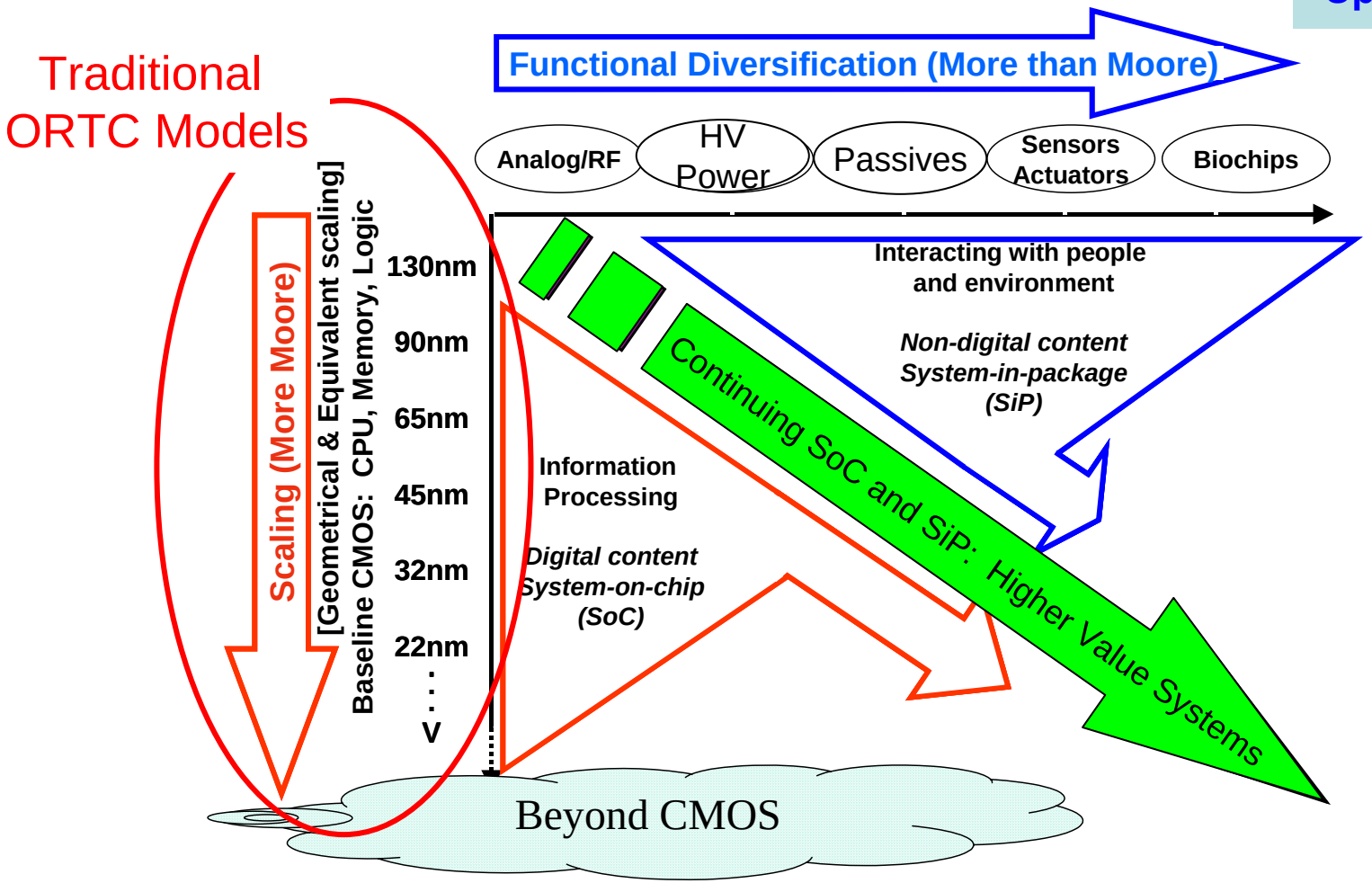
Source: ITRS Public Conference in Seoul, Dec. 2008

2007 ITRS Executive Summary Fig 5

[updated for 2007]

Moore's Law & More

[2007 – add Definitions; Update Graphic]



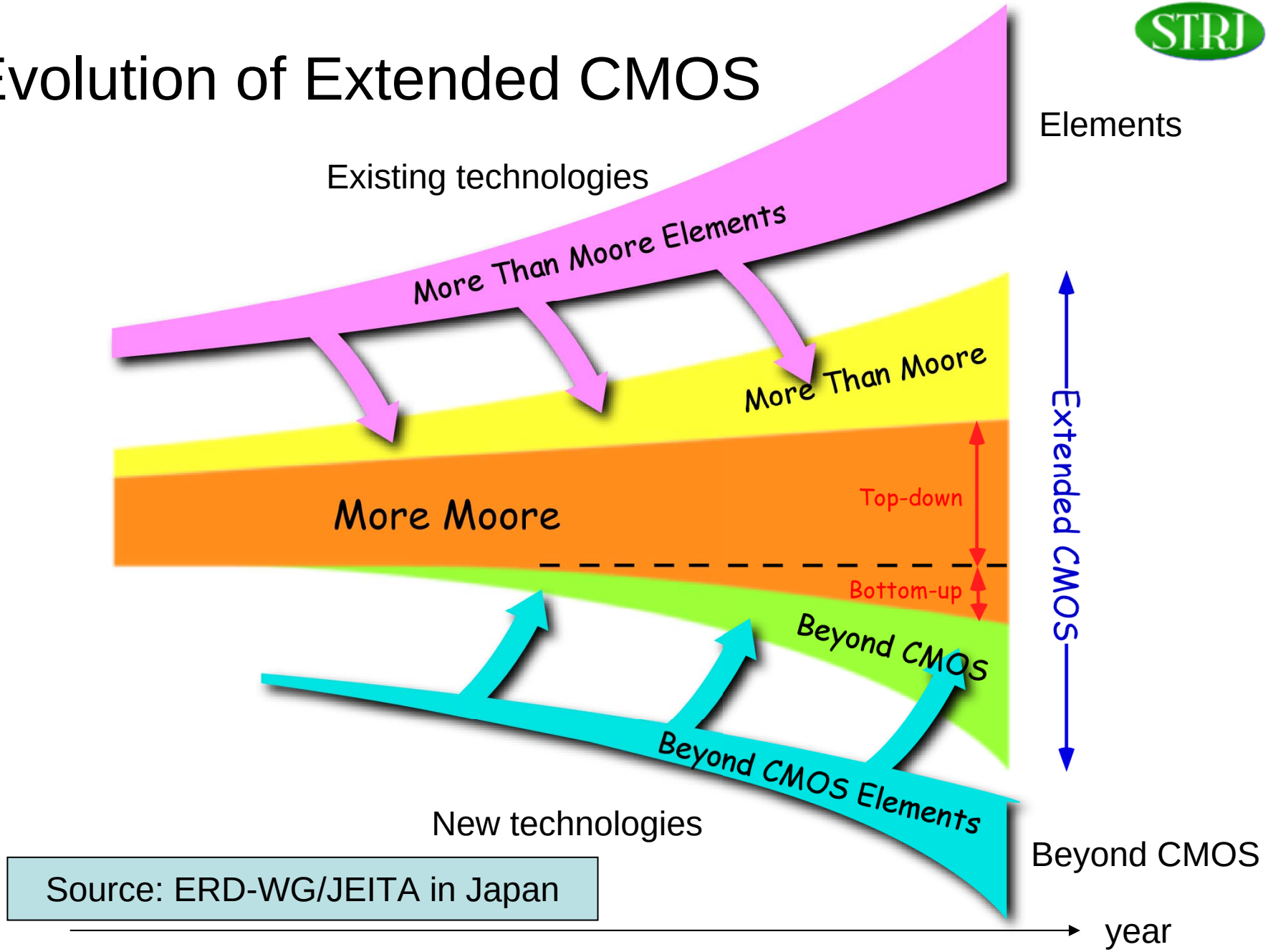
2007 ITRS Definitions: "More Moore" and "More than Moore"

1. **Scaling ("More Moore")**
   a. **Geometrical (constant field) Scaling** refers to the continued shrinking of horizontal and vertical physical feature sizes of the on-chip logic and memory storage functions in order to improve density (cost per function reduction) and performance (speed, power) and reliability values to the applications and end customers.
   b. **Equivalent Scaling** which occurs in conjunction with, and also enables, continued Geometrical Scaling, refers to 3-dimensional device structure ("Design Factor") Improvements plus other non-geometrical process techniques and new materials that affect the electrical performance of the chip.

2. **Functional Diversification ("More than Moore")**

   Functional Diversification refers to the incorporation into devices of functionalities that do not necessarily scale according to "Moore's Law," but provide additional value to the end customer in different ways. The "More-than-Moore" approach typically allows for the non-digital functionalities (*e.g.* RF communication, power control, passive components, sensors, actuators) **to migrate from the system board-level** into a particular package-level (SiP) or chip-level (SoC) potential solution.

Evolution of Extended CMOS



Source: ERD-WG/JEITA in Japan

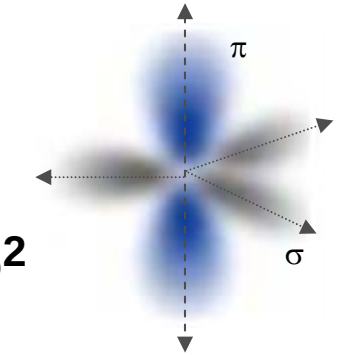
ERD（新探究デバイス）の7候補（2009年版に反映予定）

委員の投票の結果ではCarbon-based Nanoelectronicsが1位

- Nano-electro Mechanical Switches
- Collective Spin Devices
- Spin Torque Transfer Devices
- Atomic Switch / Electrochemical Metallization
- Carbon-based Nanoelectronics
- Single Electron Transistors
- CMOL / Field Programmable Nanowire Interconnect (FPNI)

SP^2 Carbon: 0-Dim. to 3-Dim.

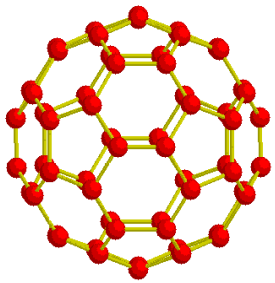
（炭素原子sp^2混成軌道が作る構造： 0次元から3次元まで）



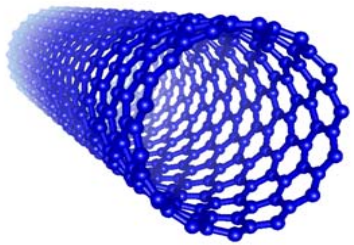
Atomic orbital sp^2

0D 1D 2D 3D

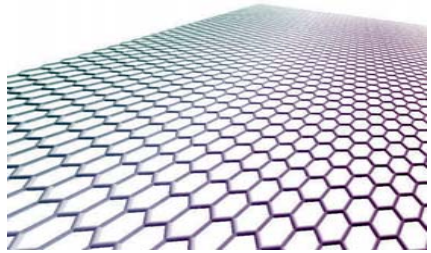
Fullerenes (C_{60})



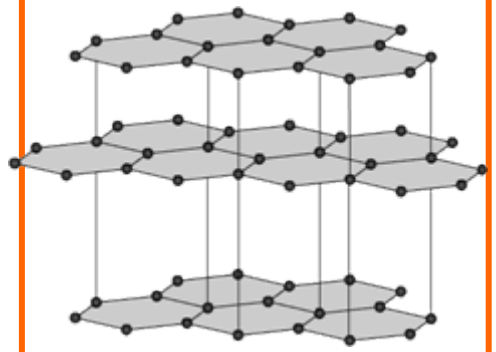
Carbon Nanotubes



Graphene



Graphite



関連webサイトのURL

さらに詳しい資料については下記を参照願います

- ITRSの公式ホームページ
  - http://www.itrs.net/ または　http://public.itrs.net/
  - ITRS 2008 Update，ITRS　2007　Editionはじめ、ITRSの最新情報
- JEITAのロードマップのホームページ
  - http://strj-jeita.elisasp.net/strj/index.htm
  - ITRS 2007の日本語訳（過去の版の和訳もあり）
  - ITRSの過去の版（英文）へのリンク
  - STRJ（半導体技術ロードマップ専門委員会）の活動情報