WG5(リソグラフィ)活動報告

「先端リソグラフィ技術　－　現状と課題　－」

株式会社東芝

東川　巌

内容

- WG5(リソグラフィ)の体制と2008年度の活動状況
- ITRS2008 Lithography章の概要
- リソグラフィ技術の現状と課題
- ITRS2009 Lithography章の指針
- まとめ

略語説明

NA	Numerical Aperture
CD	Critical Dimension, CDU (CD Uniformity)
DOF	Depth of Focus
LER/LWR	Line Edge Roughness/Line Width Roughness
RET	Resolution Enhancement Techniques
OAI	Off-Axis Illumination
PSM	Phase Shifting Mask, cPSM (complementary PSM), APSM (Alternating PSM), EPSM (Embedded PSM), Att. PSM (Attenuated PSM)
EDA	Electronic Design Automation
OPC	Optical Proximity Corrections, RB/MBOPC (Rule Base/Model Base OPC)
DFM	Design for Manufacturing/Design for Manufacturability
SB/SRAF	Scattering Bar/Sub Resolution Assist Feature™
MEEF	Mask Error Enhancement Factor (=MEF)
ARC	Anti-Reflection Coating, BARC (Bottom ARC), TARC (Top ARC)
AMC	Airborne Molecular Contamination
DE/DP/SADP	Double Exposure/Double Patterning/Self Aligned DP
ESD	Electro Static Discharge
NGL	Next Generation Lithography
EUVL	Extreme Ultraviolet Lithography
ML2	Maskless Lithography
NIL	NanoImprint Lithography, UV-NIL (Ultraviolet NIL), SFIL (Step & Flash Imprint Lithography)
DSA	Directed Self Assembly

活動体制
WG5メンバー

－ JEITA半導体部会/関連会社 －

東川 巌/リーダー (東芝)
内山 貴之/サブリーダー (NECEL)
羽入 勇 (富士通マイクロエレクトロニクス)
⇔ 安部 直道
須向 一行 (ルネサステクノロジ)
笹子 勝 (パナソニック)
守屋 茂 (ソニー)
田口 隆 (ローム/沖セミコンダクター)
和田 恵治 (ローム)
田中 秀仁 (シャープ)
岡崎 信次 (日立製作所)
山口 敦子 (日立製作所)

－ コンソーシアム －

山部 正樹/事務局 (ASET-D2I)
寺澤 恒男 (Selete)
笠間 邦彦 (EUVA)

－ 大学・独立行政法人 －

戸所 義博 (奈良先端大)

－ SEAJ、他 －

森 晋 (SEAJ: ニコン)
山田 雄一 (SEAJ: キヤノン)
中島 英男 (SEAJ: TEL) ⇐ 山口 忠之
山口 哲男 (SEAJ: ニューフレアテクノロジィ)
龜山 雅臣/国際担当 (ニコン)
大久保 靖 (HOYA)
林 直也 (大日本印刷)
外岡 要治 (凸版印刷) ⇐ 奥田 能充
小野寺 純一 (東京応化工業)
栗原 啓志郎 (アライアンスコア)　　計　25名

2008 Lithography Technology Requirements

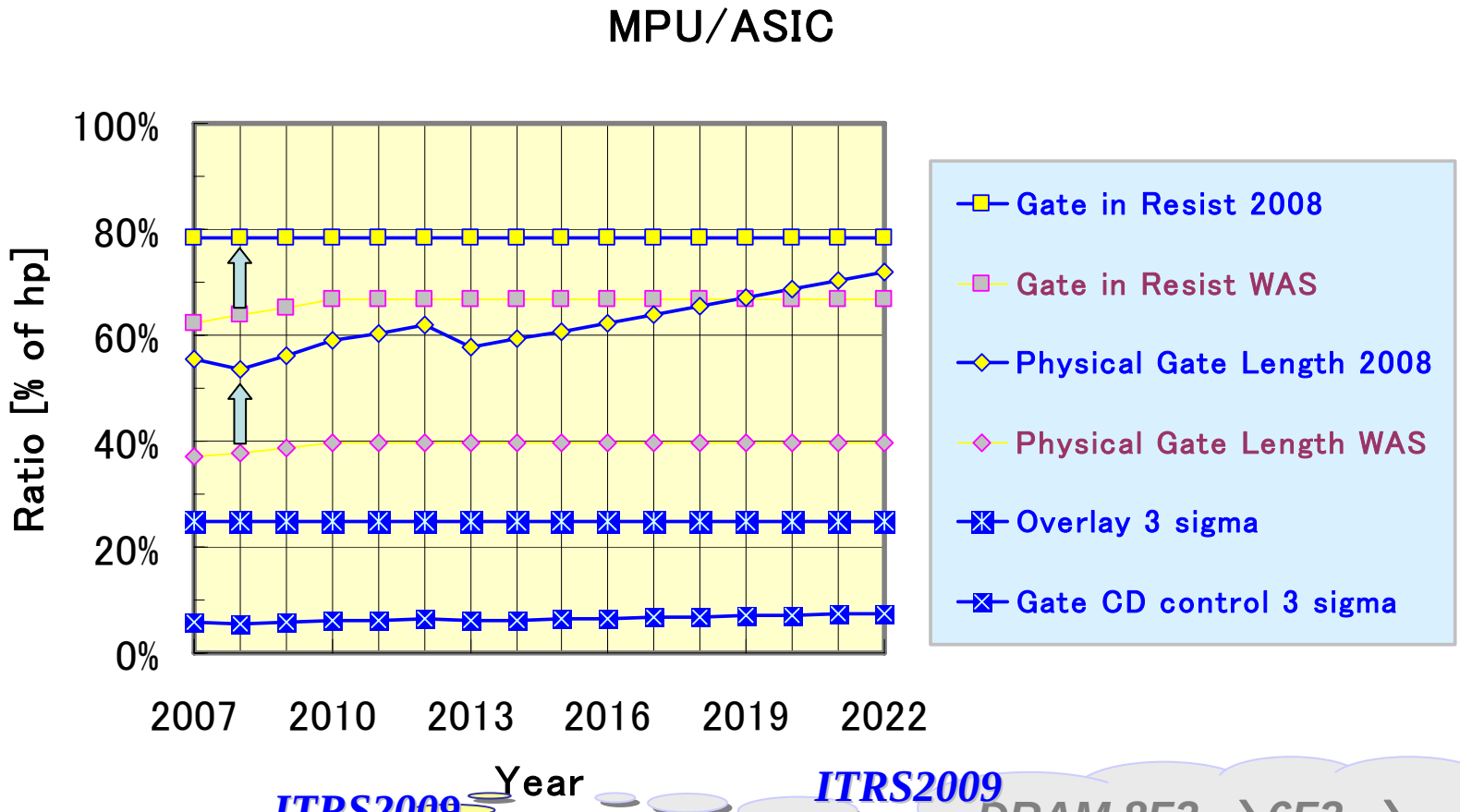
DRAM

FLASH

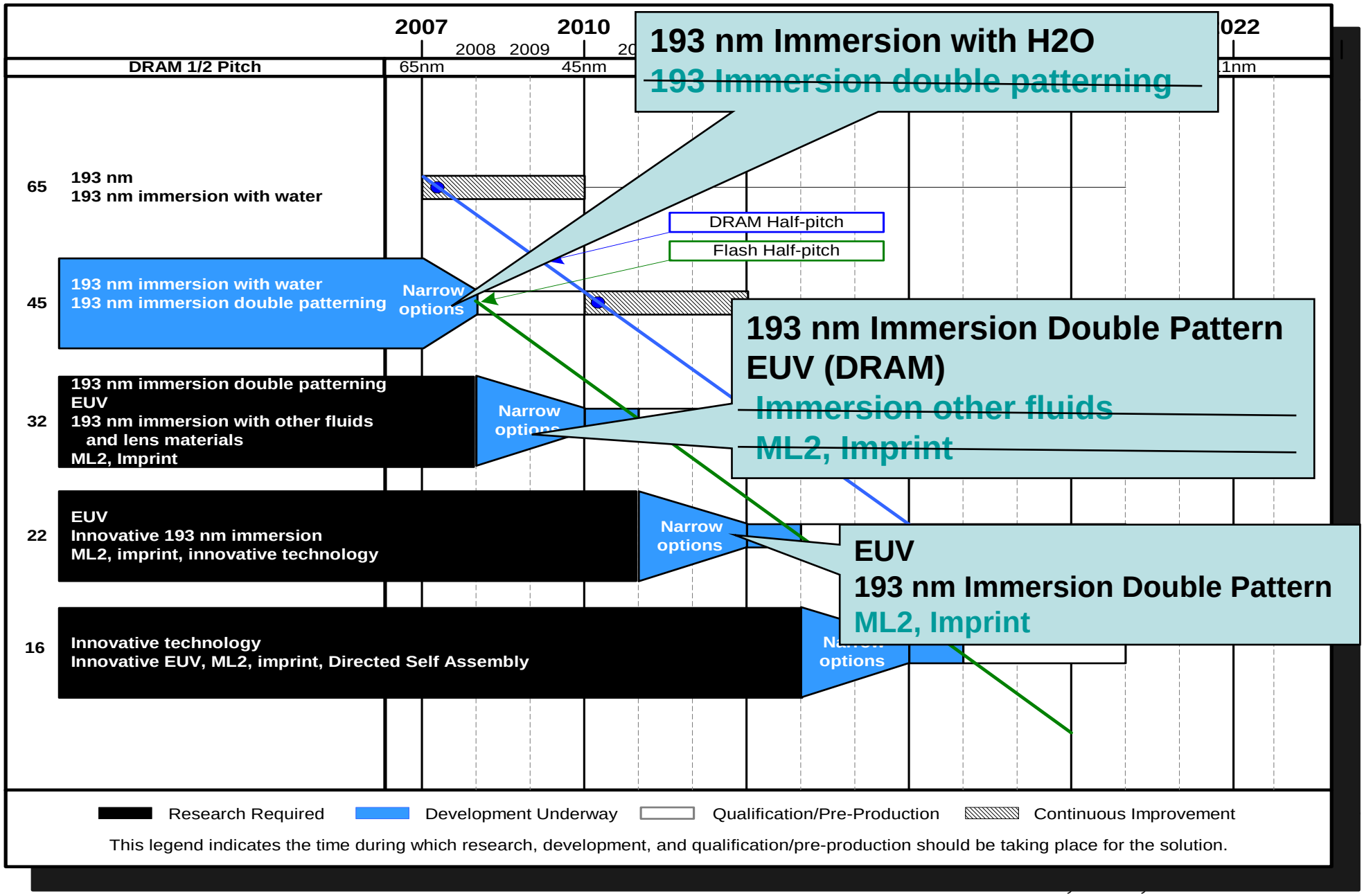
MPU

ORTC INDEX / ITWG INDEX	Table LITH3a&b Lithography Technology Re ars								
	Year of Production	2007	2008	2009	2010	2011	2012	2013	2014	2015
IS	DRAM ½ pitch (nm) (contacted)	68	59	52	45	40	36	32	28	25
	DRAM									
IS	DRAM ½ pitch (nm)	68	59	52	45	40	36	32	28	25
IS	CD control (3 sigma) (nm) [B]	7.1	6.2	5.4	4.7	4.2	3.7	3.3	2.9	2.6
IS	Contact in resist (nm)			7	50	44	39	35	31	28
IS	Contact after etch (nm)			2	45	40	36	32	28	25
IS	Overlay [A] (3 sigma) (nm)			.3	9.0	8.0	7.1	6.4	5.7	5.1
	Flash									
IS	Flash ½ pitch (nm) (un-contacted poly)	54	45	40	36	32	28	25	22	20
IS	CD control (3 sigma) (nm) [B]	5.6	4.7	4.2	3.7	3.3	2.9	2.6	2.3	2.1
IS	Contact in resist (nm)	59	49	44	39	35	31	28	25	22
IS	Contact after etch (nm)			0	36	32	28	25	22	20
IS	Overlay [A] (3 sigma) (nm)			.2	11.8	10.5	9.4	8.3	7.4	6.6
	MPU									
IS	MPU/ASIC Metal 1 (M1) ½ pitch (nm)	68	59	52	45	40	36	32	28	25
WAS	MPU gate in resist (nm)	42	38	34	30	27	24	21	19	17
IS	MPU gate in resist (nm)	54	47	41	35	31	28	25	22	20
WAS	MPU physical gate length (nm) *	25	23	20	18	16	14	13	11	10
IS	MPU physical gate length (nm) *	32	29	27	24	22	20	18	17	15.3
IS	Gate CD control (3 sigma) (nm) [B] **	3.3	3.0	2.8	2.5	2.3	2.1	1.9	1.7	1.6
IS	Contact in resist (nm)	84	73	64	56	50	44	39	35	31
IS	Contact after etch (nm)	77	67	58	51	45	40	36	32	28
IS	Overlay [A] (3 sigma) (nm)	17	15	13	11	10.0	8.9	8.0	7.1	6.3
	Chip size (mm^2)									
	Maximum exposure field height (mm)	26	26	26	26	26	26	26	26	26
	Maximum exposure field length (mm)	33	33	33	33	33	33	33	33	33

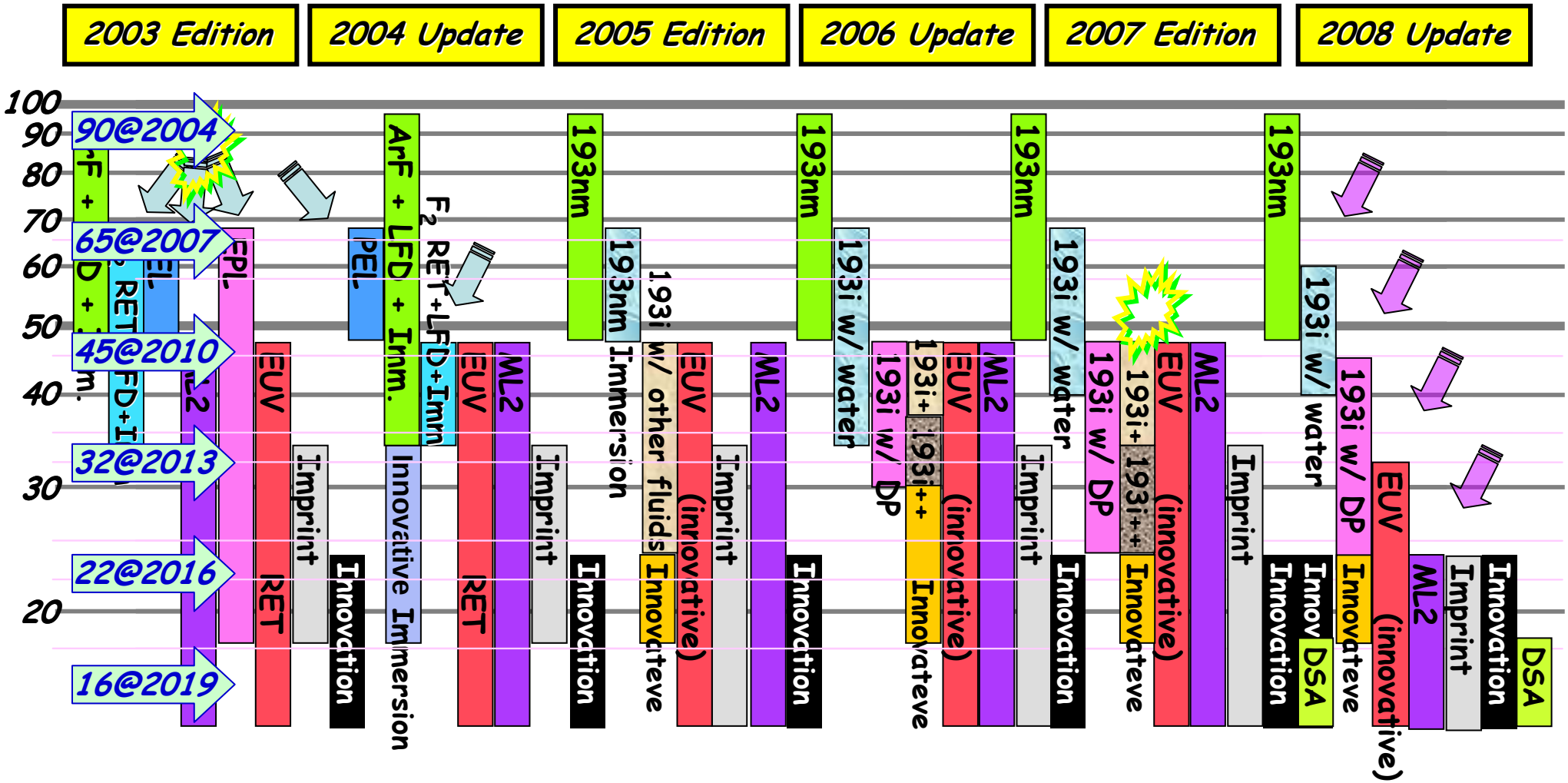
2008 update
- MPU/ASIC -



Potential Solutions 2008 – 2009



Potential Solutions



Potential Solutions

- ArF Immersion Single Exposure
- **ArF Extension: Pitch Splitting(DPT), Spacer**
- **EUVL**
- **ML2**
- **NIL**
- **DSA & Others**

Optical lithography extension

$$R = k_1 \frac{\lambda}{NA}$$

193nm/ArF Single Exposureの限界　NA=1.35 → hp 38~39nm (L&S)

Year of Production		2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
DRAM ½ pitch (nm)		68	59	52	45	40	36	32	28	25	22.5	20	17.9	15.9	14.2
Flash ½ pitch (nm) (un-contacted poly)		54	45	40	36	32	28	25	22	20	17.9	15.9	14.2	12.6	11.3
Flash ASML presentation		45		32		22		16		11					
	NA				k1										
ArF Dry	0.75	0.25													
	0.85	0.29	0.25												
	0.93	0.31	0.27	0.24											
ArF Water Immersion	1.2	0.4	0.35	0.31	0.28	0.25									
	1.3	0.44	0.38	0.34	0.3	0.27	0.24	0.21							
DRAM	1.35	0.45	0.4	0.35	0.31	0.28	0.25	0.22	0.2	0.18	0.16	0.14	0.12	0.11	
Flash	1.35	0.37	0.31	0.28	0.25	0.22	0.2	0.18	0.15	0.14	0.12	0.11	0.1	0.09	
ArF High Index Immersion	1.45	0.49	0.43	0.38	0.34	0.3	0.27	0.24							
	1.55		0.46	0.4	0.36	0.32	0.29	0.26							
	1.7		0.5	0.44	0.4	0.35	0.31	0.28	0.25						
EUVL	0.25		1.05	0.93	0.83	0.74	0.66	0.59	0.52	0.47	0.42	0.37	0.33	0.29	0.26
	0.32						0.85	0.75	0.67	0.6	0.53	0.48	0.42	0.38	0.34
	0.45								0.94	0.84	0.75	0.67	0.6	0.53	0.47

OPC evolution

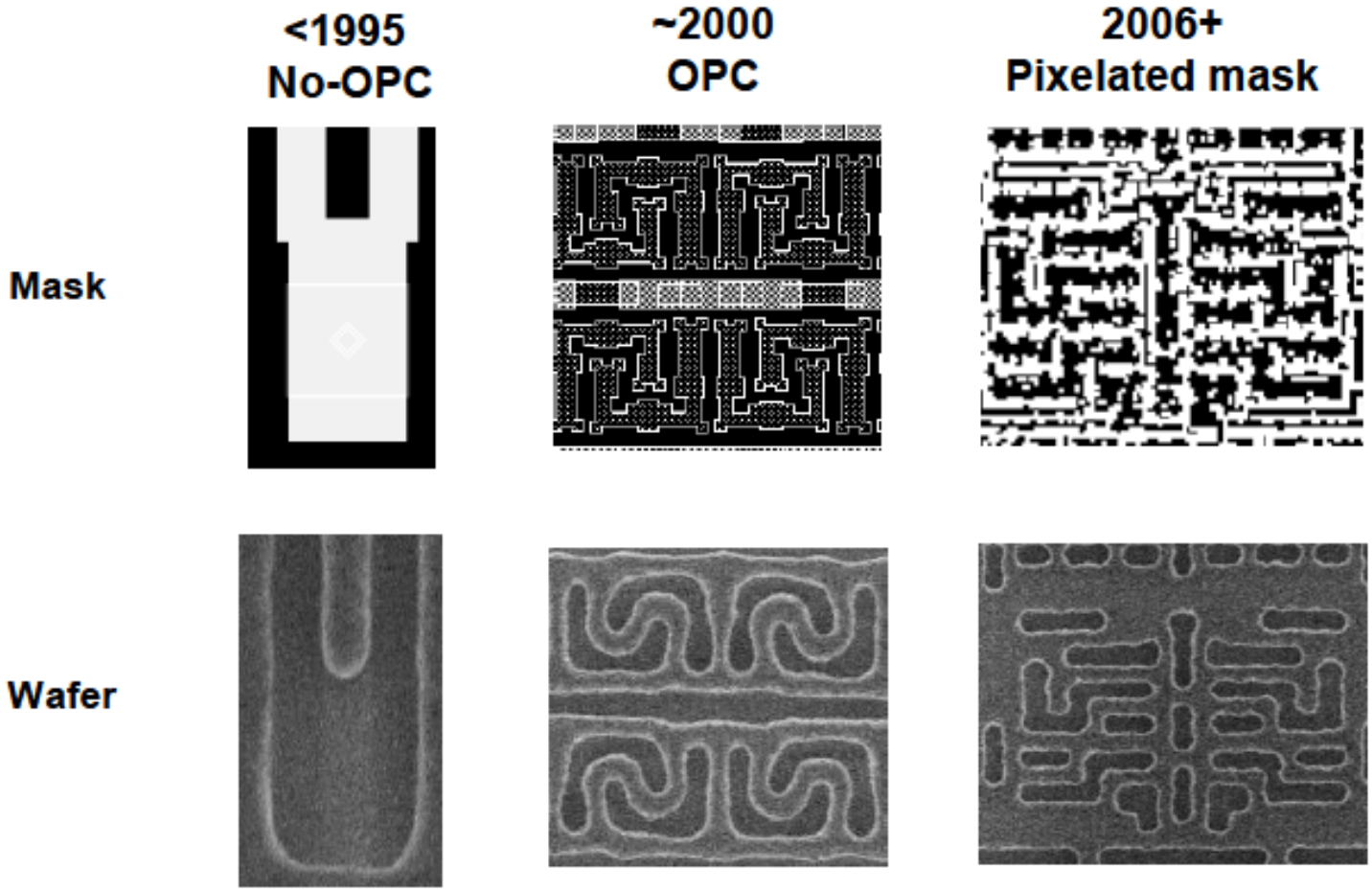


Figure 1. OPC evolution.

"Fabrication of defect-free full-field pixelated phase mask"
Wen-Hao Cheng*, Jeff Farnsworth, Wai Kwok, Andrew Jamieson, Nathan Wilcox, Matt Vernon*, Karmen Yung, Yi-Ping Liu, Jun Kim, Eric Frendberg, Scott, Proc. of SPIE Vol. 6924, 69241G, (2008)

k1<0.25

Pitch Splitting = Mask Splitting
Spacer (Self Aligned DP (SADP))

- k1 - 0.35 0.30 0.25 0.2 0.15 0.1

Single Exposure RET

hp 38~39 nm

k1< 0.25

- Current DP -

- Alt.PSM + Trim
- DDL_x + DDL_y
- Tip to Tip
- Cross Point

- Post Process -

- Resist slimming
- Contact shrink

- Mask -

- Inverse Litho.
- CL, Pixelated Phase Mask

Pitch doubling

DP

DE

Spacer

Triple ?

Triple ? Quadruple ?

Double Spacer ?

DP: LELE, LFLE (Resist freeze)

DE: Double Exposure
Magic_material (ex. Ultra_CEL)

Spacer = SADP (Self Aligned DP)

DPT Technical Issues

- Overlay、CDU、CD MTT
- Process Complexity
- Cycle time/TAT
- RDR、Area Penalty, Pitch walking
- Mask Spec. & Design
  - Data Splitting/Cutting/Coloring、OPC+SRAF
  - CDU, Image Placement, Overlay
- New Equipments/Materials
- Metrology Tool & Methodology
- Yield
- CoO、Cost

Position of the line edges

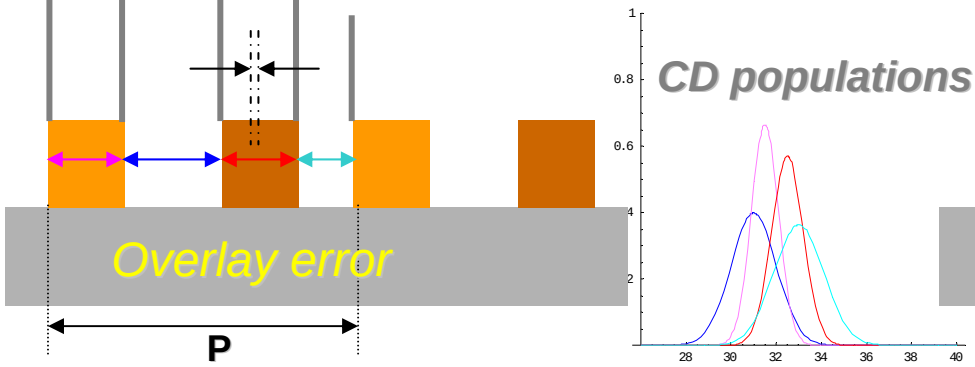
edge_1=OL_1 – line_1/2

edge_2=OL_1 + line_1/2

edge_3=P/2 + OL_2 – line_2/2

edge_4=P/2 + OL_2 + line_2/2

edge_5=P + OL_1 – line_1/2



Pitch splitting

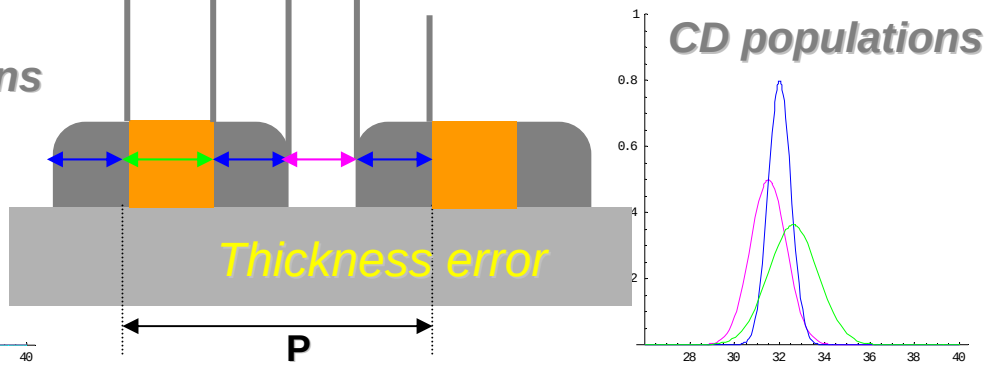
edge_1=OL – resist/2

edge_2=OL + resist/2

edge_3=OL + resist/2 + depo

edge_4=P + OL - resist/2 - depo

edge_5=P + OL – resist/2



Spacer

2008 Lithography Technology Requirements

ORTC INDEX / ITWG INDEX	Table LITH3a&b Lithography Technology Requirements—Near-term Years								
	Year of Production	2007	2008	2009	2010	2011	2013	2014	2015
IS	DRAM ½ pitch (nm) (contacted)	68	59	52	45	40	36	32	28	25
	DRAM									
IS	DRAM ½ pitch (nm)	68	59				36	32	28	25
IS	CD control (3 sigma) (nm) [B]	7.1	6.2					3.3	2.9	2.6
IS	Contact in resist (nm)	75	65				39	35	31	28
IS	Contact after etch (nm)	68	59	52	45	40		32	28	25
IS	Overlay [A] (3 sigma) (nm)	13.6	11.9	10.3	9.0	8.0	7.1	6.4	5.7	5.1
	Flash									
IS	Flash ½ pitch (nm) (un-contacted poly)	54	45	40	36	32	28			
IS	CD control (3 sigma) (nm) [B]	5.6	4.7	4.2	3.7	3.3	2.9			
IS	Contact in resist (nm)	59	49	44	39	35	31			
IS	Contact after etch (nm)	54	45	40	36	32	28			
IS	Overlay [A] (3 sigma) (nm)	17.7						8.3	7.4	6.6
	MPU									
IS	MPU/ASIC Metal 1 (M1) ½ pitch (nm)									25
WAS	MPU gate in resist (nm)									17
IS	MPU gate in resist (nm)							25	22	20
WAS	MPU physical gate length (nm) *						14	13	11	10
IS	MPU physical gate length (nm) *						20	18	17	15.3
IS	Gate CD control (3 sigma) (nm) [B] **	3.3	3.0		2.5	2.3	2.1	1.9	1.7	1.6
IS	Contact in resist (nm)	84	73	64	56	50	44	39	35	31
IS	Contact after etch (nm)	77	67	58	51	45	40	36	32	28
IS	Overlay [A] (3 sigma) (nm)	17	15	13	11	10.0	8.9	8.0	7.1	6.3
	Chip size (mm^2)									
	Maximum exposure field height (mm)	26	26	26	26	26	26	26	26	26
	Maximum exposure field length (mm)	33	33	33	33	33	33	33	33	33

2013
32 nm SE

CDU 3.3 nm
OL 3s 6.4 nm

CDU 2.5 nm
&
OL 3s 2.3 nm

Pitch splitting

Process wafer vs. Single wafer

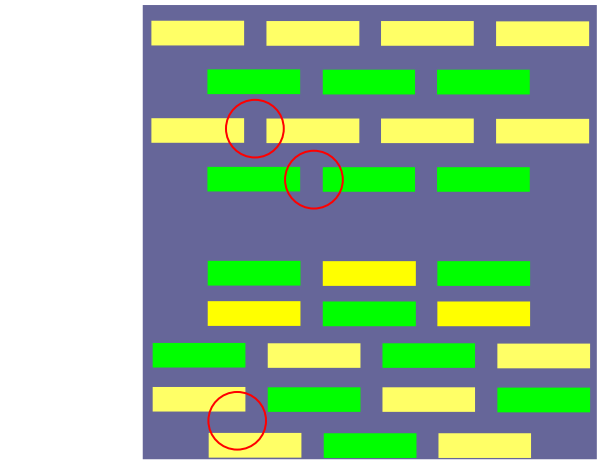
Overlay Challenge !!

2008 Update Mask Requirements (DE/DP)

Optical Mask Requirements [nm]	2007 *65*	2010 *45*	2013 *32*	
Image Placement (Single Exposure)	8.2	5.4	3.8	*1 node*
Image Placement (Double Exposure) (Indep	5.8	3.8	2.7	
Image Placement (DE) (Lines Dependent)	2.4	1.6	1.1	*4 nodes*
Mean to Target (MTT)	5.5	3.6	2.5	
Difference in CD MTT for DE	2.7	1.8	1.3	*2 nodes*
CD Uniformity (nm, 3 Sigma) Isolated Lines	3.3	1.8	1.4	
CD Uniformity (nm, 3 Sigma) Dense Lines	5.2	3.4	2.4	
DE - Dual Line Mask CD (nm, 3 Sigma)	2.4	1.6	1.1	*2 nodes*

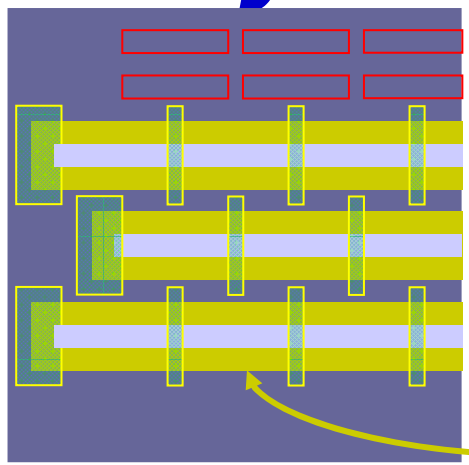
Note these are issues with LELE, LFLE
Not the Spacer Technology

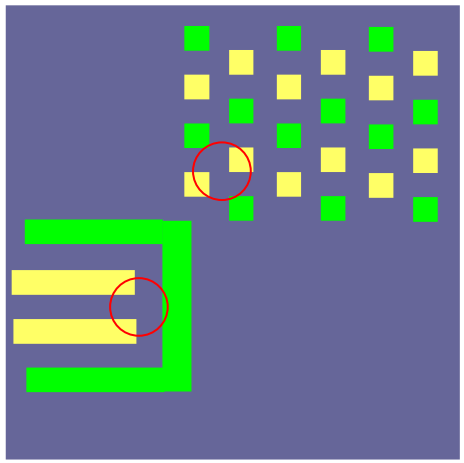
Splitting & Restricted Design Rule & Area Penalty



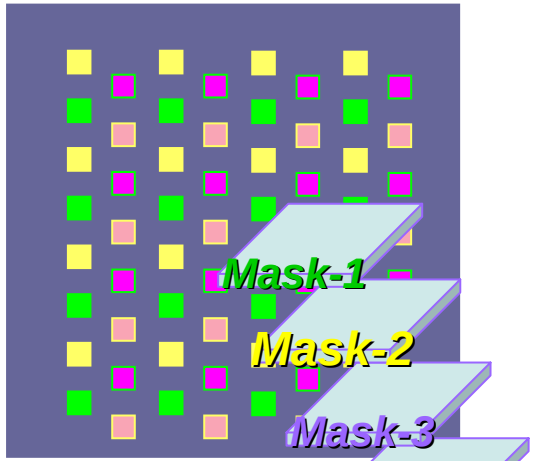
Coloring Confliction

Stitching

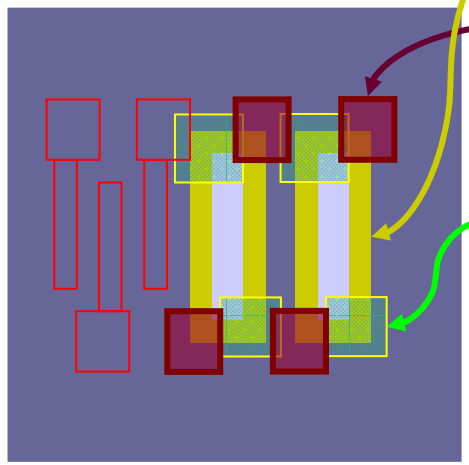




Pitch Splitting

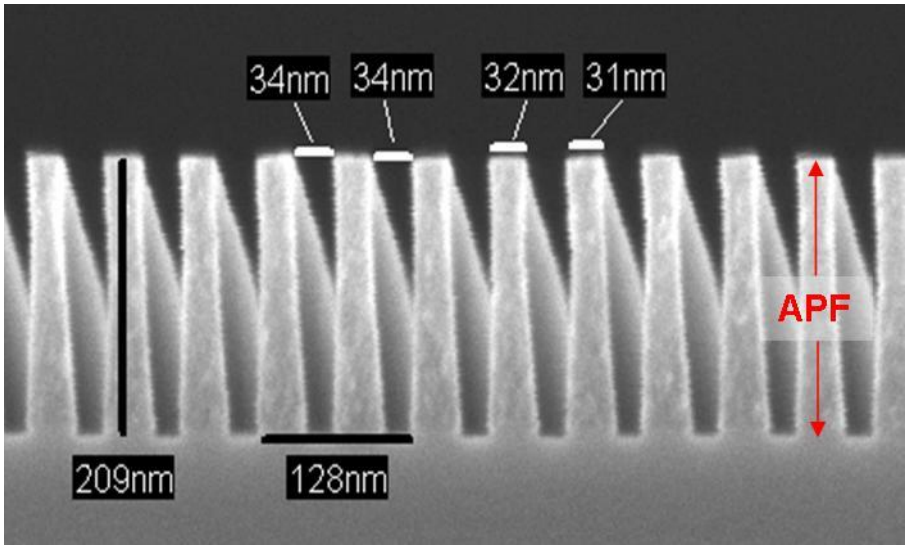


4 masks



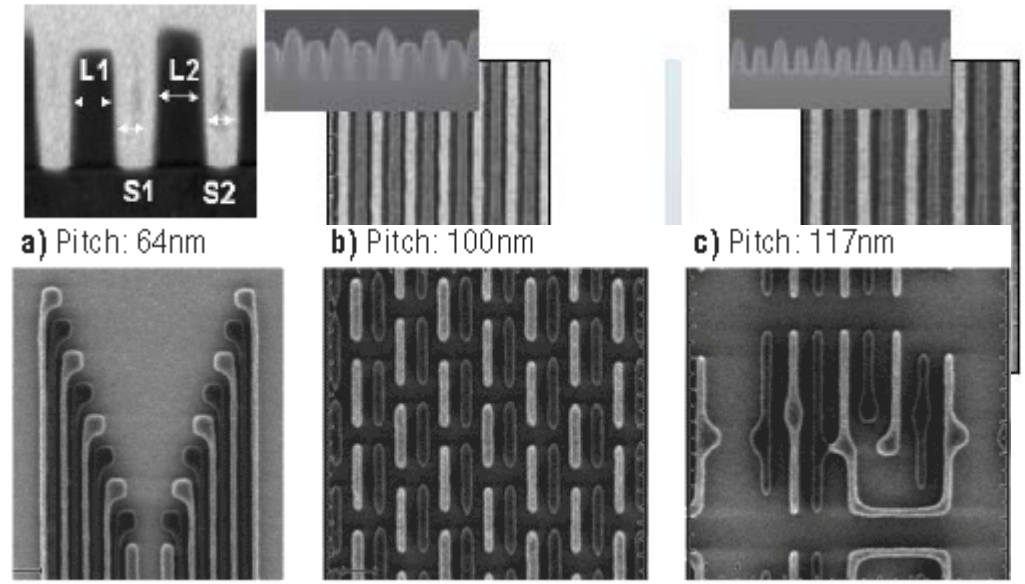
Spacer

3D metrology

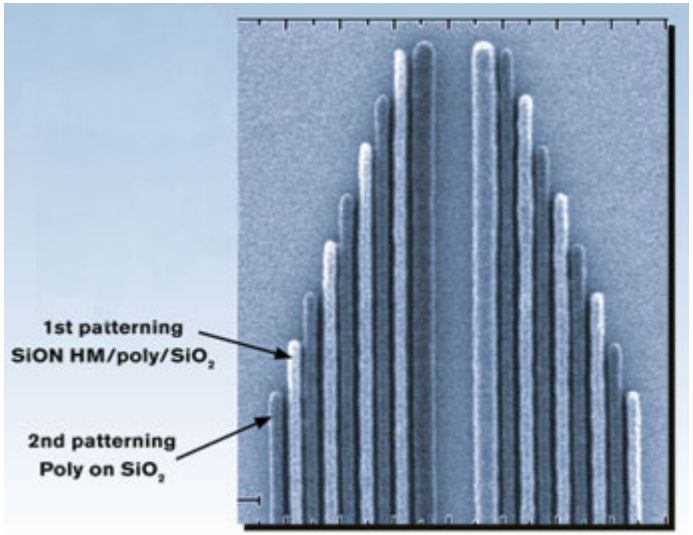


APPLIED MATERIALS
think it. apply it.™

"22nm Half-Pitch Patterning by CVD Spacer Self Alignment Double Patterning (SADP)", Christopher Bencher, Proc. of SPIE Vol. 6924, 69244E, (2008)
"Robust Method for Promotion of Adhesion of Resist to Dielectric ARC", Martin Seamons, International Immersion Lithography Symposium22-25 September, 2008

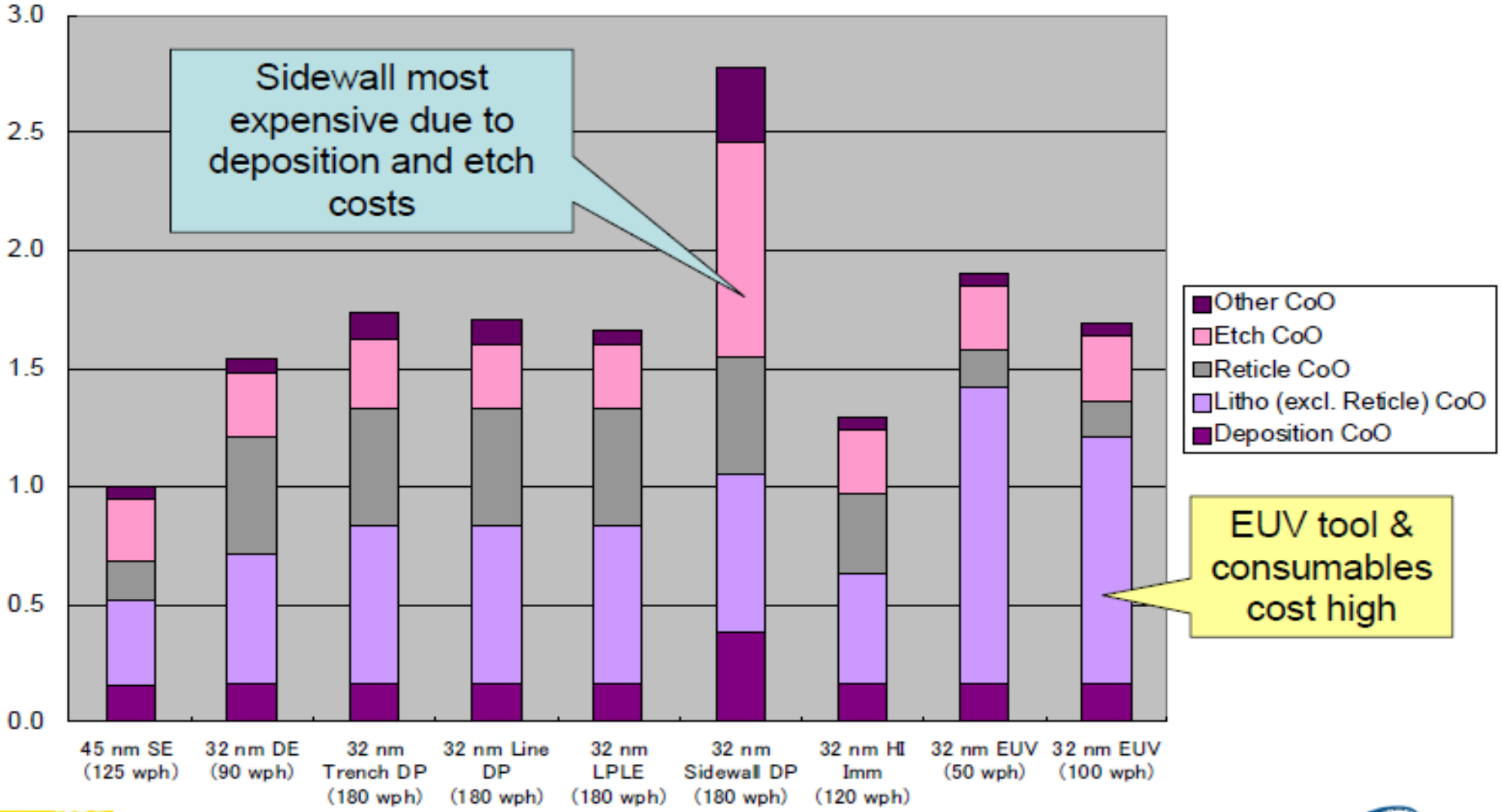


imec
aspire invent achieve



Source: "Meeting Double Patterning Challenges: from split to process control", Vincent Wiaux, et. al. (IMEC), NGL2007 Workshop

Results – 32 nm (20,000 wafers/mask)



EUVL

$$R = k_1 \frac{\lambda}{NA}$$

$k1 = HP * NA/\lambda$

方式	NA	DRAM Half-Pitch							
		2007	2010	2013		2016		2019	
		65nm	45nm	32 / SE	32 / DP	22 / SE	22 / DP	16 / SE	16 / DP
193i-water	0.92	0.31	0.21	0.15	0.31	0.10	0.21	0.08	0.15
	1	0.34	0.23	0.17	0.33	0.11	0.23	0.08	0.17
	1.07	0.36	0.25	0.18	0.35	0.12	0.24	0.09	0.18
	1.2	0.40	0.28	0.20	0.40	0.14	0.27	0.10	0.20
	1.3	0.44	0.30	0.22	0.43	0.15	0.30	0.11	0.22
	1.35	0.45	0.31	0.22	0.45	0.15	0.31	0.11	0.22
	1.45	0.48	0.34	0.24	0.48	0.17	0.33	0.12	0.24
	1.5	0.50	0.35	0.25	0.50	0.17	0.34	0.12	0.25
	1.6	0.54	0.37	0.27	0.53	0.18	0.36	0.13	0.27
	1.7	0.57	0.40	0.28	0.56	0.19	0.39	0.14	0.28
EUV	0.25	1.20	0.83	0.59		0.41		0.30	
	0.3	1.44	1.00	0.71		0.49		0.36	
	0.35	1.69	1.17	0.83		0.57		0.41	
	0.4	1.93	1.33	0.95		0.65		0.47	

×HIL

高NA-EUV、RETにより16nm-hpも視野に！

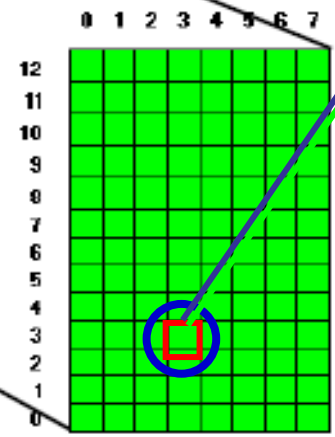
Electrical Inspection

SRAM Test Areas

R1 (area 1)

R1 (area 2)

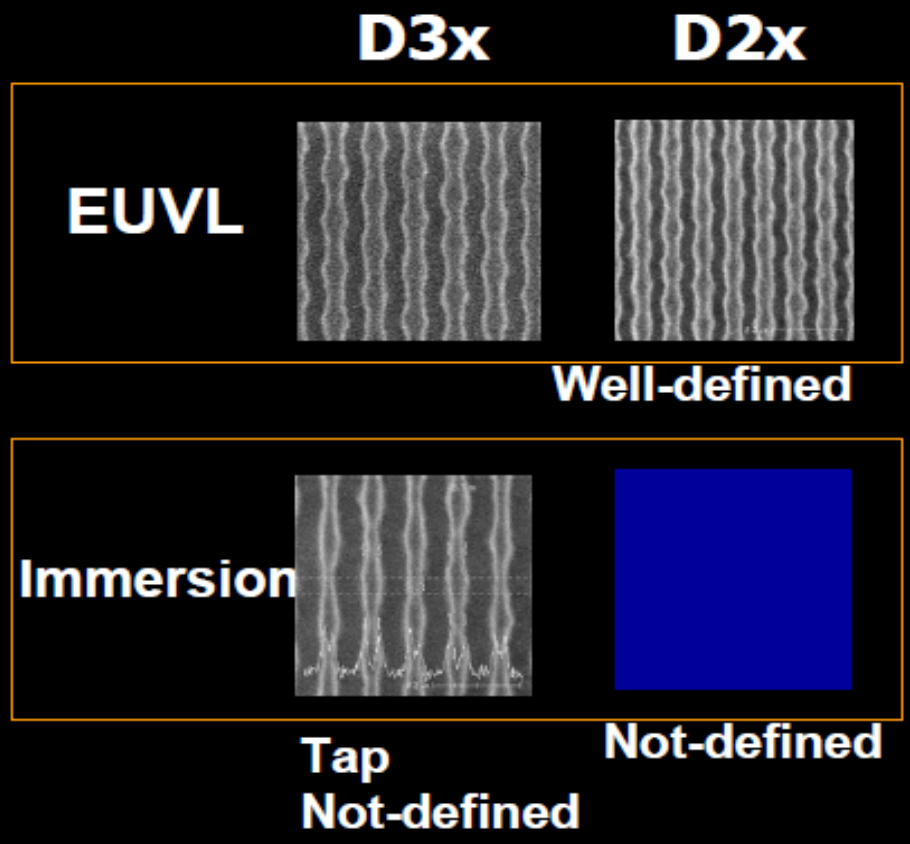
99.9992% yield or 2 bits out of 256 kbits are failing

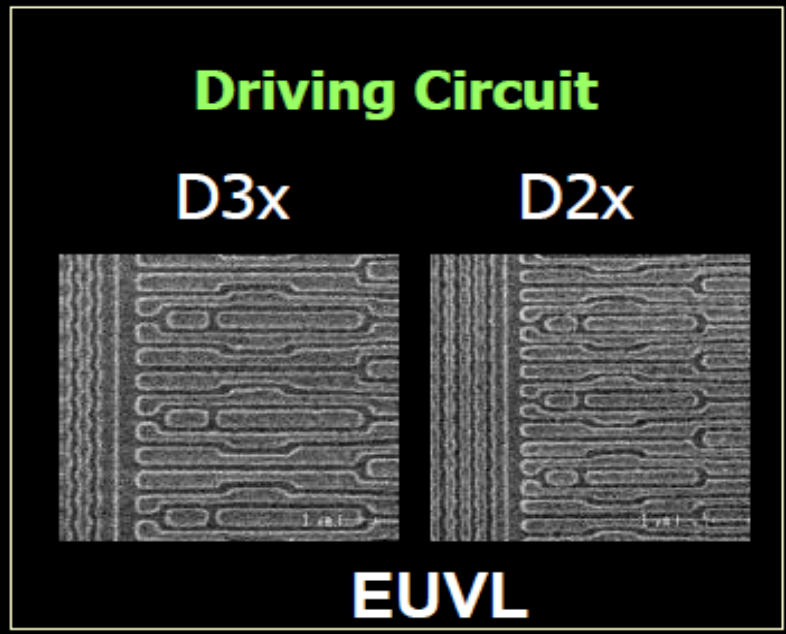


26 Mbits area (each square is 256 kbits)

"A Practical Approach to EUV Reticle Inspection", Anna Tchikoulaeva, et. al. ; 2008 International Symposium on Extreme Ultraviolet Lithography

DRAM cell pattern





EUVL shows superior patterning performance

"Full-field Patterning Test with ADT for 30-nm node Device Application", Doohoon Goo*, Insung Kim, Joo-On Park, Jeonghoon Lee, Changmin Park, Jinhong Park, Jeong-Ho Yeo, Sungwoon Choi, Woosung Han;
2008 International Symposium on Extreme Ultraviolet Lithography

EUV Focus Areas 2003-2008

SEMATECH

2003	2004	2005	2006	2007	2008
1. Source power and lifetime including condenser optics lifetime	1. Availability of defect free mask	1. Resist resolution, sensitivity & LER met simultaneously	1. Reliable high power source & collector module	1. Reliable high power source & collector module	1. Long-term source operation with 100 W at IF and 5MJ/day
2. Availability of defect free mask	2. Lifetime of source components & collector optics	2. Collector lifetime	2. Resist resolution, sensitivity & LER met simultaneously	2. Resist resolution, sensitivity & LER met simultaneously	2. Defect free masks through lifecycle & inspection/review infrastructure
3. Reticle protection during storage, handling and use	3. Resist resolution, sensitivity & LER met simultaneously	3. Availability of defect free mask	3. Availability of defect free mask	3. Availability of defect free mask	3. Resist resolution, sensitivity & LER met simultaneously
4. Projection and illuminator optics lifetime	▪ Reticle protection during storage, handling and use	4. Source power	4. Reticle protection during storage, handling and use	4. Reticle protection during storage, handling and use	• Reticle protection during storage, handling and use
5. Resist resolution, sensitivity and LER	▪ Source power	▪ Reticle protection during storage, handling and use	5. Projection and illuminator optics quality & lifetime	5. Projection and illuminator optics quality & lifetime	• Projection / illuminator optics and mask lifetime
6. Optics quality for 32-nm half-pitch node	▪ Projection and illuminator optics lifetime	▪ Projection and illuminator optics quality & lifetime			

EUVL Symposium 2008 (9/28-10/2)

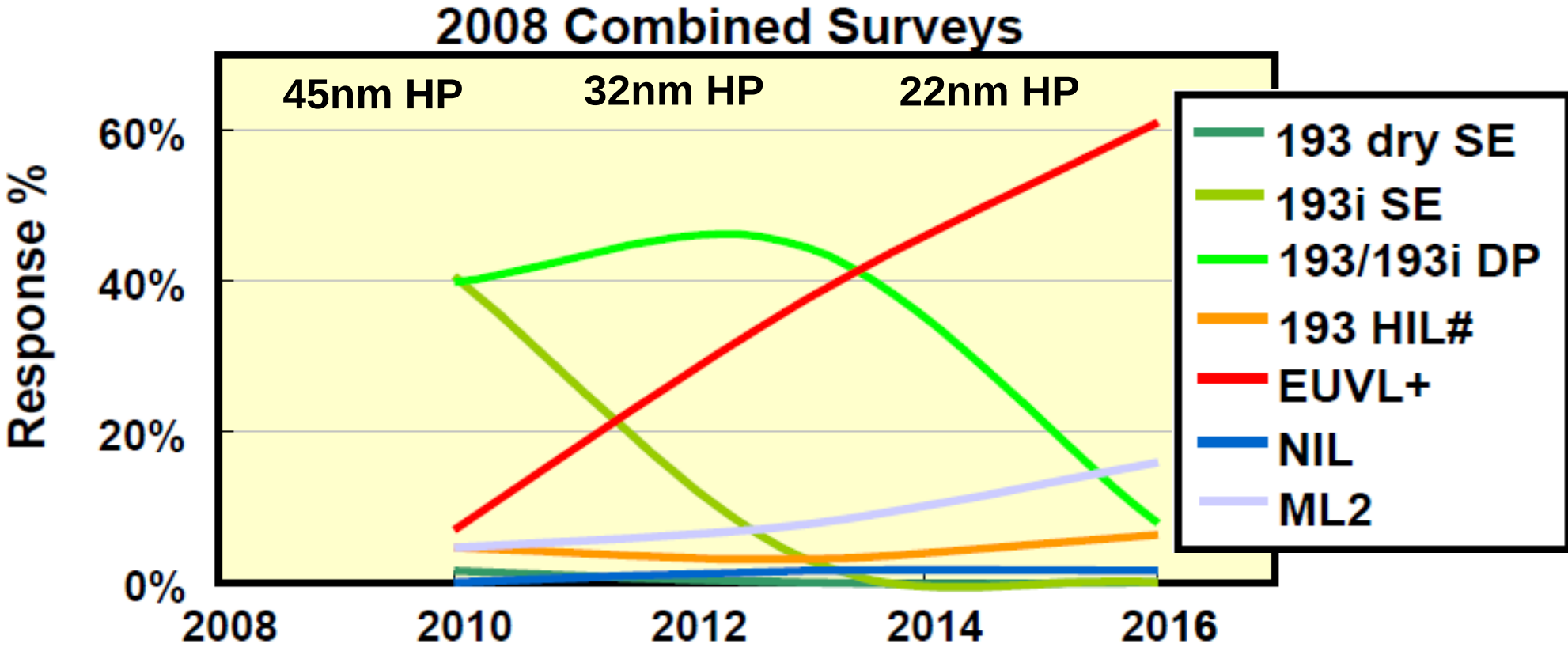
	Now	2010	2010	2012	2012	2012	2013	2013
Maker	Nikon	ASML	Nikon	ASML	Nikon	ASML	Canon	ASML
Tool	EUV1	PPT	EUV2	HVM1	EUV3	HVM2	HVM	HVM3
NA	0.25	0.25	0.25	0.3	>0.3	0.32 (offaxis)	>0.3	0.4
Flare	10%		7%		5%		5%	
Overlay	10nm	4nm	5nm	3nm	<3nm		<3nm (SMO)	
Resolution	32nm	27nm	22nm	22nm	16nm	16nm	LS <25nm, IL 17nm, CH <28nm	11nm
Throughput wph power resist shots/w	5-10 wph (10W IF, 5mJ/cm2) 76 shots	>60wph (100W IF, 10mJ/cm2)	20 wph (50W IF, 10mJ/cm2) 76 shots	150 wph (200W IF, 10mJ/cm2)	100 wph (115W IF, 5mJ/cm2 180W IF, 10mJ/cm2) 76 shots	150 wph (200W IF, 10mJ/cm2)	55 wph (100W IF, 10mJ/cm2)	150 wph (400W IF, 15mJ/cm2)
Field Size		26x33mm2						
Magnification		x1/4						

Pilot line 2010~2012

HVM 2012/2013~

Preferred Technology by Year

2008 SEMATECH Litho Forum survey results



Includes Double Patterning

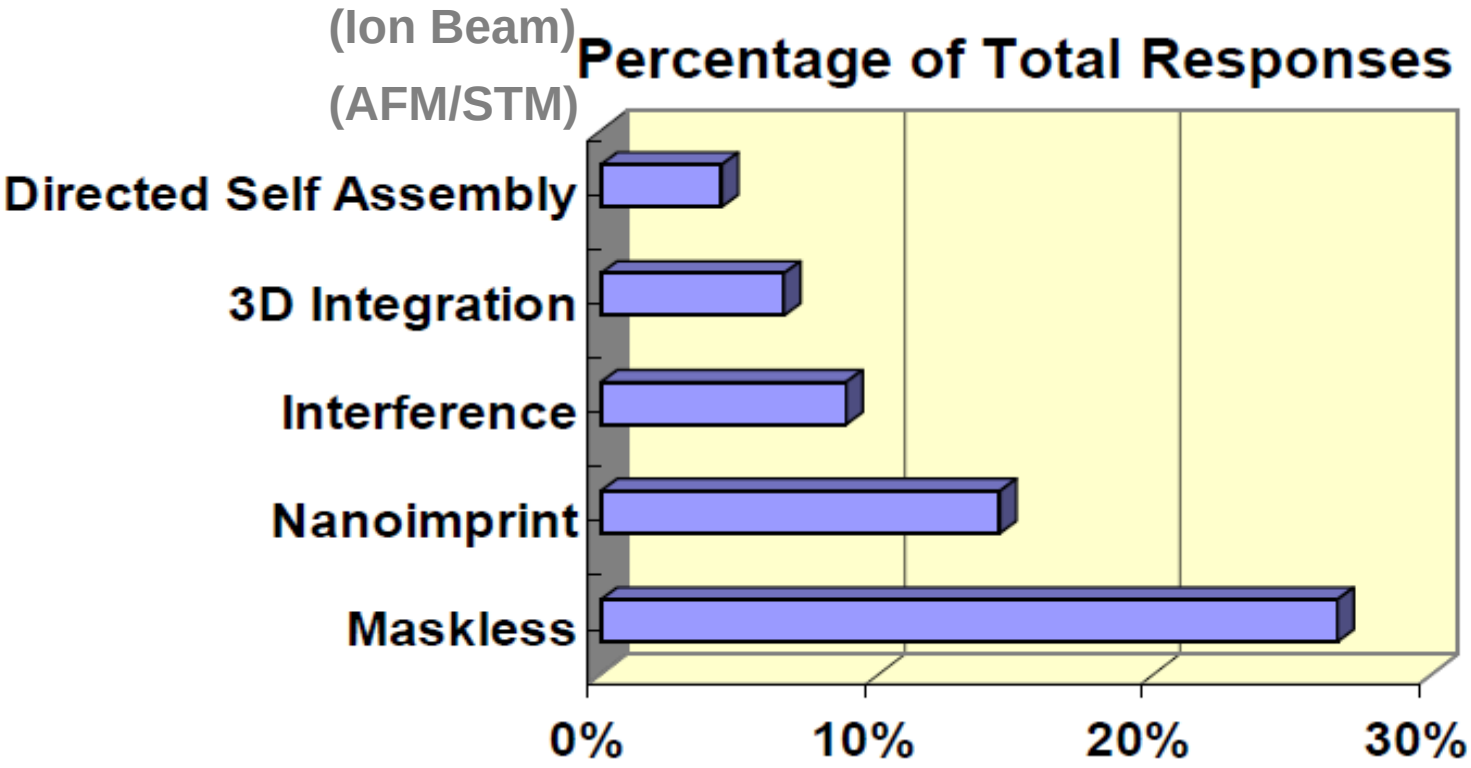
\+ Includes EUVL extension in 2016

Looking at 16nm Half Pitch

Alternative Lithography Technologies

2008 SEMATECH Litho Forum survey results

Technologies that should be pursued more aggressively to achieve ITRS goals



ML2 (Mask Less Lithography)

- **E-beam, Photo, Ion-beam**

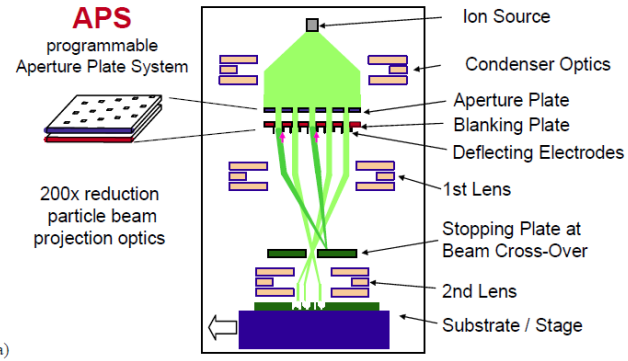
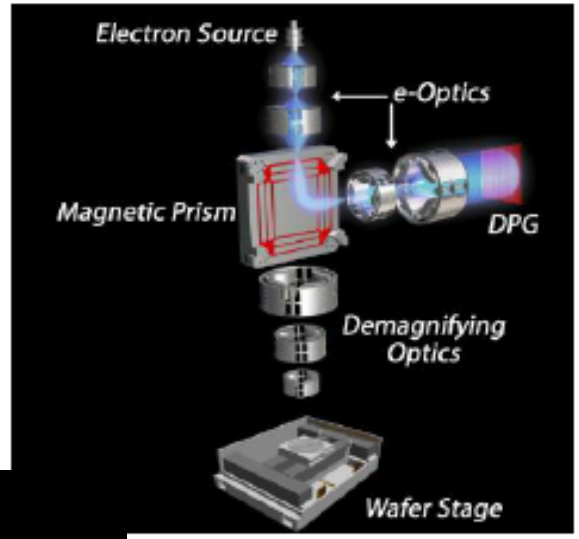


Figure 1: Principles of Projection Mask-Less Patterning (PMLP) and PMLP Proof-of-Concept Tool, realized as part of the European integrated project CHARPAN (Charged Particle Nanotech).

CEA-LETI

-EU- FP7
MAGIC



21 KLA-Tencor reflected e-beam
ithography (REBL) system.

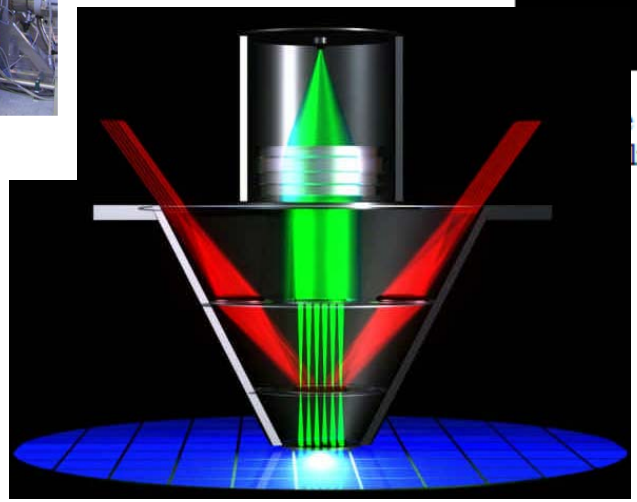
REBL/KLA-Tencor

PML2 PMLP/IMS Nanofabrication

Multibeam Systems

ZPAL/LumArray

OML/Micronic, ASML



MAPPER

DARPA

DIVA

Marching of the microlithography horses: Electron, ion, and photon: Past, present, and future
Burn J. LinProc. of SPIE Vol. 6520 652002-1

E-beam ML2 Throughput

Gun

Coulomb effect / Shot size

Design + Data preparation (VSB, CP)

Resist heating

Stage Max. G

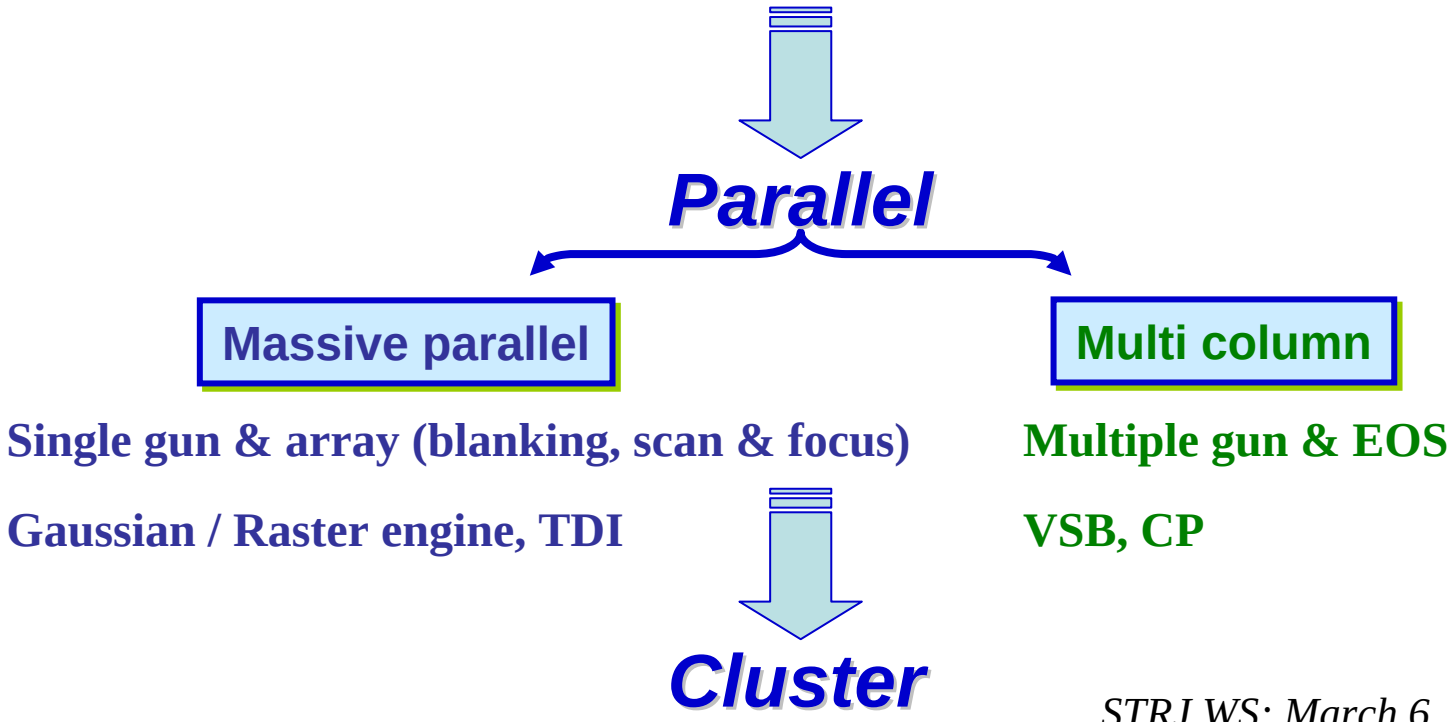
Wafer handling

Alignment

Resist sensitivity

DAC_AMP

TPT (wph) = Shots/Wafer × [Resist_Sensitivity/Current_density + Settling_time] + OH

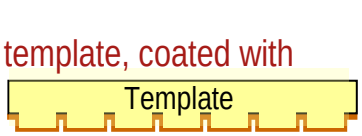


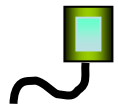
ML2

Multibeam Systems Inc. [MBI]/米 + TEL	Multi-Column, 50kV	・EBDW、マスク描画 ・>15wph (Via EBDW) ・2009年にデモ機完成 ・2013年 88コラム、10wph	・固定矩形に近い(3rd Order Imaging)、倍率可変、ベクター ・>1000A/cm2、50nA、Plasmaクリーニング ・2011年、10本カラム、0.2wph ・VSBのASIC用・マスク用、ポイントビームのマスク用も検討
KLA-Tencor (REBL) /米	Massive-Parallel, 50kV	・EBDW、マスク描画 ・2～40wph (層による) ・2013年にβ機	・反射型電子マスク(>1Mピクセル) ・回転ステージ ・DARPA ($100M+$100Mのマッチングファンド) '12年Proj.完了
Mapper Lithography (Mapper)/蘭	Massive-Parallel, 5kV	・EBDW ・10wph ・13k本ビーム ・2010年にα機	・ポイントビーム ・POL(110本) で40nm描画(静止)(但し1umフィールド、0.2nA/Beam(仕様1nA)) ・2009年、TSMC、LETIにプロト機(POL) ・ECのFP7の1つのプログラム(MAGIC)に参加(2008~2010)
IMS Nano-fabrication (PML2)/墺	Massive-Parallel, 50kV	・EBDW (マスクはIon) ・10wph ・>10M本ビーム ・2010年にα機	・ポイントビーム ・2千本ビームで描画成功(静止)、16nm解像 ・ECのFP7の1つのプログラム(MAGIC)に参加(2008~2010)
アドバンテスト (MCC)/日	Multi-Column, 50kV	・マスク描画、EBDW ・>5wph (EBDW、16カラム、20Gshot/wafer) ・2010年にβ(?)機	・VSB/CPビーム ・700CPアパーチャ ・ASET Mask D2I Projectでマスク描画用4カラムPOC機開発中

Nanoimprint

High resolution quartz template, coated with release layer

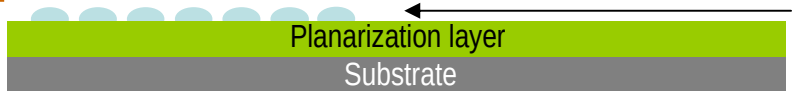




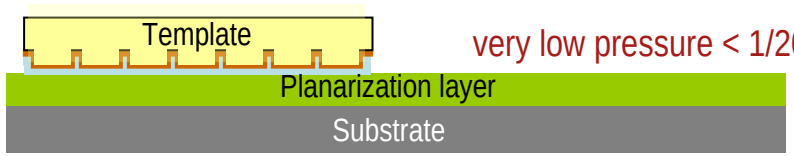
S-FIL fluid dispenser

Low viscosity fluid (Si-containing)

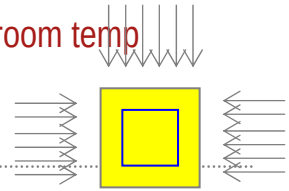
Step 1: Dispense drops



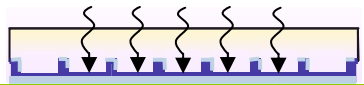
Step 2: Lower template and fill pattern

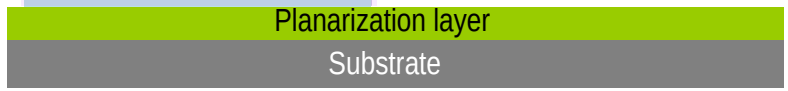


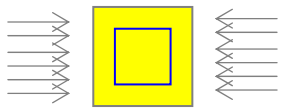
very low pressure < 1/20 atmosphere at room temp



Step 3: Polymerize S-FIL fluid with UV exposure



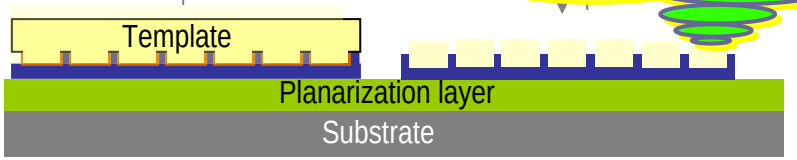


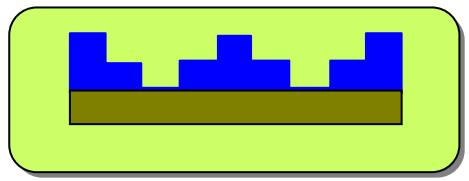


Step & Repeat!

LER/LWR, 3D (DD)

Step 4: Separate template from substrate

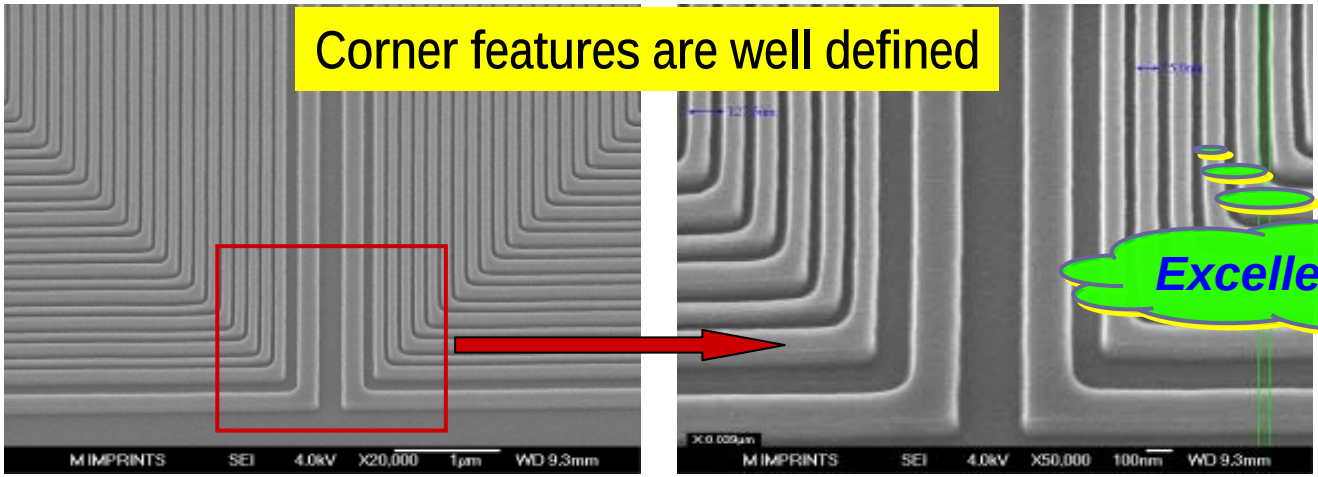


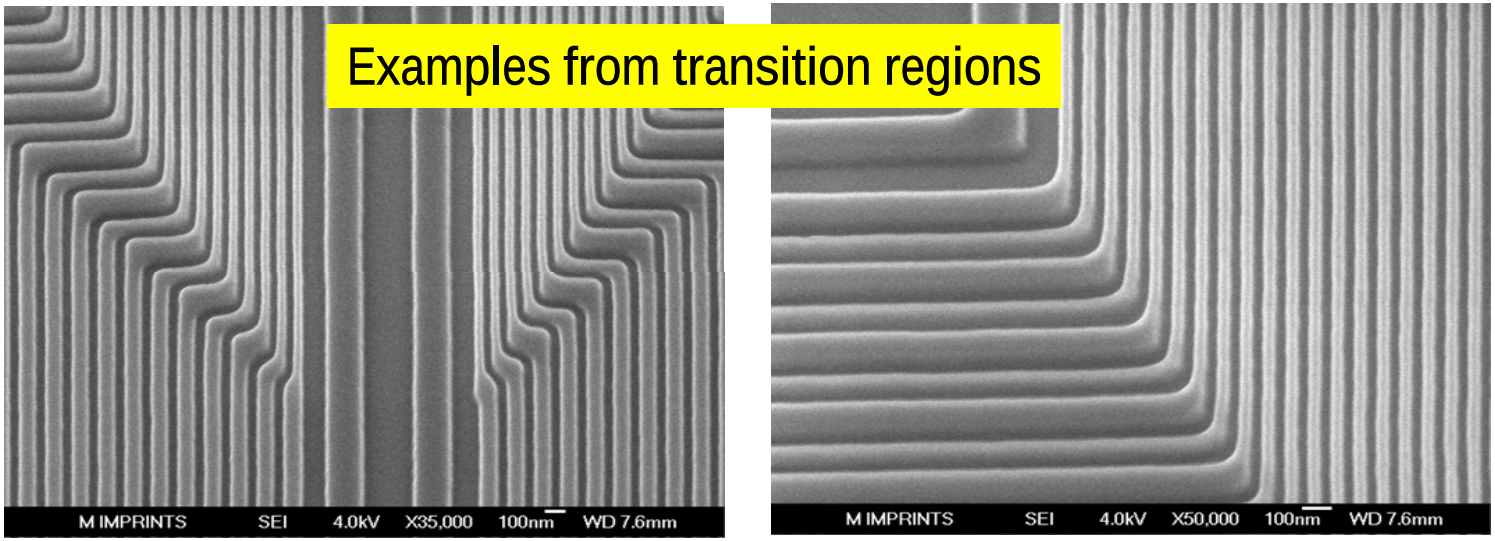


http://www.molecularimprints.com/NewsEvents/techarticles.html

Imprinted Structures in Resist

Main Pattern

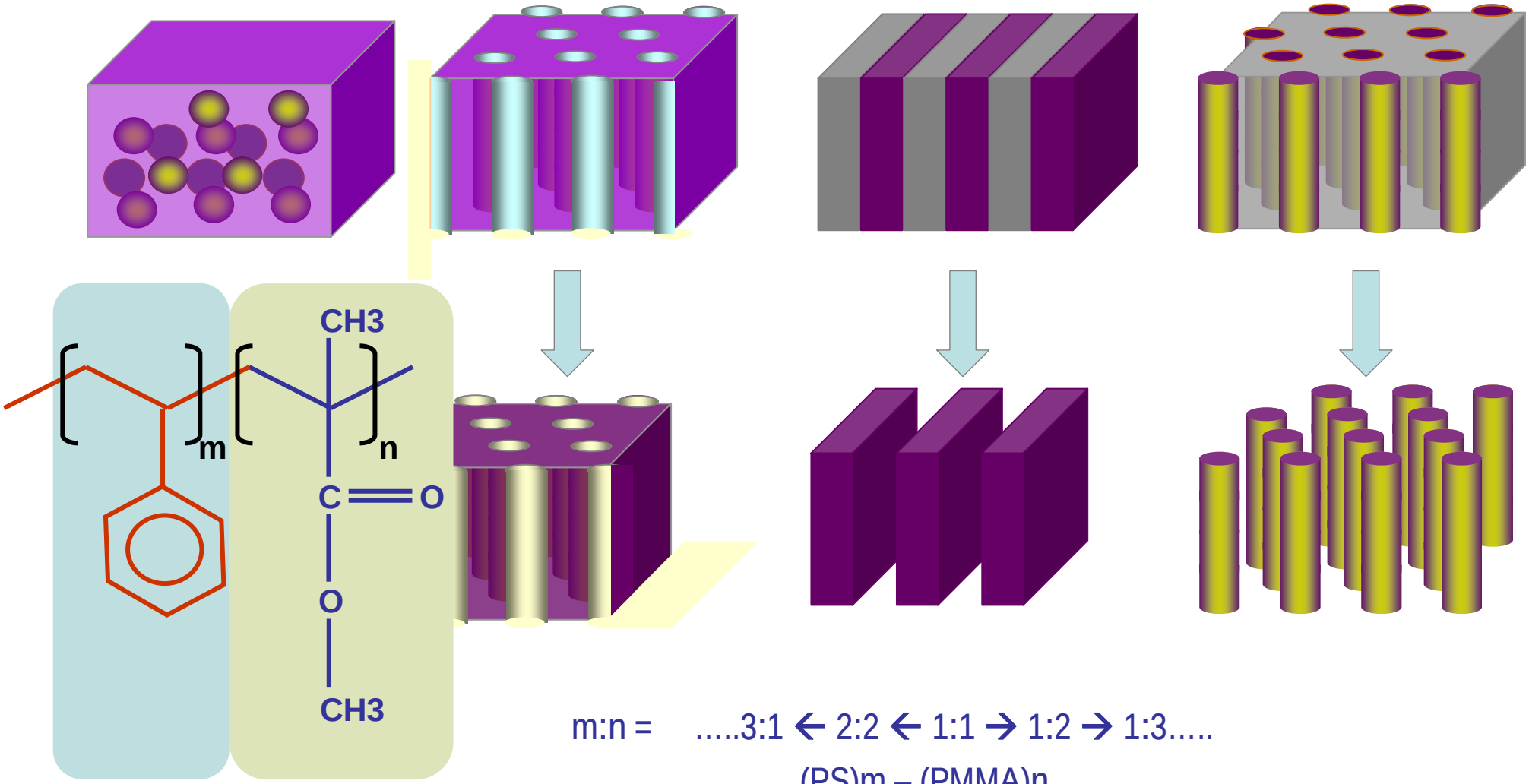




Feature fidelity is maintained in the transition regions

"Full field imprinting of sub-40 nm patterns", Jeongho Yeo, Hoyeon Kim, Ben Eynon, Samsung Electronics Co., Ltd, Proc. of SPIE Vol. 6921, 692107, (2008)

DSA (Directed Self Assembly)



m:n = ...3:1 ← 2:2 ← 1:1 → 1:2 → 1:3.....

(PS)m – (PMMA)n

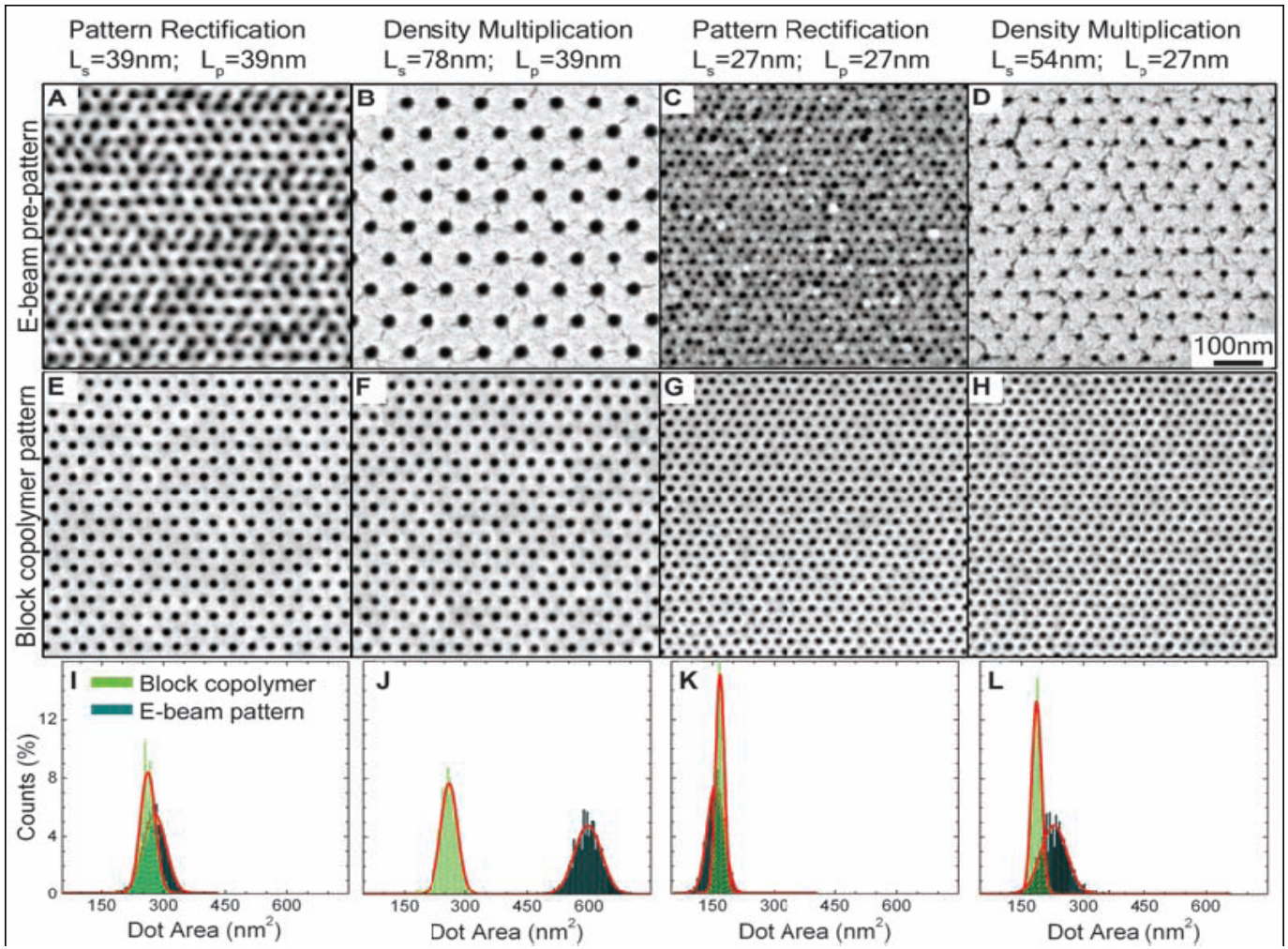


Fig. 2. (A to D) SEM images of developed e-beam resist with Ls = 39, 78, 27, and 54 nm, respectively. (E to H) SEM images of the block copolymer film on top of the prepattern defined by the corresponding e-beam pattern above. The lattice pitch on the block copolymer samples is Lp = 39, 39, 27, and 27 nm, respectively. (I to L) Dot size distribution of e-beam (dark teal) and guided block copolymer patterns (light green).

D. S. Kercher, T. R. Albrecht, J. J. de Pablo, P. F. Nealey, Science 936 vol. 321 (2008)

2009版に向けて

- EUVLの見極め
  - 光源
  - マスク
  - 露光装置
  - 欠陥、ペリクルレス
  - コスト

- More Moore
  - 16nm以細のリソグラフィ技術、NGL
  - 450mm

- More than Moore
  - リソグラフィへの要求　⇔　デバイス

まとめ

- 32 nmは、DPで。
  - 特に先行するFlashには、EUVLは、間に合わない。
  - DRAM、LogicにはEUVLが適用される可能性がある
  - DPは、コストが課題
    - データ分割処理
    - プロセス
    - マスク
    - 露光装置
- 22 nmの本命はEUVL

  ✓光源、無欠陥マスク、レジスト、など課題は依然山積
- 16 nm以細は混沌