

ITRS 2009の概要

半導体技術ロードマップ専門委員会(STRJ) 委員長

石内秀美 (東芝)

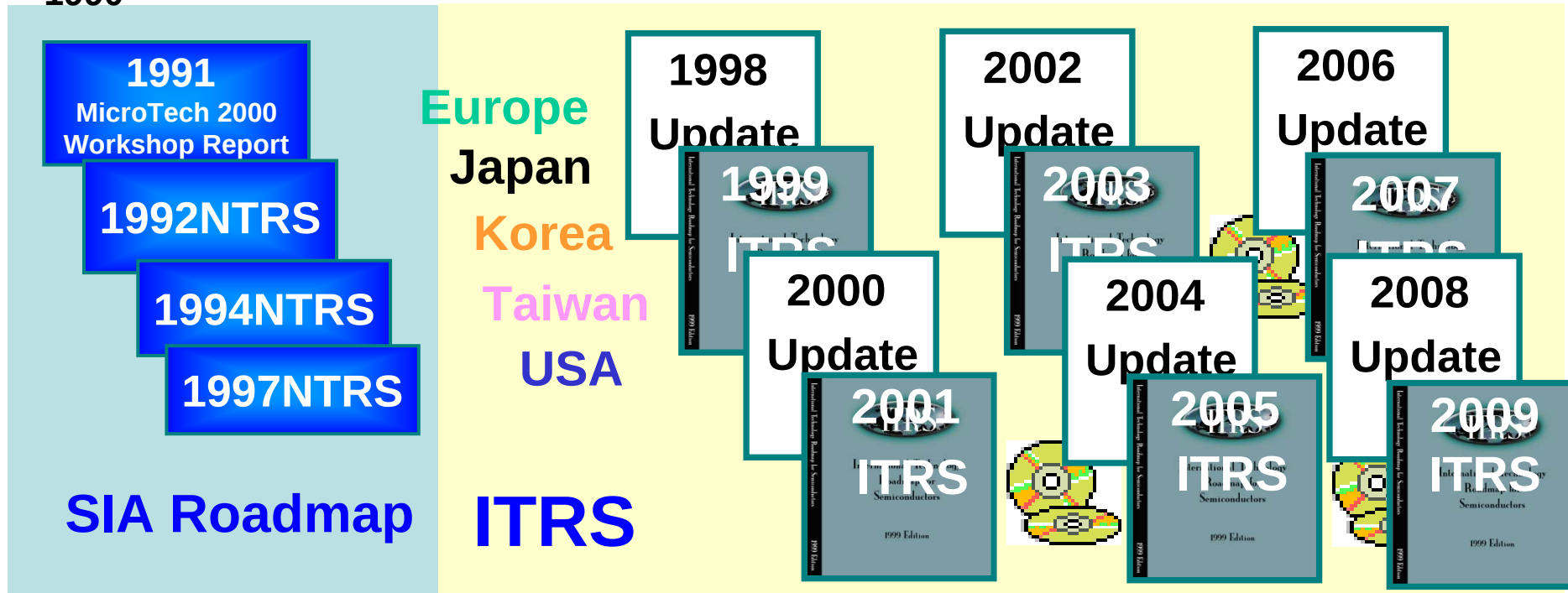
主要略語一覧(アルファベット順)

- ERD: Emerging Research Devices 新探究デバイス
- ERM: Emerging Research Materials 新探究材料
- EUV: Extreme Ultra Violet
- FEP: Front End Process (ITRSの章の名前でもある)
- High-k: 高誘電率(比誘電率の記号としてkを使うことから)絶縁膜。MOSFET用のゲート絶縁膜
- ITRS: International Technology Roadmap for Semiconductors 国際半導体技術ロードマップ
- JEITA: 社団法人 電子情報技術産業協会 (Japan Electronics and Information Technology Industries Association)
- Low-k: 低誘電率(比誘電率の記号としてkを使うから)絶縁膜。多層金属配線用絶縁膜
- M1: Metal-1 最下層(第1)の金属配線層
- MPU: Micro Processor Unit マイクロプロセッサ
- NTRS: National Technology Roadmap for Semiconductors 米国のSIAが編集した半導体技術ロードマップ
- PIDS: Process Integration, Devices and Structures (ITRSの章の名前)
- SIA: Semiconductor Industry Association 米国半導体工業会
- STRJ: Semiconductor Technology Roadmap committee of Japan 半導体技術ロードマップ専門委員会。JEITA半導体部会 半導体技術委員会 の専門委員会

STRJ, ITRSの歴史と現状



1990



STRJ

タスクフォース、クロスカット活動

1998年発足

半導体産業・技術開発の経済性委員会

1999	2000	2001	2002	2003	2004	2005	2006	2007	2008
STRJ報告	STRJ報告	STRJ報告	STRJ報告	STRJ報告	STRJ報告	STRJ報告	STRJ報告	STRJ報告	STRJ報告

1. Executive Summary
2. System Drivers
3. Design
4. Test & Test Equipment
5. Process Integration, Devices & Structures
6. RF and A/MS Technologies for Wireless Communications
7. Emerging Research Devices
8. Emerging Research Materials
9. Front End Processes
10. Lithography
11. Interconnect
12. Factory Integration
13. Assembly & Packaging
14. Environment, Safety & Health
15. Yield Enhancement
16. Metrology
17. Modeling & Simulation

ITRS 2009年版 の概要(1)

- 電子化を推進。各章ごとにpdfファイルとして公開。印刷を前提としない。
- 表はエクセルのファイルとして公開。
- NAND Flashメモリの微細化トレンドについて見直す。現状のサーベイに基づき、微細化ペースを前倒しする方向で議論。2010年まで、2年ごとに0.7倍のペースで微細化が進み2010年に32nmに達する。以後は3年で0.7倍のペース。
- MPUのM1ハーフピッチは2013年まで、2年ごとに0.7倍のペースで微細化が進み2013年に27nmに達する。以後は3年で0.7倍のペース。
- DRAMのハーフピッチについては変更せず。ただし、2011年にDRAMセルサイズは6F2から4F2に移行。

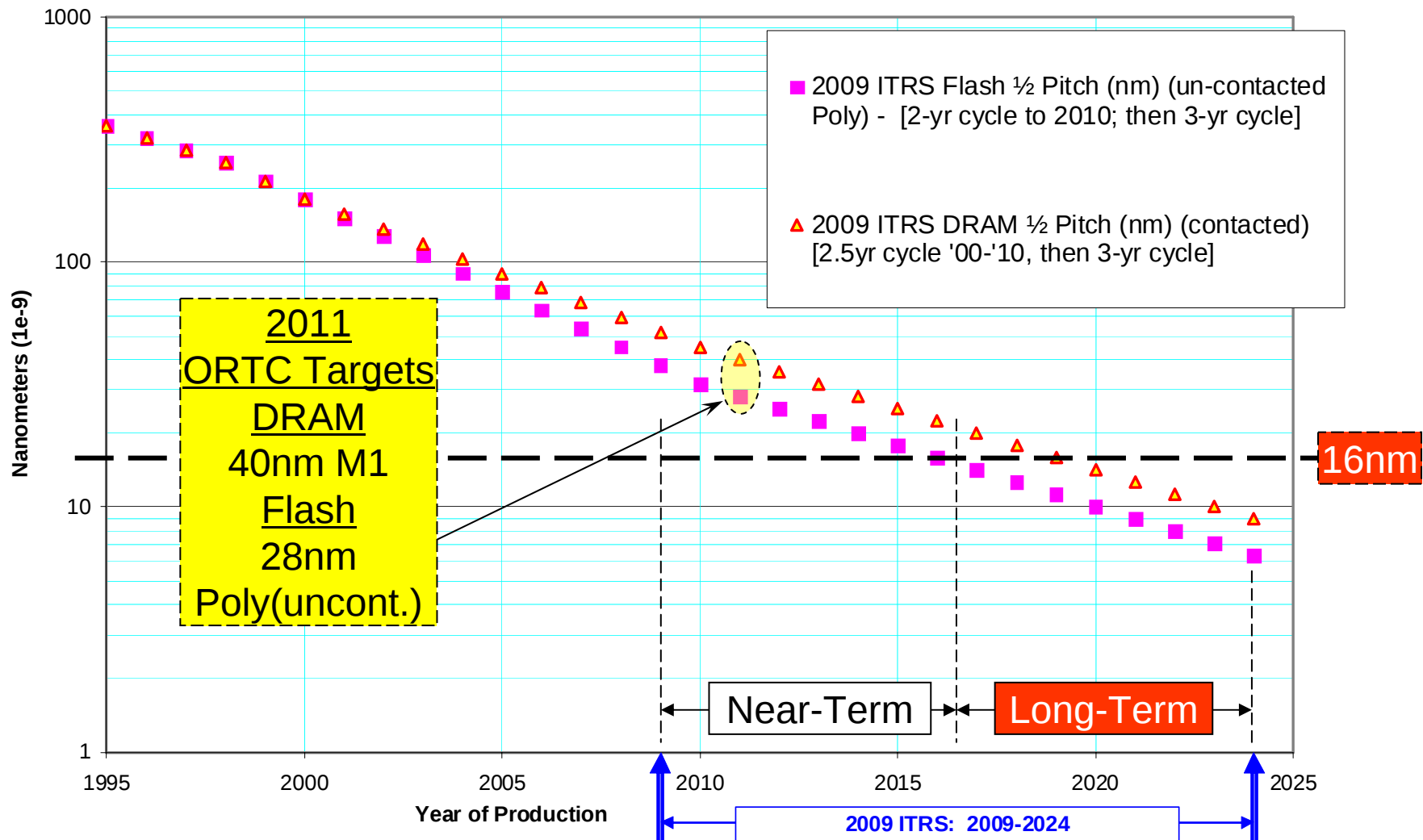
ITRS 2009年版 の概要(2)

- 昨年は、ERD(新探究デバイス)WGでは新探究デバイスの候補を7つに絞り込み、メンバー間で投票。カーボン系の材料(グラフェン、カーボンナノチューブ)を使ったデバイスが第1位。昨年度はERDとしてはITRSのUpdateを見送ったため、この内容が掲載されるのはITRS 2009年版が最初となる。
- ERDでは、上記に加え、新規メモリのための技術候補についてアセスメントを行う予定。
- 450mmウェーハでの製造については、2012年にパイロットラインの整備、その2-3年後の量産化をめざす。

Figure 7a

2009 ITRS - Technology Trends

Memory

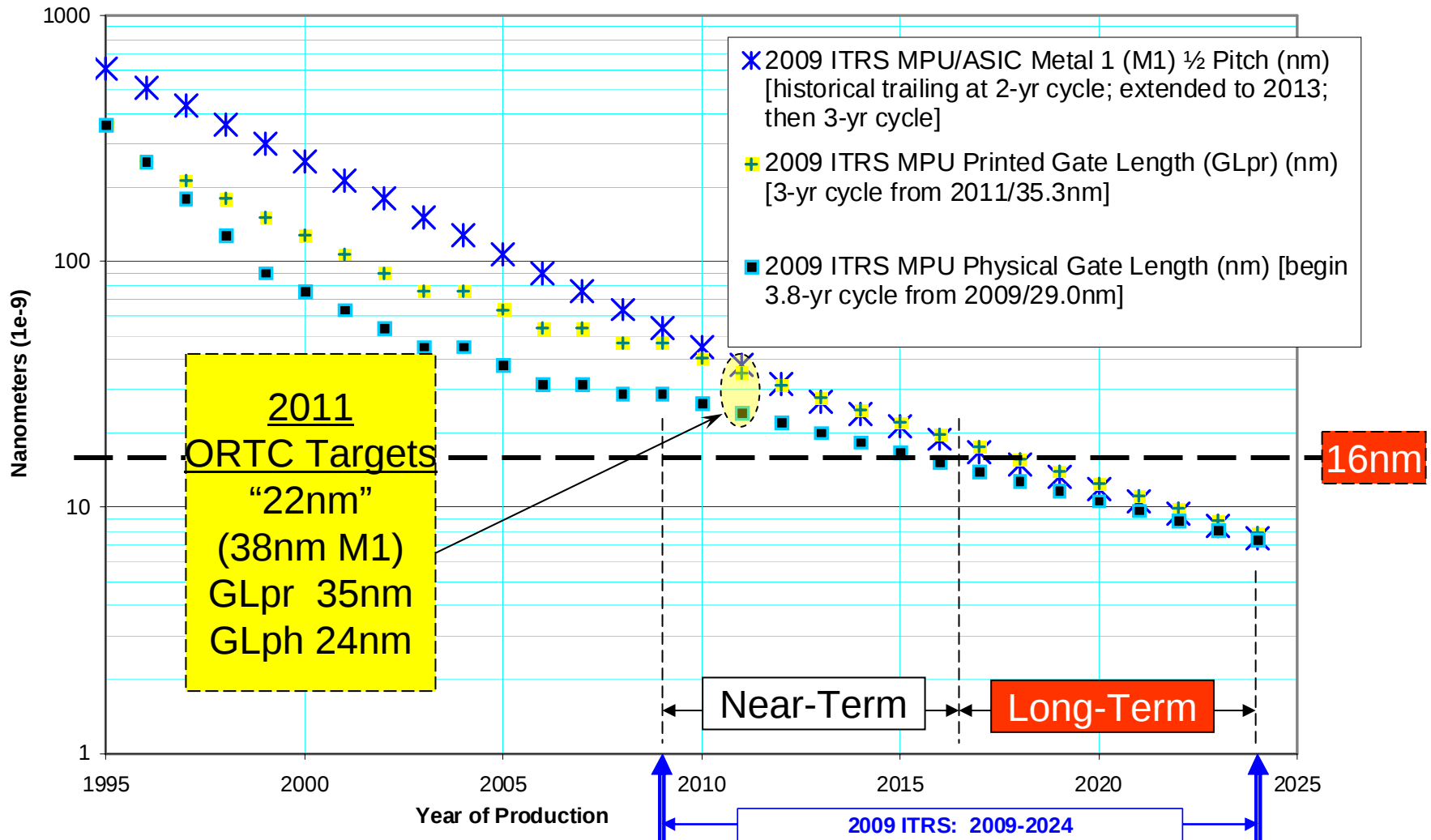


Source: 2009 ITRS - Executive Summary Fig 7a

Figure 7b

2009 ITRS - Technology Trends

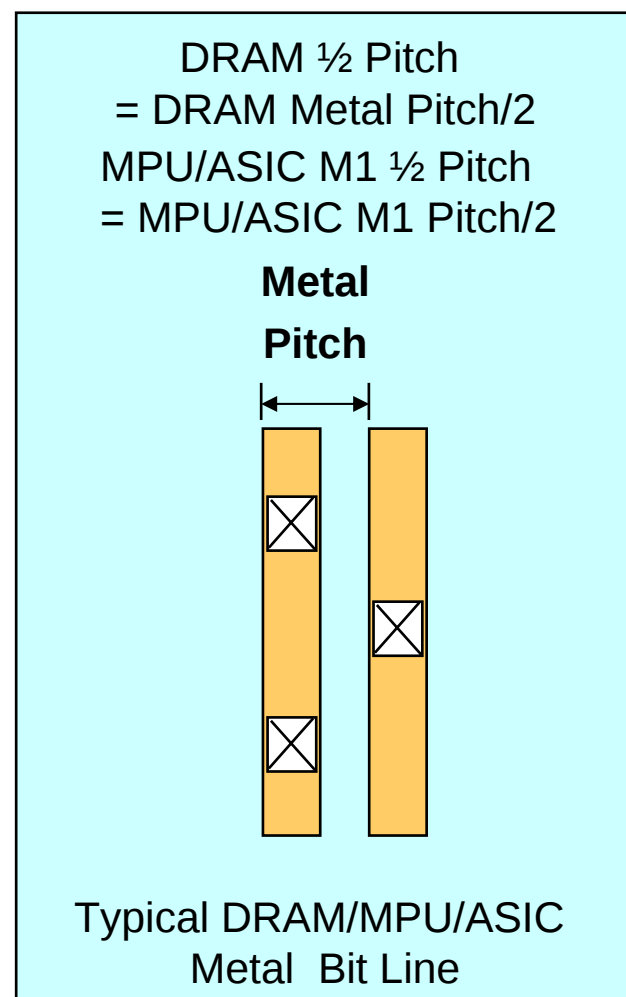
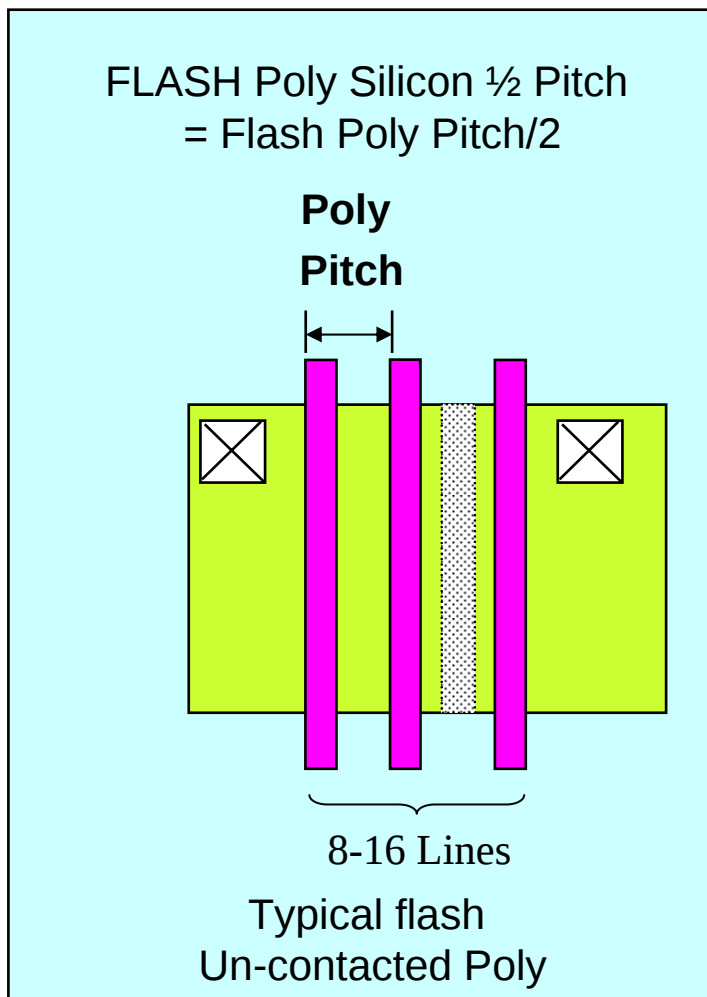
Logic



Source: 2009 ITRS - Executive Summary Fig 7b

2007 Definition of the Half Pitch - **unchanged**

[No single-product “node” designation; DRAM half-pitch still litho driver; however, other product technology trends may be drivers on individual TWG tables]



Source: 2005 ITRS - Exec. Summary Fig 2

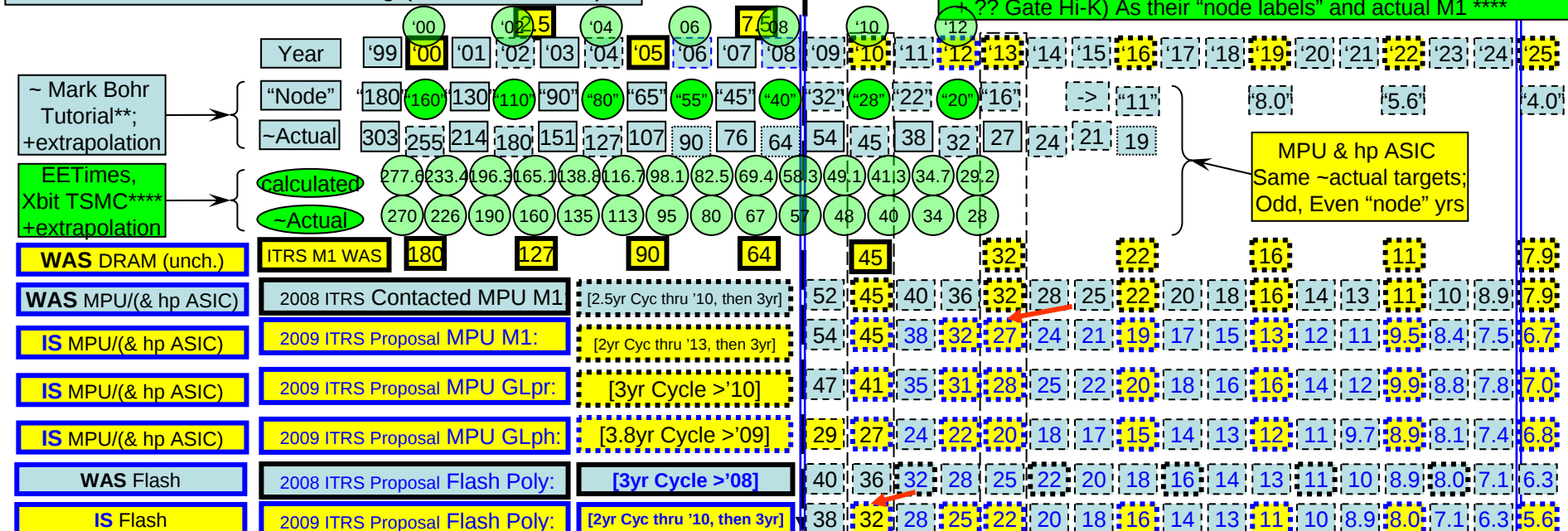
Industry MPU [also Hi-Performance (hp) ASIC] "Node"* Alignment w/ITRS

DRAM Density "Equiv. Scaling":	8f ²	8f ²	6f ²	4f ²	TBD	TBD	TBD
Flash Density MLC "Equiv. Scaling":	16/11/8/5.5/4f ² : 2b/cell	2.0f ² : 2b/cell	1.5f ² : 3b/cell	1.0f ² : 4b/cell	TBD	TBD	TBD
MPU Perform/Power "Equiv. Scaling":	Copper	Strain	HiK/MG	TBD	TBD	TBD	TBD

Dimensional Half Pitch Scaling (EOT not shown):

Past ↔ Futu

Note: TSMC uses "40nm" (no HiK/MG) and "28nm" (SiON Lo-K) as their "node labels" and actual M1 ****



*Notes:

- 1) DRAM industry "Node" typically = Contacted M1 half-pitch***;
- 2) Flash "Node" typically = Uncontacted Poly half-pitch, which is approx. equivalent (i.e., using same lithography technology) to a 2-year lead of DRAM contacted M1 DRAM.
- 3) Litho TWG estimates Flash driving Lithography since 2007.
- 4) At 2-year behind the Flash Uncontacted-Poly, the 2012/32nm Contacted M1 MPU/hp-ASIC will be a co-driver of Lithography, and will lead DRAM M1 by 1 year.

**Mark Bohr Tutorial, 3/5/08, #19 "Transistor [half] Pitch" and #5 "Minimum Feature Size"

***However, Inoue-san presentation has Samsung Using "40nm-class" announcement in 2009 (52nm?)

* http://intel_im.edgesuite.net/2008/123085/IM2008_Bohr.pdf

****TSMC "Nodes" Articles @:

http://www.tsmc.com.tw/pressroom/2009030205529_TSMC_Unveils_32nm_28nm_Process_Technologies_Roadmap.html; <http://www.eetimes.com/news/semi/showArticle.jhtml?articleID=177100920>

Source: ITRS Public Conference, July 2009

2009 ITRS: 2009-2024

Work in Progress - Do not publish

STRJWS: March 5, 2010, IRC 10

More Moore と More than Moore

- More Moore
 - Geometrical Scaling: 幾何学的(寸法の)スケーリング
 - Equivalent Scaling: 等価的(実効的)スケーリング
- More than Moore
 - 必ずしも微細化のみによらない多様化
 - SiP(System in Package)技術による異種のチップの集積化
- Beyond CMOS
 - シリコンCMOS技術に代わる新技術

2007 ITRS Executive Summary Fig 4

Moore's Law & More

✓ New work
In 2009

Traditional
ORTC Models

Functional Diversification (More than Moore)

Scaling (More Moore)
[Geometrical & Equivalent scaling]
Baseline CMOS: CPU, Memory, Logic

130nm
90nm
65nm
45nm
32nm
22nm
...
V

Analog/RF

HV
Power

Passives

Sensors
Actuators

Biochips

Interacting with people
and environment

Non-digital content
System-in-package
(SiP)

Information
Processing

Digital content
System-on-chip
(SoC)

Combining SoC and SiP: Higher Value Systems

Beyond CMOS

New in 2009:
✓ More than Moore
"White Paper"
✓ More Commentaries
In ITWG Chapters

Online in 2008:
✓ SIP "White Paper"
www.itrs.net/papers.htm

New in 2009:
✓ Survey updates
to ORTC Models
✓ Equivalent Scaling
Roadmap Timing
Synchronized with
PIDS and FEP

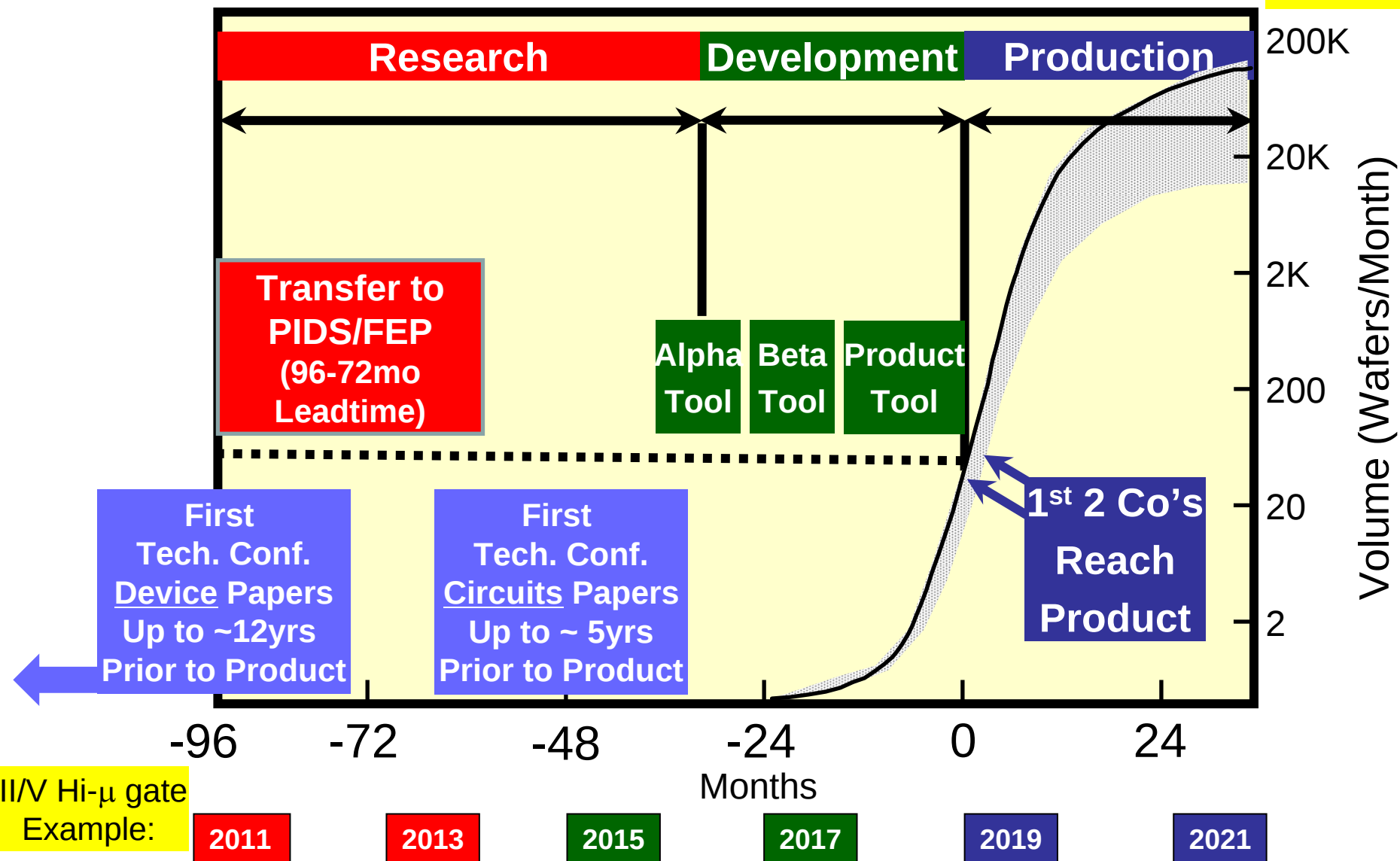
New in 2009:
✓ Research and PIDS transfer timing clarified
✓ Work underway to identify next storage element

Source: 2009 ITRS - Executive Summary Fig 1

ERD/ERM Long-Range R&D and PIDS Transfer Timing Model Technology Cycle Timing

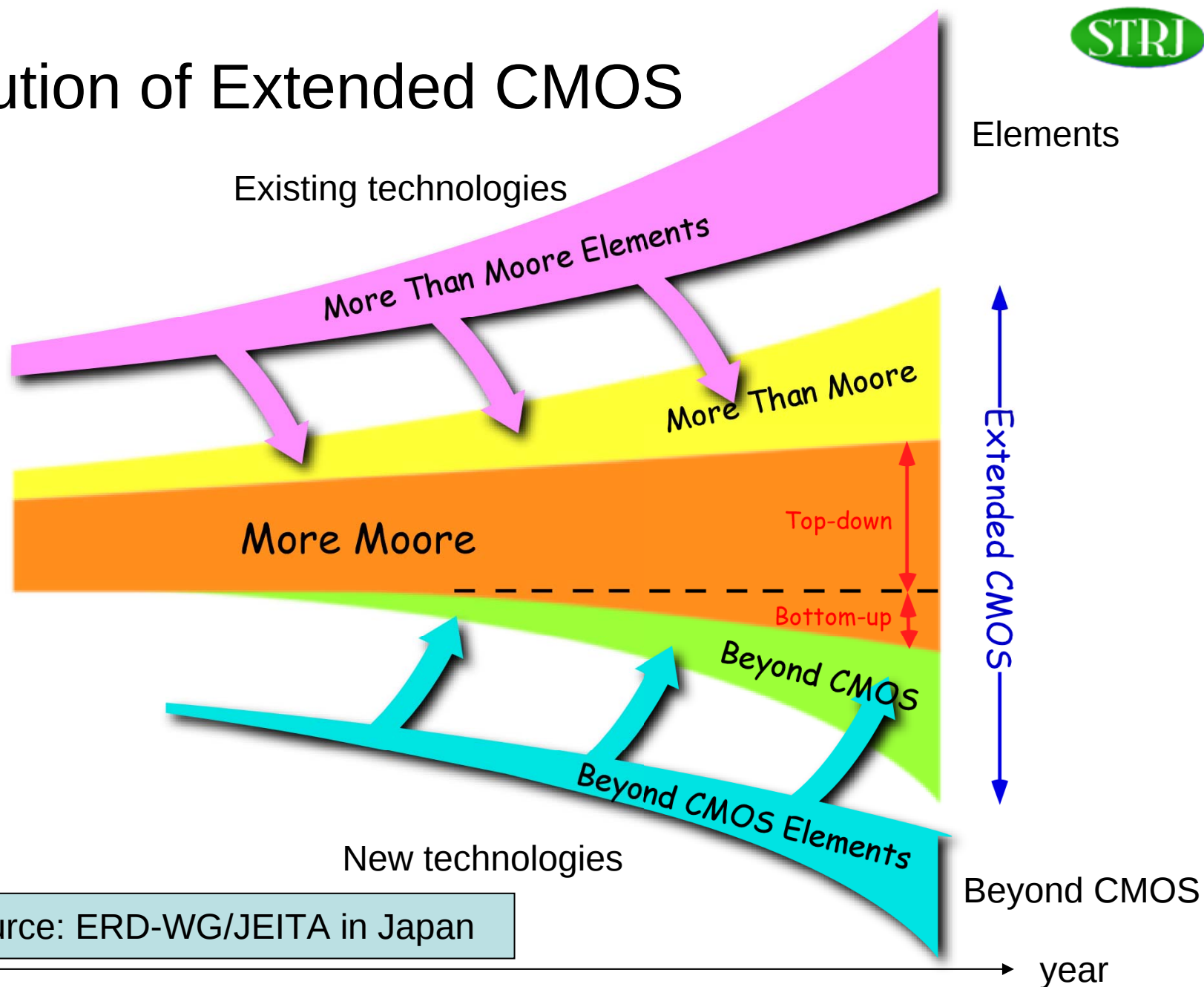
[Example: III-V MOSFET High-mobility Channel Replacement Materials]

New
for 2009



Source: 2009 ITRS - Executive Summary Fig 2b

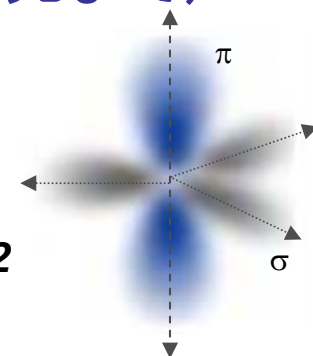
Evolution of Extended CMOS



sp^2 Carbon: 0-Dim. to 3-Dim.

(炭素原子 sp^2 混成軌道が作る構造: 0次元から3次元まで)

Atomic orbital sp^2



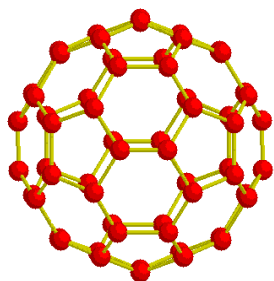
0D

1D

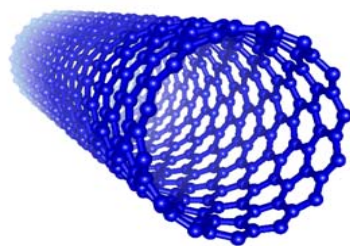
2D

3D

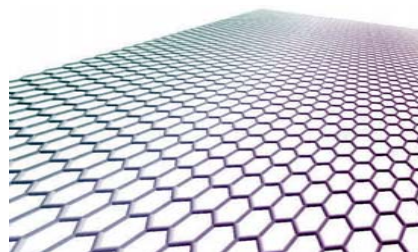
Fullerenes (C_{60})



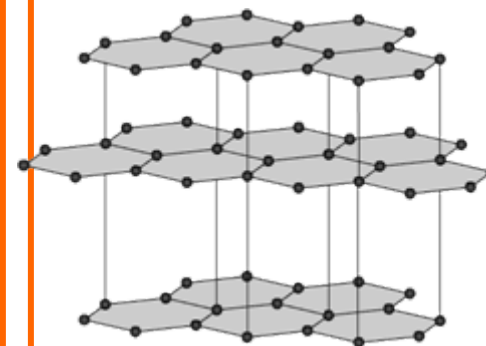
Carbon Nanotubes



Graphene



Graphite



2009 ITRS 450mm Update

[from Public ORTC San Francisco SEMICON, July, 2009]

ITRS IRC 2009 Position (Source 2009 Executive summary; 450mm Special Topic):

“...Intel, Samsung, and TSMC (IST) announced in May’08 that they will work together with suppliers, other semiconductor players and ISMI to develop 450mm with a goal of a pilot line in 2012. Full production may be 2-3 years after that^[1]. This Public announcement and assessment may be subject to revision based on future statements; but it is the statement of record by these three companies and ISMI, as of the date of writing of the ITRS 2009 edition

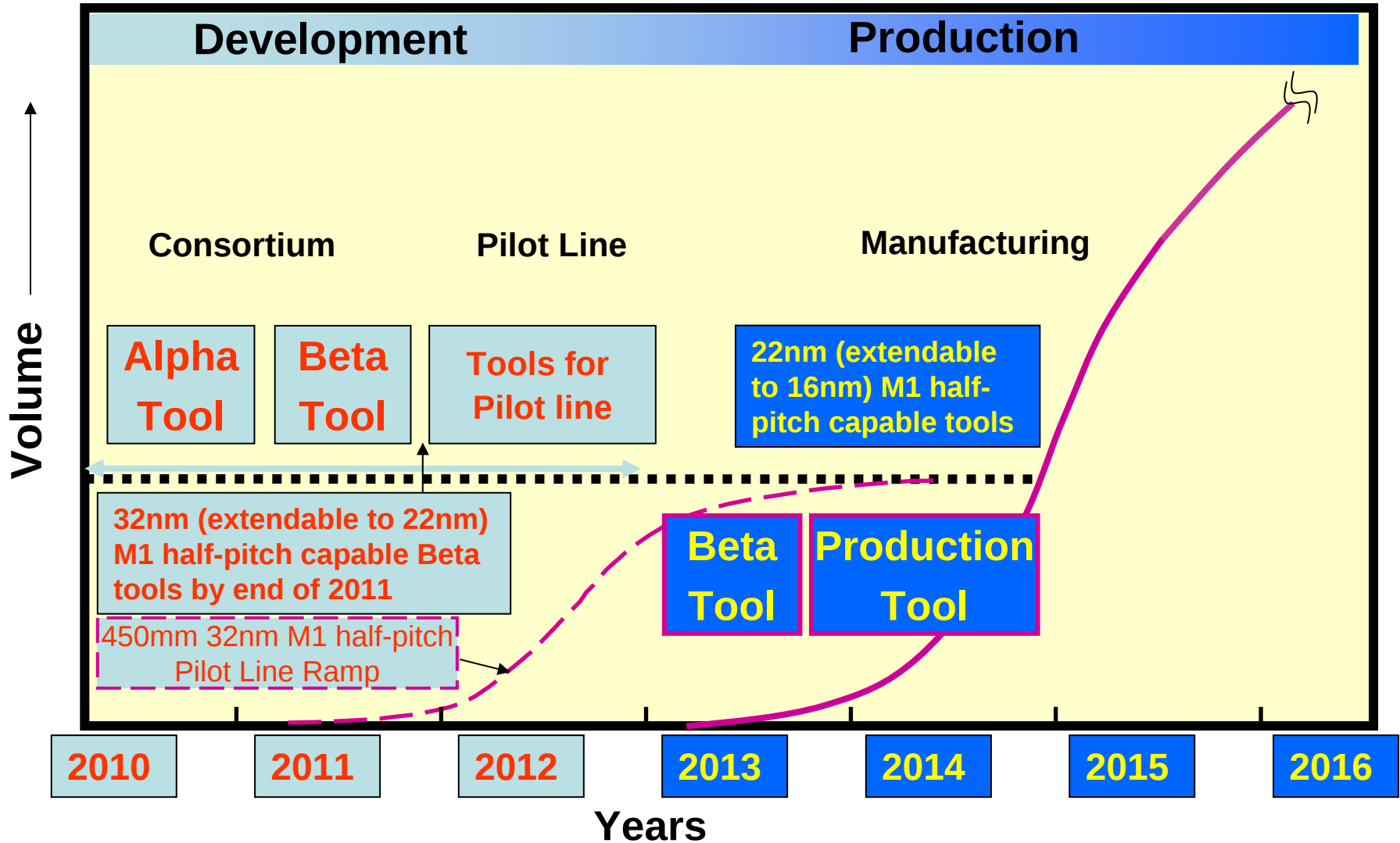
The timing of the production ramp of 450 mm facilities (versus early pilot line capability) depends not only on the mastering of all technical issues, associated with this transition to a new diameter, but also on the preparedness of the industry. To assess the likelihood of that timing, the whole value chain must therefore be examined...”

“...Furthermore, and new in the 2009 ITRS, a 450mm Production Ramp-up Model Graphic has been provided (Figure 2c) to clarify the special dual “S-curve” timing required when a new wafer generation is being introduced [modeled after the experience with the 300mm wafer generation ramp on two succeeding technology cycles in the 2001-2003 (180nm-130nm M1) timeframe]...”

^[1] Source: “May 2008”/ “Oct 2008 ISMI symposium”/Dec’08 ISMI 450mm Transition Program Status Update for ITRS IRC, Seoul, Korea [and also at SEMICON Japan]

450mm Production Ramp-up Model

[2009 Figure 2c A Typical Wafer Generation Pilot Line and Production "Ramp" Curve]



さらに詳しい資料については下記を参照願います

- ・ ITRSの公式ホームページ
 - <http://www.itrs.net/> または <http://public.itrs.net/>
 - ITRS 2007 Edition, 2008 Updateはじめ、ITRSの最新情報
 - ITRS 2009 Edition は2010年1月に公表
- ・ JEITAのロードマップのホームページ
 - <http://strj-jeita.eliasp.net/strj/index.htm>
 - ITRS 2007の日本語訳(過去の版の和訳もあり)
 - ITRSの過去の版(英文)へのリンク
 - STRJ(半導体技術ロードマップ専門委員会)の活動情報