WG5 (リソグラフィWG)活動報告
「NGLの現状と課題」

ルネサスエレクトロニクス（株） 内山 貴之

－内容－

- WG5(リソグラフィWG)の活動体制
- ITRS 2010 updateリソグラフィの概要
- ITRS 2011 改訂の検討状況
- WG5 活動状況
- NGLの現状と課題
- まとめ

略語

NA	Numerical Aperture
CD	Critical Dimension, CDU (CD Uniformity)
DOF	Depth of Focus
LER/LWR	Line Edge Roughness/Line Width Roughness
RET	Resolution Enhancement Techniques
OAI	Off-Axis Illumination
PSM	Phase Shifting Mask cPSM (complementary PSM), APSM (Alternating PSM), EPSM (Embedded PSM), Att. PSM (Attenuated PSM)
EDA	Electronic Design Automation
OPC	Optical Proximity Corrections, RB/MBOPC (Rule Base/Model Base OPC)
DFM	Design for Manufacturing/Design for Manufacturability
SB/SRAF	Scattering Bar/Sub Resolution Assist Feature™
MEEF	Mask Error Enhancement Factor (=MEF)
ARC	Anti-Reflection Coating, BARC (Bottom ARC), TARC (Top ARC)
AMC	Airborne Molecular Contamination
DE	Double Exposure
DP	Double Patterning
SADP	Self Aligned DP
ESD	Electro Static Discharge
NGL	Next Generation Lithography
EUVL	Extreme Ultraviolet Lithography
ML2	Maskless Lithography
NIL	NanoImprint Lithography
UV-NIL	Ultraviolet NIL
SFIL	Step & Flash Imprint Lithography
DSA	Directed Self Assembly

WG5(リソグラフィWG)の活動体制

■JEITA半導体部会/関連会社

- 内山 貴之/ リーダー (ルネサスエレクトロニクス)
- 笹子 勝 / サブリーダー (パナソニック)
- 千々松 達夫/ 事務局(富士通セミコンダクター)
- 東川 巌 (東芝)
- 川平 博一(ソニー)
- 和田 恵治 (ローム)
- 田中 秀仁 (シャープ)
- 山口 敦子 (日立製作所)

■コンソーシアム

- 寺澤 恒男 (Selete)
- 笠間 邦彦 (EUVA)
- *【山部 正樹 (ASET-D2I)】:2010/9までで退任*

■SEAJ、他

- 奥村 正彦/ 国際委員 (SEAJ:　ニコン)
- 高橋 和弘 (SEAJ:　キヤノン)
- 中島 英男 (SEAJ:　TEL)
- 山口 哲男 (SEAJ:　ニューフレアテクノロジー）
- 大久保 靖 (HOYA)
- 林 直也 (大日本印刷)
- 森本 博明（凸版印刷）
- 佐藤 和史 (東京応化工業)
- 栗原 啓志郎 (アライアンスコア)

計　19名

ITRS 2010 update リソグラフィの概要

- Potential Solutions NAND FlashとMPU/DRAMを分割、見直し
- Difficult Challenge 見直し
- カラーリング見直し

等

ITRS 2010 update “Potential Solutions (NAND Flash)”

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	First Year of IC Production	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024
	Flash ½ Pitch (nm) (un-contacted Poly)(f)	*38*	*32*	*28*	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*	*8.9*	*8.0*	*7.1*	*6.3*
32	193 nm Immersion Double Pattern																
22	193 nm Immersion Double Pattern																
16	193nm immersion Multiple Pat																
	EUV							row Option									
	Imprint																
	193nm immersion + DSA																
11	EUV																
	193nm immersion Multiple Pattern																
	Imprint									Narrow Option							
	EUV + DSA																
	Innovative patterning solution																

32nm (2010): 193nm液浸DP

22nm (2013): 193nm液浸DP

NAND Flash Time Line

16nm (2016): 193nm液浸MP
EUV
Imprint
193nm液浸+DSA

11nm (2019): EUV
193nm液浸MP
Imprint
EUV+DSA
Innovative patterning solution

This legend indicates the time during which research, development, and qualification

Research Required
Development Underway
Qualification / Pre-Production
Continuous Improvement

ITRS 2010 update “Potential Solutions (MPU/DRAM)”

First Year of IC Production	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024
DRAM ½ pitch (nm) (contacted)	52	45	40	36	32	28	25	23	20	18	16	14	13	11	10	9
MPU/ASIC Metal 1 (M1) ½ pitch (nm)	54	45	38	32	27	24	21	19	17	15	13	12	11	9.5	8.4	7.5

45
- 193 nm Immersion with water

32
- 193 nm Immersion Double Pattern
- EUV

Narrow Options

22
- EUV
- 193 nm Immersion Double / Multiple Pattern
- ML2 (MPU only)
- Imprint (DRAM only)

Narrow Option

16
- EUV
- 193nm immersion Multiple Pattern
- ML2
- Imprint
- 193nm immersion + DSA

11
- EUV
- ML2
- Imprint
- Litho + DSA
- Innovative patterning solution

Narrow Option

MPU / DRAM time line

45nm (2010): 193nm液浸

32nm (2013): 193nm液浸 DP
EUV

22nm (2016): EUV
193nm液浸DP/MP
ML2(MPU)
Imprint (DRAM)

16nm (2019): EUV
193nm液浸MP
ML2
Imprint
193nm液浸+DSA

11nm (2022): EUV
ML2
Imprint
Litho+DSA
Innovative patterning solution

This legend indicates the time during which research, development, and

Research Required
Development Underway
Qualification / Pre-Production
Continuous Improvement

Work in Progress - Do not publish

ITRS Potential Solutions

NAND Flash	MPU /DRAM	ITRS 2009	ITRS2010 update	
		NAND Flash, MPU/DRAM	NAND Flash	MPU/DRAM
2009 32nm	2013	193 nm-i DP	193 nm-i DP	193 nm-i DP
		EUV (DRAM / MPU)		EUV (DRAM)
2013 22nm	2016	EUV	193 nm-i DP	EUV
		193 nm-i DP/MP		193 nm-i DP/MP
		ML2		ML2 (MPU only)
		Imprint		Imprint (DRAM only)
2016 16nm	2019	EUV	193nm-i MP	EUV
		Innovative 193nm-i MP	EUV	193nm-i MP
		ML2	Imprint	ML2
		Imprint	193nm-i + DSA	Imprint
		Directed Self Assembly		193nm-i + DSA
		Interference Lithography		
2019 11nm	2022	EUV	EUV	EUV
		ML2	193nm-i MP	ML2
		Imprint	Imprint	Imprint
		Directed Self Assembly	EUV + DSA	Litho + DSA
		Interference Lithography	Innovative patterning solution	Innovative patterning solution

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Difficult Challenges ≥ 16 nm

Near term

Optical masks with features for resolution enhancement and post-optical mask fabrication	Equipment infrastructure (writers, inspection, metrology, cleaning, repair) for fabricating masks with sub-resolution assist features Registration, CD, and defect control for masks Eliminating formation of progressive defects and haze during exposure Understanding and achieving the specific signature and specifications for a Double Patterned mask Establishing a stable process so that signatures can be corrected.
Doluble and Multiple Patterning	Overlay of multiple exposures including mask image placement, mask-to-mask matching, and CD control for edges defined by two separate exposures Availability of software to split the pattern, apply OPC, and verify the quality of the split while preserving critical features and maintaining no more than two exposures for arbitrary designs Availability of high productivity scanner, track, and process to maintain low cost-of-ownership Photoresists with independent exposure of multiple passes Fab logistics and process control to enable low cycle time impact that efficient scheduling of multiple exposure passes.
Cost control and return on investment	Achieving constant/improved ratio of exposure related tool cost to throughput over time ROI for small volume products Resources for developing multiple technologies at the same time Cost-effective resolution enhanced optical masks and post-optical masks, and reducing data volume 450 mm diameter wafer infrastructure if at 16nm

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Difficult Challenges ≥ 16 nm (cont’)

Near term

Process control	New and improved alignment and overlay control methods independent of technology option to <5.7 nm 3 overlay error Controlling LER, CD changes induced by metrology, and defects < 10 nm in size Greater accuracy of resist simulation models Accuracy of OPC and OPC verification, especially in presence of polarization effects Lithography friendly design and design for manufacturing (DFM)
EUV lithography	Source power > 180 W at intermediate focus, acceptable utility requirements through increased conversion efficiency and sufficient lifetime of collector optics and source components Cost control and return on investment Resist with < 1.5 nm 3s LWR, < 10 mJ/cm2 sensitivity and < 20 nm ½ pitch resolution Fabrication of Zero Printing Defect Mask Blanks Establishing the EUVL mask Blank infrastructure (Substrate defect inspection, actinic blank inspection) Establishing the EUVL patterned mask infrastructure (Actinic mask inspection, EUV AIMs) Controlling optics contamination to achieve > five-year lifetime Protection of EUV masks from defects without pellicles Fabrication of optics with < 0.10 nm rms figure error and < 7% intrinsic flare

EUVLがNear termに!

Difficult Challenges <16nm

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Long term

EUV lithography - Extendibility	*NA*
	higher Source power
	double patterning at EUV, flare
	Resist
	incident angle
	Different LTEM and absorber material to deal with high source power and heating
Resist materials	Limits of chemically amplified resist sensitivity for < 16 nm half pitch due to acid diffusion length Materials with improved dimensional and LWR control add (limits) Resist and antireflection coating materials composed of alternatives to PFAS compounds Low defects in resist materials (size < 10nm) Line width roughness < 1.4nm 3 sigma
Mask fabrication	Timeliness and capability of equipment infrastructure (writers, inspection, metrology, cleaning, repair) Increasingly long mask write and cycle time Mask process control methods and yield enhancement Cost control and return on investment Required degree of complexity with computational Lithography

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Difficult Challenges <16nm

Long term

Cost control and return on investment	Achieving constant/improved ratio of exposure-related tool cost to throughput Development of cost-effective post-optical masks Cost effective 450mm lithography systems Achieving ROI for small volume products
193 nm Immersion Multilple Patterning	Cost control and return on investment Wafer processing to tighter overlay and CD controls Mask fabrication to tighter specifications Required degree of complexity with computational Lithography Increasing numbers of masks required.
Metrology and defect inspection	Defect inspection on patterned wafers for defects < 20 nm Resolution and precision for critical dimension measurement down to 6 nm, including line width roughness metrology for 0.8 nm 3s Metrology for achieving < 2.8 nm 3s wafer overlay error Template inspection for 1X Imprint Patterned Masks Phase shifting masks for EUV Limits of chemically amplified resist sensitivity for < 16 nm half pitch due to acid diffusion length

Difficult Challenges <16nm

Long term

~~Gate~~ CD control improvements and process control	Development of litho and post litho processes to control gate CD < 1.5 nm 3s with < 1.4 nm 3s line width roughness. Printed, post print process reduction, and final roughness Development of new and improved alignment and overlay control methods independent of technology option to achieve total < 2.8 nm 3s overlay error on products. ~~especially for imprint lithography~~
Maskless Lithography	Wafer Throughput Cost control and return on investment Die-to-database inspection of wafer patterns written with maskless lithography Pattern placement - including stiching Controlling variability between beams in multibeam systems
Imprint Lithography	Defect-free Imprint templates at 1X dimensions Infrastructure for 1X technology Templates (Write, inspection, and repair) Template fabrication to tighter specifications Protection of Imprint templates from defects without pellicles ~~Mask Life time~~ Throughput Cost control and return on investment Overlay Process control methods to compensate for systematic CD and overlay errors

ITRS 2011 改訂の検討状況

- Potential Solutions 見直し
- Difficult Challenge 全面見直し
- カラーリング見直し

等予定

ITRS 2011 update “Potential Solutions (NAND Flash)”

	First Year of IC Production	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024
	Flash ½ Pitch (nm) (un-contacted Poly)(f)	*32*	2010 28 & 25 nm HP		*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*	*8.9*	*8.0*	*7.1*	*6.3*
32	**193 nm Immersion Double Pattern**															
22	**193 nm Immersion Double Pattern**															
16	**EUV**															
	193nm immersion Multiple Pattern					Narrow Options										
	Imprint															
	193nm immersion + DSA															
11	**EUV**															
	193nm immersion Multiple Pattern								Narrow Options							
	EUV + DP															
	Imprint															
	193nm immersion / EUV+ DSA															
	Innovative patterning solution															

Preliminary

NAND Flash Time Line

順位入れ替え

量産化タイミングで見直し

追加

ITRS 2011 update "Potential Solutions (MPU/DRAM)"

	First Year of IC Production	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024
	DRAM ½ pitch (nm) (contacted)	*45*	*40*	*36*	*32*	*28*	*25*	*23*	*20*	*18*	*16*	*14*	*13*	*11*	*10*	*9*
	MPU/ASIC Metal 1 (M1) ½ pitch (nm)	45	38	32	27	24	21	19	17	15	13	12	11	9.5	8.4	7.5
45	193 nm Immersion with water															
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	193nm immersion + DSA															
11	EUV															
	193nm immersion Multiple Pattern															
	ML2															
	Imprint								Narrow Option							
	193nm immersion / EUV+ DSA															
	Innovative patterning solution															

Difficult Challenges (2011 -)

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Preliminary

全面見直し

Equipment / Process	Defect inspection equipment (mask and wafer)
	Mask Write time
	CD / Placement metrology tools
	450mm Wafer Scaling
	Throughput for various litho options
	EUV Source Power
	Development of litho and post litho processes to control CD, line width roughness, and overlay. Printed and post print process to meet design specifications.
	Non Planar substrates such as multilayer NAND
Defects	Native defects / Contamination
	Defect free handling and storage for masks without pellicles
	Pattern Collapse
Mask	Mask Min feature size (MRC restriction)
	Mask CD Control
	1X challenges for Nano Imprint (such as defects, CD, OL)
Multiple Pattering	Total Overlay (exposure tools and Masks)
	Small area high MEEF for DP
	OPC generation and verification for multiple patterning
Resist / Material	Resist Candidates for 16nm node and below
	DSA materialization (from concept to production)
	The need of robust negative resist such as high image contrast for bright field masks

ITRS 2011 改訂ポイント

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- Potential Solutions (long term vs short term)
- Number of masks trend
- Impact of LWR on EUV mask inspection.
- EUV blank surface roughness is not in the spec (actinic and non actinic inspection)
- Imprint LER Litho resist spec
- DSA – Start a new table OR become part of double patterning
- Computational Lithography – Start a new table OR figures
- Data Volume for mask and maskless writers update
- Max in mask write time (for process control and throughput)
- Mask Grid – 0.5nm (0.125nm 1X) or 0.4nm (0.1nm 1X)?

WG5活動状況

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2010年度の活動状況

- ITRS 2010 update/ITRS 2011改訂に向けた取り組み
  - 各テーブルの見直し
  - Potential Solutionsテーブルの見直し
  - ITWG参加・議論

- NGL進捗確認
  (カンファレンス・学会等の最新状況を参加委員から報告)
  - EUVL開発状況
    - 光源パワー、マスクインフラ整備、レジスト開発
      ➔光リソからEUVへの移行時期見極め
  - ML2、Imprint開発の進捗確認

ITRS会議(リソグラフィ)の状況 -STRJのポジション

STRJ

- 経験豊富なメンバーで定期的にF2Fミーティング実施(1回/2ヶ月)
  - LSIメーカの状況や学会・カンファレンス等のリソグラフィ最新情報を元に、ITRSロードマップ作成に寄与

- 日本にはリソの装置・材料メーカが多い ➔各技術の情報が多い
  ➔ITRS策定に多大な寄与
  - マスク全主要メーカ(DNP*/Toppan*/HOYA*)
  - レジスト主要メーカ(TOK*/JSR/住友化学/信越化学/FFEM/etc.)
  - 露光機メーカ2/3社(ニコン*/キヤノン*)
  - 光源(Gigaphoton/USHIO/EUVA*)
  - トラック(TEL*/SOKUDO)
  - CD-SEM(HHT/日立*)
  - EUVブランクス検査技術(Selete*)

*：STRJ-WG5委員

- ITRS会議には1名+αで参加

ITRS会議(リソグラフィ)の状況　-他極の状況

- 米国
  - リソグラフィのリーダー(David Chan氏, SEMATECH)と中心とした活動
  - インターナルで電話会議を実施
- 欧州
  - インターナル会議は実施しない
  - ITRS会議には2~3名参加
- 台湾
  - インターナル会議はなし
  - メンバーは5名
  - リーダーがT. Yen氏(TSMC)に変更になり、ITRS会議の議論に参加
- 韓国
  - 過去1年間ITRS会議(リソ)に欠席のため不明

今年度WG会議でのカンファレンス・学会参加報告、勉強会

- 4/16
  - 参加報告　SPIE Advanced Lithography (2月)、PMJ (4月)
- 6/18
  - 参加報告　Litho Forum (5月)、EIPBN (6月)
- 9/3
  - *勉強会　EUV光源の現状 (笠間委員による特別講演)*
- 10/8
  - 参加報告　SPIE BACUS (9月)、MNE (9月)
- 12/10
  - 参加報告　Int. Symp. EUVL / Litho Ext. (10月)、MNC (11月)、Litho Workshop (11月)
- 2/4
  - *勉強会　波長6.6nmリソ技術 (特別講師　ギガフォトン・溝口様)*

NGLの現状と課題

次世代リソグラフィ技術(NGL)の動向

- EUVL
  - ASML β機NXE:3100の1号機が昨年10月に出荷。
  - 課題はマスクインフラ整備、光源、レジスト。
  - 1x nmではレジストが最大の課題に。
  - 6.6nmリソの基礎検討開始。
- ML2
  - 主にロジック向け用途。
  - MAPPER LithographyのPre-αツールは一昨年出荷されたが、その後の進捗が見えてこない。
  - 装置のスループットが最大の課題。次いで、ビーム補正・検証/ウェハ検査、ビーム安定性・信頼性。
- インプリント
  - 主にメモリ向け用途。最近進捗が見えず。
  - マスク欠陥・コンタミが最大の課題。次いで、アライメント/重ね合わせ精度、露光装置スループット。

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EUVLの現状

- 露光機開発
  - ASML β機 NXE:3100の1号機出荷済み(2010年10月)
    量産機は2012年の予定
  - ニコンの量産機は2014年以降

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EUVLの現状

EUV Focus Areas 2006-2010: 22 nm half-pitch insertion target

SEMATECH

2006 / 32hp	2007 / 22hp	2008 / 22hp	2009 / 22hp	2010 / 22hp
1. Reliable high power source & collector module	1. Reliable high power source & collector module	1. Long-term source operation with 100 W at IF and 5MJ/day	1. Mask yield & defect inspection/review infrastructure	1. Mask yield & defect inspection/review infrastructure
2. Resist resolution, sensitivity & LER met simultaneously	2. Resist resolution, sensitivity & LER met simultaneously	2. Defect free masks through lifecycle & inspection/review infrastructure	2. Long-term reliable source operation with 200 W at IF	1. Long-term reliable source operation with 200 W at IF
3. Availability of defect free mask	3. Availability of defect free mask	3. Resist resolution, sensitivity & LER met simultaneously	3. Resist resolution, sensitivity & LER met simultaneously	2. Resist resolution, sensitivity & LER met simultaneously
4. Reticle protection during storage, handling and use	4. Reticle protection during storage, handling and use	• Reticle protection during storage, handling and use	• EUVL manufacturing integration	• EUVL manufacturing integration
5. Projection and illuminator optics quality & lifetime	5. Projection and illuminator optics quality & lifetime	• Projection / illuminator optics and mask lifetime		

SEMATECH EUVL Symposium 2010

EUVL pilot line insertion in 2011/12 and HVM introduction in 2013

EUV光源の開発進捗が遅延、EUVマスクと並んで#1
光源も大きな課題に

EUVLの現状

2010 EUV Extendibility (11 nm hp) Focus Areas identified

Key Focus Areas	Rank*
Resist materials extendibility / new platforms / image transfer solutions	1.3
Source technology scalability / extendibility	2.2
Mask technology extendibility (defects, materials)	2.3
Overlay requirements / CD control / metrology	not ranked
Infrastructure development / manufacturing integration	not ranked
Cost of Ownership	not ranked

SEMATECH EUVL Symposium 2010

*) Average of 25 steering committee member votes

1x nmに向けてはレジストが最大の課題

EUVLの現状

- 光源開発
  - サイマーのLPP光源開発が遅延。現状の実用パワーは単体で14~20W@IFレベル。ウシオのDPP、ギガフォトンのLPPが追う状況。2011年Q2~Q3の目標が100W@IF (➔60WPH相当)。

ASML

ASML社報告・NXE3100用光源ロードマップ

ASML's Presentation by Rard De Leeuw
ET-01 "EUV into production with ASML's NXE platform"

		LPP		DPP	
Timing	Source Configuration	Expose Power	Throughput	Expose Power	Throughput
Q3/2010	Integration	1W	<1wph	3W	2wph
Q4/2010	Integration	7W	4wph	15W	10wph
Q1/2011	Upgrade 1	40W	25wph	65W	35wph
Mid 2011	Upgrade 2	100W	60wph	100W	60wph

EUVA EUVA CONFIDENTIAL 2 2010.10.17～21 EUV Symposium Kobe International Conference Center

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EUVLの現状

光源

EUV光源ベンチマーク(2010 EUV Symposium, Kobe)

Suppliers	Type	SoCoMo Performance: Performance at plasma /2πsr	Performance at IF	Average power at IF	Level of integration	Operating time	Plan: Mid/2011
Cymer	Sn LPP	LT-1@Cymer 525W	175W (Calc.Raw)	1.75W(Raw) (Duty 1%)	PrePulse No Collector	1.5hrs	β-tool(HVM1) 200W(Raw) 100W (Exposure) Output power ~1/2 due to Dose-Control & SPF
		HVM1@Cymer 90W	15W (Exposure)	6W(Exposure) (Duty 40%)	Full-DMS w 5sr	~100hrs	
		HVM1@ASML 60W	10W (Exposure)	1W(Exposure) (Duty 10%)	Full-DMS w 5sr	~200hrs	
Gigaphoton Komatsu EUVA	Sn LPP	ETS 75W	26W (Calc.Raw)	2.6W(Raw) (Duty 10%)	Snドロプレット (60μmφ) No Collector	9hrs	PPT; 50-188W(Raw, Duty 50-75%)
		ETS 197W	104W (Calc.Raw)	21W(Raw) (Duty 20%)		<1hr	PPT; under development
XTREME Ushio EUVA	Sn LA-DPP	ADT 170W	8W	8W	Full-DMS Full-SoCoMo	Years	β-tool 180W(Exposure Duty 100%)
		β 640W	14.7W (Exposure.) 51W (Predicted. Exposure)	14.7W(Exposure) 51W(Predicted, Exposure) (Duty100%)	Full-DMS Full-SoCoMo	Many Months (14MJ~ 3500wafer)	

EUVA CONFIDENTIAL

21 EUV Symposium Kobe International Conference Center

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EUVLの現状

- マスクインフラ整備
  - EUVL用マスク検査装置
    - マスクブランクス欠陥検査装置(Actinic inspection)
    - パターン欠陥検査装置
      DUV光/EBを用いた検査装置開発中
    - EUV-AIMS (Aerial Image Measurement System)
      [EUV転写像測定装置] ➔ Carl Zeissが開発中
  - EMI (EUV Mask Infrastructure)プログラム
    [SEMATECH]により加速(6社)
  - EUV導入に積極的なLSIメーカはCaptive mask shop を保有し、EUVマスク開発を促進。Merchant mask shop*にとってEUVマスクビジネスは不透明な状況。

    *: DNP, Toppan, HOYA等

EUVLの現状

- レジスト開発
  - RLS(解像度/LER/感度)トレードオフに加え、レジストパターン倒れが課題。解像度は変形照明により2x nmまで。1x nmには届かず。
  - LWRは下層プロセスやリンスプロセスで改善。

まとめ

- ITRS Potential Solutionsリソグラフィ技術の動向
  - MPU/DRAM向け
    - 45nm hp (2010年): ArF液浸シングル露光
    - 32nm hp (2013年): ダブルパターニングまたはEUV
  - NAND Flash向け
    - 32 ~22 nm hp(2010~2013年): スペーサー型ダブルパターニング
  - 16nm hp のNAND Flash、22nm hp のDRAM/MPUにEUVLが有力視 (2016年)

- NGLの現状と課題は下記の通り。
  - EUVL： マスクインフラだけでなく、光源も大きな問題に。
    - β機が昨年10月に出荷開始。今後の開発加速を期待。
    - 1x nm以降のEUVLの最大の課題はレジスト。
  - ML2： スループットが最大の課題。
    - 主にロジック向け用途。
    - MAPPER LithographyがPre-αツールを一昨年出荷済みだが進捗見えず。
    - ビーム補正・検証/ウェハ検査、ビーム安定性・信頼性も課題。
  - インプリント： 欠陥が最大の課題。
    - 最近進捗が見えず。
    - マスク欠陥・コンタミが最大の課題。次いで、重ね合わせ精度、スループット。
  - リソグラフィコスト高騰が大問題に。
    - 特に開発費はコンソーシアム等の有効活用で効率アップしていく流れに。