

STRJ WS 2012

# WG6 (PIDS及びRF&AMS)の活動報告 – 2012年版の内容と2013年版の状況 –

2013年3月8日金曜日

11:45–12:10 (20+5分)

WG6主査: 若林整(東京工業大学)

## Agenda

### ■STRJ WG6活動の紹介

### ■ITRS

#### ● PIDS

◆ 2011→2012年版変化点

◆ 2013年版の方針

#### ● RF & A/MS

◆ 2011→2012年版変化点

◆ 2013年版の方針

# 用語集

- PIDS  
(**P**rocess **I**ntegration, **D**evelopments, and **S**tructures)
  - Logic
    - ◆ HP: High Performance
    - ◆ LOP: Low-Operating Power
    - ◆ LSTP: Low-Standby Power
  
    - ◆ FD-SOI: Fully-Depleted Silicon-on-Insulator
    - ◆ MG: Multi Gates, FinFET, Tri-gates等の総称
    - ◆ Ge: Germanium, ゲルマニウム
    - ◆ III-V: III属-IV属化合物半導体
    - ◆ Vdd: 電源電圧
    - ◆ Ion: ON時駆動電流
    - ◆ Wfp: Wfootprint, 投影トランジスタ幅
    - ◆ Tr.: Transistor
    - ◆ DIBL: Drain Induced Barrier Lowering
    - ◆ SS: Sub-threshold Slope
  - Memory
    - ◆ SRAM: Static Random Access Memory
    - ◆ DRAM: Dynamic Random Access Memory
    - ◆ RCAT: Recessed-Channel Transistor
    - ◆ STT-MRAM: Spin-Torque Transfer Magnetic RAM
    - ◆ PCRAM: Phase-Change RAM
    - ◆ FeRAM: Ferro-electric RAM
    - ◆ RTN: Random Telegraph Noise
  - Reliability
- RF&AMS  
(Radio Frequency & Analog/Mixed-Signal)
  - Low-noise amplifier (LNA)
  - Voltage-controlled oscillator (VCO)
  - Power amplifier (PA)
  - Analog-to-digital converter (ADC)
  - Serializer-Deserializer (SerDes)
  - HV: High Voltage
  - CIS: CMOS Image Sensor

# 2012年度、WG6メンバー構成

主査:若林整(東工大) 副主査/国際:井上裕文(東芝) 幹事:久本大(日立)

| SWG                                                                | SSWG        | 委員                                                                   | 特別委員                                                                             | オブザーバー           |
|--------------------------------------------------------------------|-------------|----------------------------------------------------------------------|----------------------------------------------------------------------------------|------------------|
| PIDS<br>(Process<br>Integration,<br>Devices,<br>and<br>Structures) | Logic       | 尾田秀一(ルネエレ)<br>倉田創<br>(富士通セミコン)                                       | *若林整(東工大)<br>吉見信(SOITEC Asia)<br>井田次郎(金工大)<br>平本俊郎(東大)<br>高木信一(東大)<br>赤坂 泰志(TEL) | 野田泰史<br>(パナソニック) |
|                                                                    | Memory      | *井上 裕文(東芝)<br>岩本邦彦(ローム)                                              | 杉井寿博(LEAP)<br>笠井直記(東北大)                                                          | 五寶 靖<br>(パナソニック) |
|                                                                    | Reliability | *最上徹(PETRA)                                                          | 丹羽正昭(東北大)                                                                        |                  |
| RF & AMS<br>(Radio Frequency &<br>Analog/Mixed-Signal)             |             | *久本 大(日立)<br>竹下光明(ソニー)<br>大黒達也(東芝)<br>林喜宏(ルネエレ)<br>二木俊郎<br>(富士通セミコン) | 田中 徹(東北大)                                                                        |                  |

# 2012年度、WG6活動

## ■ 国際会議

- オランダ (4月): 平本特別委員
- San Francisco (7月): 井上委員(国際), 竹下委員
- 台湾 (12月): 井上委員(国際), 赤坂特別委員

## ■ 国内会議: 6回

- ヒアリング(下表)

| 講演者(敬称略) | 御所属 | 題目                                         | 日にち   | 分野名         |
|----------|-----|--------------------------------------------|-------|-------------|
| 松澤昭      | 東工大 | Analog回路技術                                 | 5/16  | RF&AMS      |
| 大黒達也     | 東芝  | High-RF & A/MS<br>planar MOSFET and FinFET | 7/6   | RF&AMS      |
| 高宮真      | 東大  | 低電圧化の限界に挑む<br>ロジック回路設計技術                   | 8/17  | Logic       |
| 杉林直彦     | NEC | スピントロニクス素子を使ったLSI                          | 11/15 | Memory      |
| 大野泰夫     | 徳島大 | GaN電子デバイス                                  | 12/18 | RF&AMS      |
| 菊地克弥     | 産総研 | 三次元LSI集積実装技術                               | 3/5   | Reliability |

# PIDS構成

## ■ ロジック

Table PIDS6

*Comparison of HP, LOP, LSTP, and III-V/Ge Technologies*

|                            | HP | LOP                | LSTP               | III-V/Ge |
|----------------------------|----|--------------------|--------------------|----------|
| Speed ( $I/CV$ )           | 1  | 0.5                | 0.25               | 1.5      |
| Dynamic power ( $CV^2$ )   | 1  | 0.6                | 1                  | 0.6      |
| Static power ( $I_{off}$ ) | 1  | $5 \times 10^{-2}$ | $1 \times 10^{-4}$ | 1        |

## ■ メモリ

### ● DRAM

### ● NVM

#### ◆ 3端子電荷蓄積型FET

□ 浮遊ゲート (NOR and NAND)

□ 電荷トラップ (NOR and NAND)

#### ◆ 2端子非電荷蓄積型

□ FeRAM, PCRAM, MRAM, STT-MRAM

## ■ 信頼性

# PIDS章の修正点、2011→2012

## ■ 1社判断化と各社公表により修正

## ■ ロジック

- FD-SOIの導入を1年前倒し
- FinFETの導入を3年前倒し
- 2026年の $L_g \sim 6\text{nm}$ まで微細化可能とした。

## ■ メモリー

- Japan PIDSによる調査を追加実施
- DRAMにおいて、縦Tr.による $4F^2$  cellの1年遅延
- NAND/FeRAMの微調整

## ■ 信頼性: 変更なし

# FD-SOIとMulti-gatesの前倒し

## ■ FD-SOI: 1年前倒し

- ST-Ericsson/ST-Microelectronics/GF

## ■ Tri-gates: 3年前倒し

- Intel 22 nm

## ■ HP, LOP, LTSPで同様の対応

Table PIDS2 High-performance (HP) Logic Technology Requirements

2011 HP

| Year of Production                                      | 2012  | 2013  | 2014  | 2015  | 2016  | 2017  | 2018  | 2019  | 2020  | 2021  | 2022  | 2023  | 2024  | 2025  | 2026  |
|---------------------------------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| $L_g$ : Physical Lgate for HP Logic (nm) [1]            | 22    | 20    | 18    | 17    | 15.3  | 14.0  | 12.8  | 11.7  | 10.6  | 9.7   | 8.9   | 8.1   | 7.4   | 6.6   | 5.9   |
| $I_{d,sat}$ : NMOS Drive Current ( $\mu A/\mu m$ ) [14] |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |
| Extended Planar Bulk                                    | 1,367 | 1,422 | 1,496 | 1,582 | 1,670 | 1,775 |       |       |       |       |       |       |       |       |       |
| FD SOI                                                  |       | 1,475 | 1,530 | 1,591 | 1,654 | 1,717 | 1,791 | 1,847 | 1,942 |       |       |       |       |       |       |
| MG                                                      |       |       |       | 1,628 | 1,685 | 1,744 | 1,805 | 1,858 | 1,916 | 1,976 | 2,030 | 2,087 | 2,152 | 2,228 | 2,308 |

Revised for 2012 update

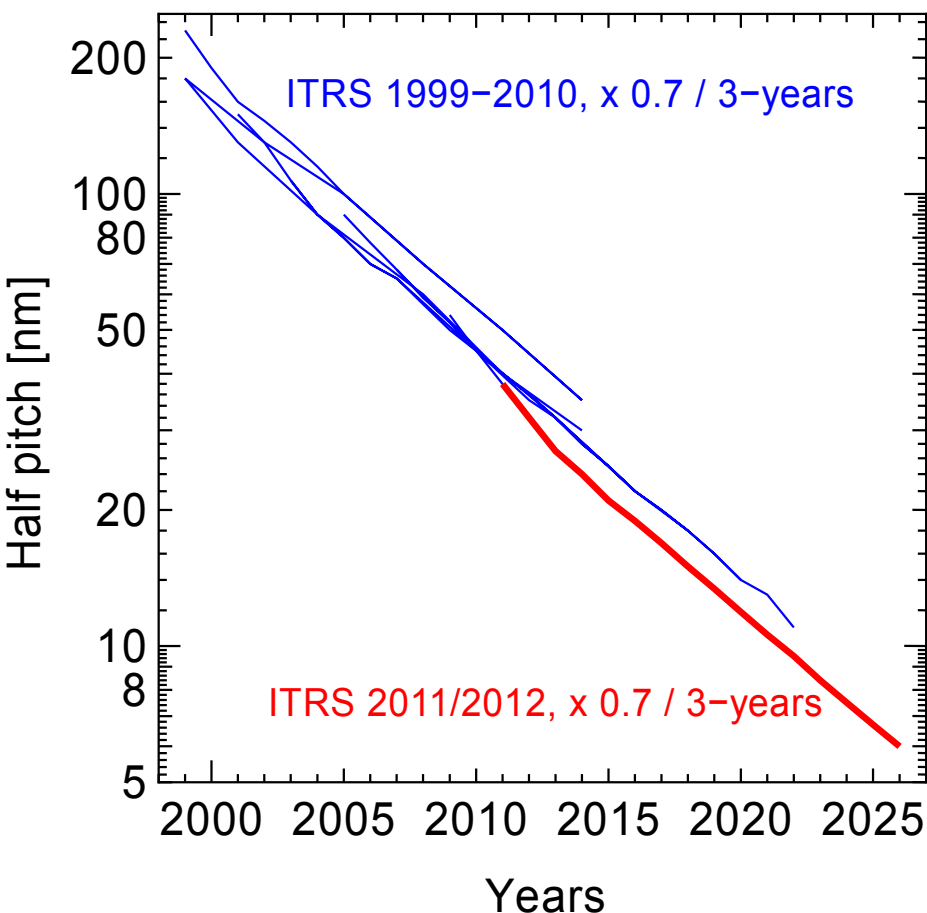
2012 HP

| Year of Production                                      | 2012  | 2013  | 2014  | 2015  | 2016  | 2017  | 2018  | 2019  | 2020  | 2021  | 2022  | 2023  | 2024  | 2025  | 2026  |
|---------------------------------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| $L_g$ : Physical Lgate for HP Logic (nm) [1]            | 22    | 20    | 18    | 17    | 15.3  | 14.0  | 12.8  | 11.7  | 10.6  | 9.7   | 8.9   | 8.1   | 7.4   | 6.6   | 5.9   |
| $I_{d,sat}$ : NMOS Drive Current ( $\mu A/\mu m$ ) [14] |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |
| Extended Planar Bulk                                    | 1,367 | 1,422 | 1,496 | 1,582 | 1,670 | 1,775 |       |       |       |       |       |       |       |       |       |
| FD SOI                                                  | 1,415 | 1,475 | 1,530 | 1,591 | 1,654 | 1,717 | 1,791 | 1,847 | 1,942 |       |       |       |       |       |       |
| MG                                                      | 1,469 | 1,520 | 1,573 | 1,628 | 1,685 | 1,744 | 1,805 | 1,858 | 1,916 | 1,976 | 2,030 | 2,087 | 2,152 | 2,228 | 2,308 |

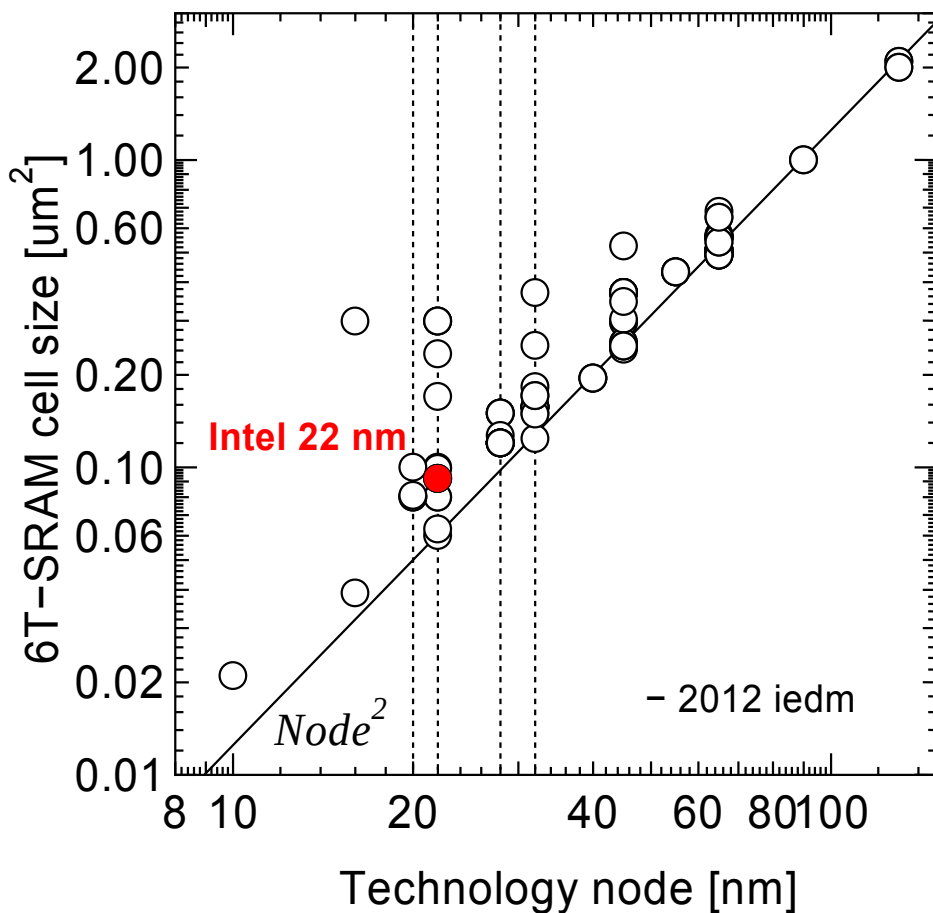
追加

# 微細化による面積削減の進捗

## ■ ITRSの要請



## ■ 6T-SRAM面積低減 Benchmark





# Intel 22-nm-node SoC

■ iedm 2012, 3.1.

■ Tri-gate FET @ 0.75 V

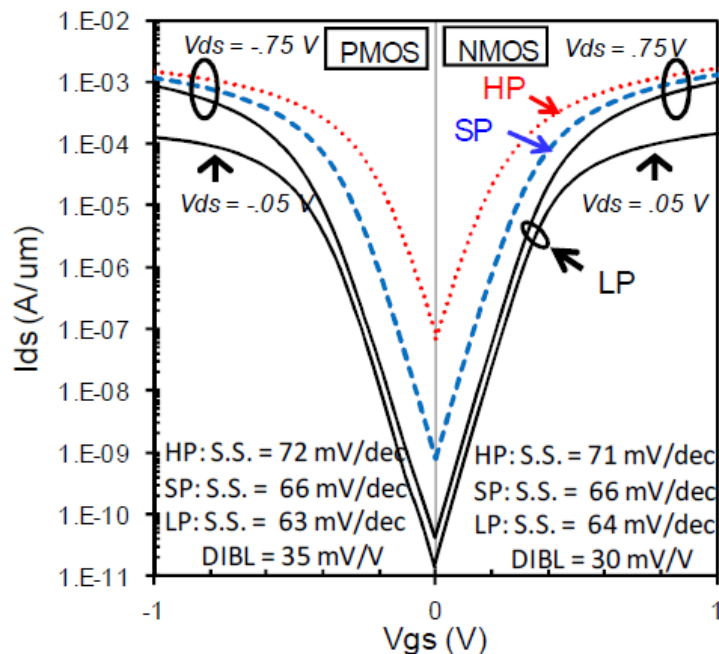
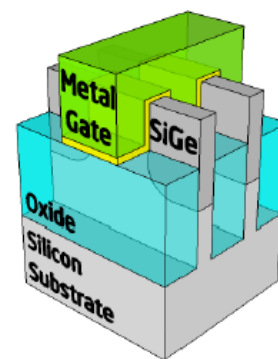
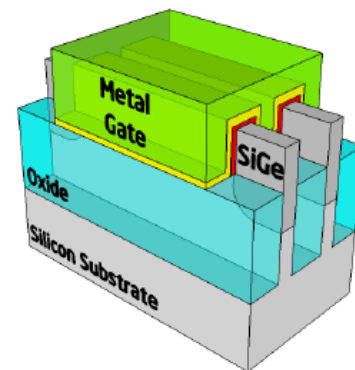


Fig. 5.  $I_{ds}$ -vs.- $V_{gs}$  characteristics showing steep subthreshold and low DIBL, especially for LP transistors ( $< 65$  mV/dec S.S. and  $< 40$  mV DIBL)



(a) High Speed (HP/SP) and Low Power Logic (LP/ULP)



(b) High Voltage (TG)

Fig. 1. 22 nm SoC Tri-Gate transistor families, including high speed logic (HP/SP), low power logic (LP/ULP) and high voltage (TG)

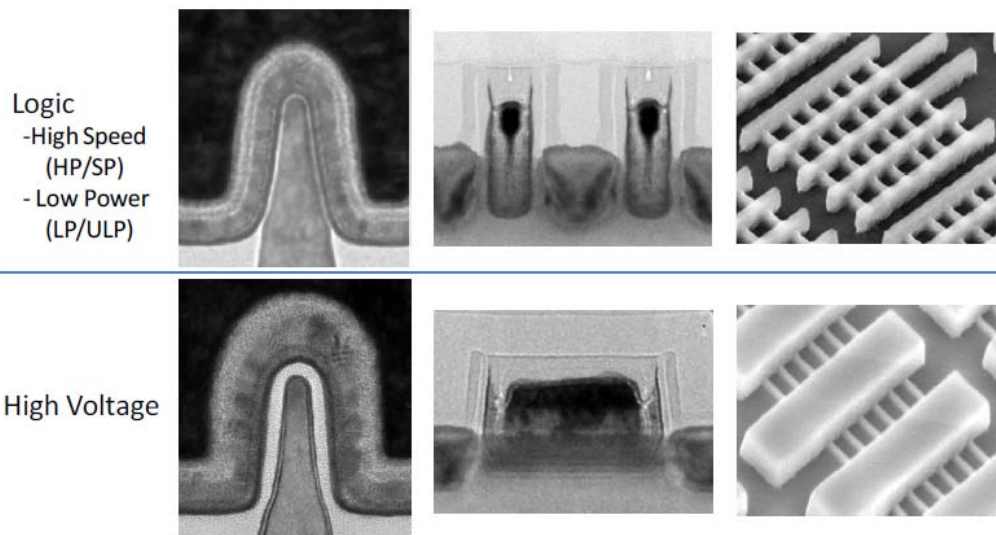
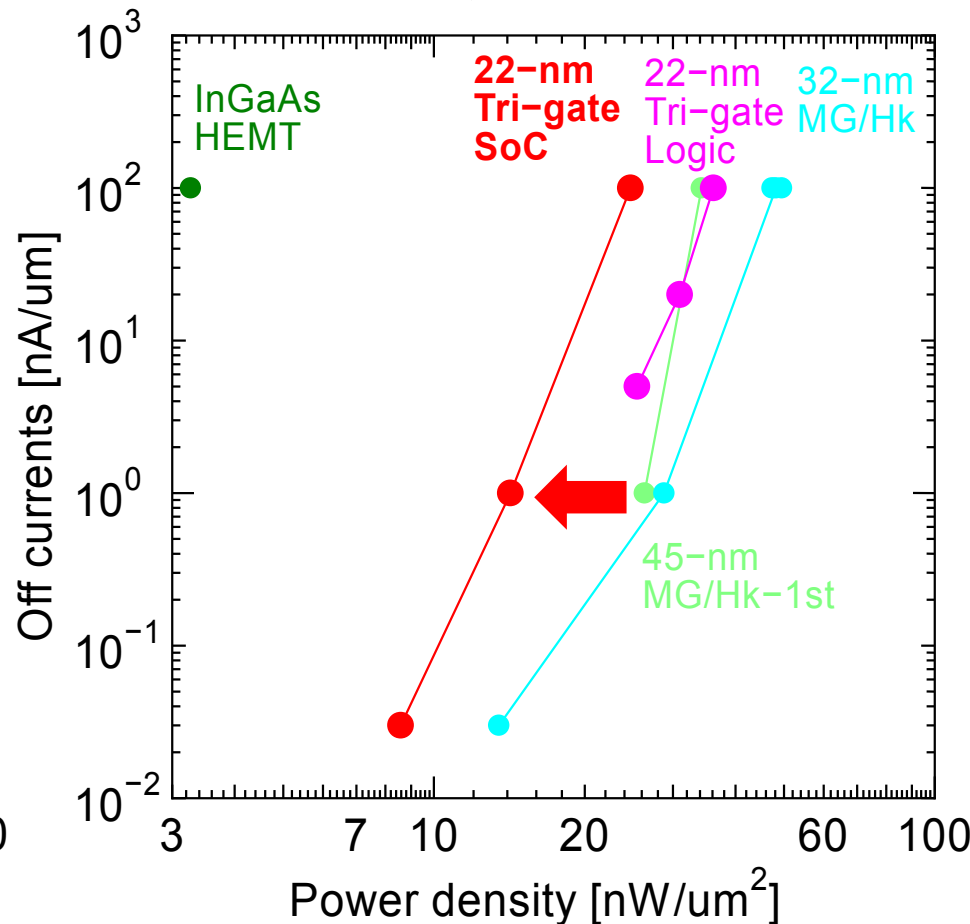
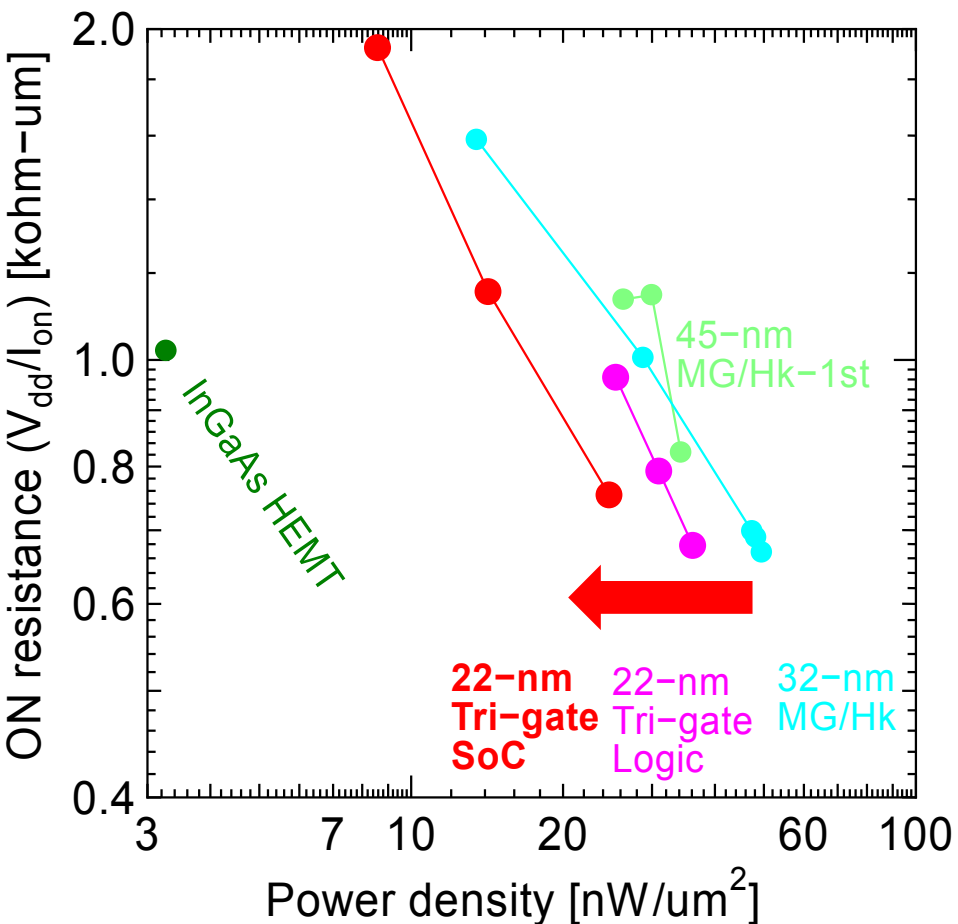


Fig. 2. Fin cut TEM, gate cut TEM, and tilted SEM of logic thin gate (top) and high-voltage thick-gate (bottom) transistors

# Tri-gates性能のBenchmark

- Tri-gate FETにより高速化と低電力化を両立
- Logic (VL12) → SoC (iedm12)でMulti-OxidesプロセスによりFin幅が低減し、DIBL/SS (短チャネル効果)改善



# DRAM, 2011→2012

- Japan PIDSによる調査を基礎に修正
- (Saddle-) FinFETからRCAT+FinFET表記へ
- Vertical Channel Transistor (VCT)による $6F^2 \rightarrow 4F^2$  cellの1年遅延と2026年までの継続

| Table PIDS7 |                  | DRAM Technology Requirements |          |          |      |      |      |      |      |      |      |      |      |      |      |      |      |
|-------------|------------------|------------------------------|----------|----------|------|------|------|------|------|------|------|------|------|------|------|------|------|
|             |                  | Year in Production           | 2012     | 2013     | 2014 | 2015 | 2016 | 2017 | 2018 | 2019 | 2020 | 2021 | 2022 | 2023 | 2024 | 2025 | 2026 |
|             | <i>ITRS 2012</i> | DRAM ½ Pitch (nm) [1]        | 31       | 28       | 25   | 22   | 20   | 18   | 16   | 14   | 13   | 12   | 11   | 10   | 9    | 7    | 6    |
| <b>WAS</b>  | <i>ITRS 2011</i> | DRAM cell FET structure [6]  | FinFET   | VCT      | VCT  | VCT  | VCT  | VCT  | VCT  | VCT  | VCT  | VCT  | VCT  | VCT  | VCT  |      |      |
| <b>IS</b>   | <i>ITRS 2012</i> |                              | RCAT+Fin | RCAT+Fin | VCT  | VCT  | VCT  | VCT  | VCT  | VCT  | VCT  | VCT  | VCT  | VCT  | VCT  | VCT  | VCT  |
| <b>WAS</b>  | <i>ITRS 2011</i> | Cell Size Factor: a [11]     | 6        | 4        | 4    | 4    | 4    | 4    | 4    | 4    | 4    | 4    | 4    | 4    | 4    | 4    | 4    |
| <b>IS</b>   | <i>ITRS 2012</i> |                              | 6        | 6        | 4    | 4    | 4    | 4    | 4    | 4    | 4    | 4    | 4    | 4    | 4    | 4    | 4    |

# DRAM cell Tr.構造例

## ■ RCAT+Fin: Saddle-Fin

- Symp. on VLSI Tech. 2006, T5-1.
- RCAT: Recessed-Ch. Tr.

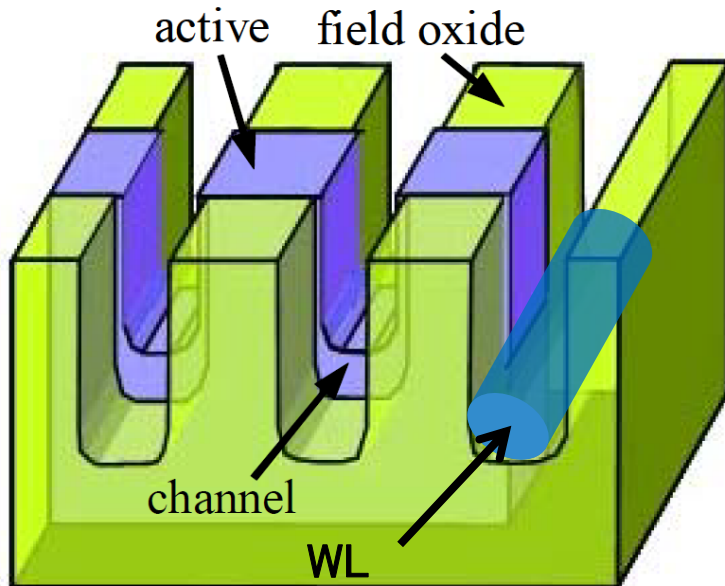


Fig. 1. Schematic diagram of S-Fin. The groove like RCAT and fin structure to the channel width direction are formed.

## ■ VCT: Vertical Channel Transistor

- ESSDERC 2011, p. 211.
- ◆ VPT (Vertical Pillar Tr.)

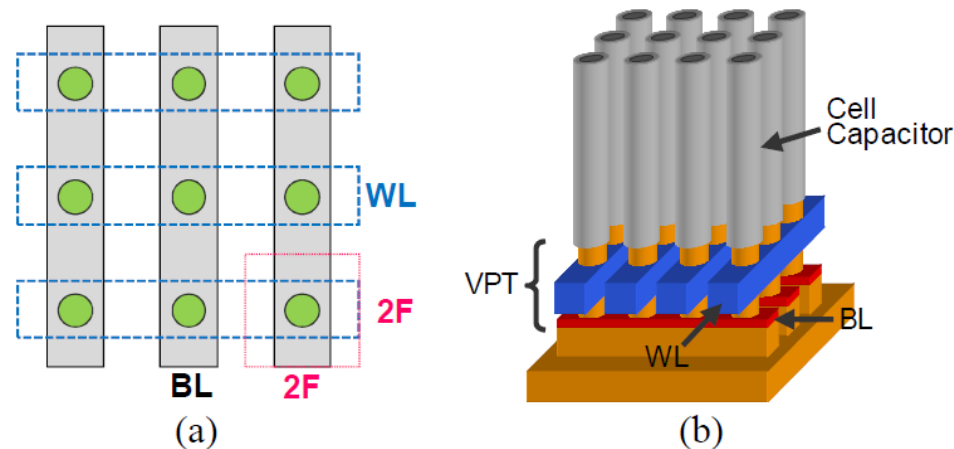


Figure 2. (a)  $4F^2$  cell layout, (b) Schematic diagram of VPT  $4F^2$  cell array

# NAND Flash, 2011→2012

■ PIDS Japanによる調査よりHalf pitch変更無

■ FG: Floating gate, CT: Charge Trap

| Year of Production                                                                                                                                                           |        | 2011   | 2012   | 2013   | 2014   | 2015   | 2016   | 2017   |        |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| Planar (2D) NAND Flash uncontacted poly 1/2 pitch – F (nm) [1]                                                                                                               |        | 22     | 20     | 18     | 17     | 15     | 14     | 13     |        |
| Number of word lines in one NAND string [2]                                                                                                                                  |        | 64     | 64     | 64     | 64     | 64     | 64     | 64     |        |
| Dominant Cell type (FG, CT, 3D, etc.) [3]                                                                                                                                    |        | FG     | FG     | FG     | FG/CT  | FG/CT  | CT-3D  | CT-3D  |        |
| 3D NAND number of memory layers (A range is given since layer number depends on device type, array architecture and choice of poly 1/2 pitch of a specific 3D approach.) [4] |        |        |        |        |        |        | 4-32   | 8-64   |        |
|                                                                                                                                                                              | 2018   | 2019   | 2020   | 2021   | 2022   | 2023   | 2024   | 2025   | 2026   |
|                                                                                                                                                                              | 12     | 11     | 10     | 9      | 8      | 8      | 8      | 8      | 8      |
|                                                                                                                                                                              | 64     | 64     | 64     | 64     | 64     | 64     | 64     | 64     | 64     |
|                                                                                                                                                                              | CT-3D  | CT-3D  | CT-3D  | CT-3D  | CT-3D  | CT-3D  | CT-3D  | CT-3D  | CT-3D  |
|                                                                                                                                                                              | 16-128 | 16-128 | 32-256 | 32-256 | 48-392 | 48-392 | 48-392 | 64-512 | 64-512 |

# CT-3D構造の有力候補

■ **Bit Cost Scalable (BiCS)** technology

■ Symp. on VLSI Tech. 2007, T2-2.

■ Pipe-shaped BiCS Flash memory

■ Symp. on VLSI Tech. 2007, T7-1.

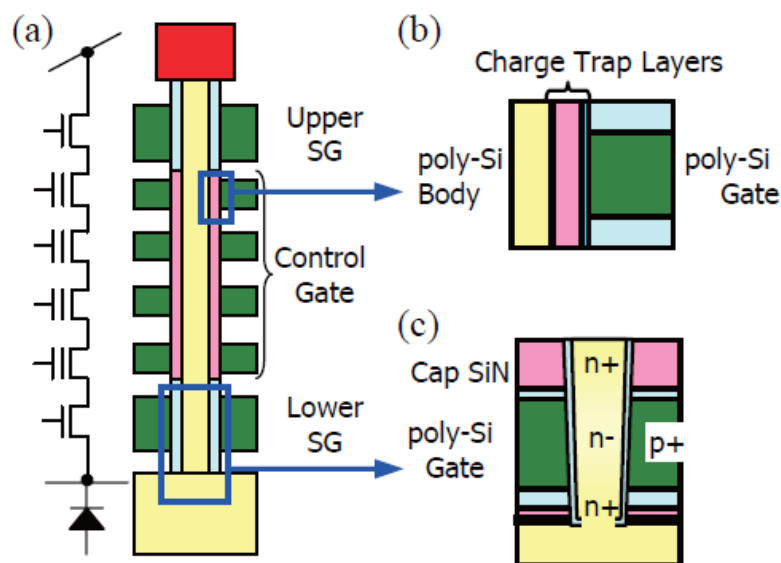


Fig. 6 (a) Cross section of BiCS flash memory string, (b) Cross section of vertical SONOS cell, (c) Cross sections of vertical FET.

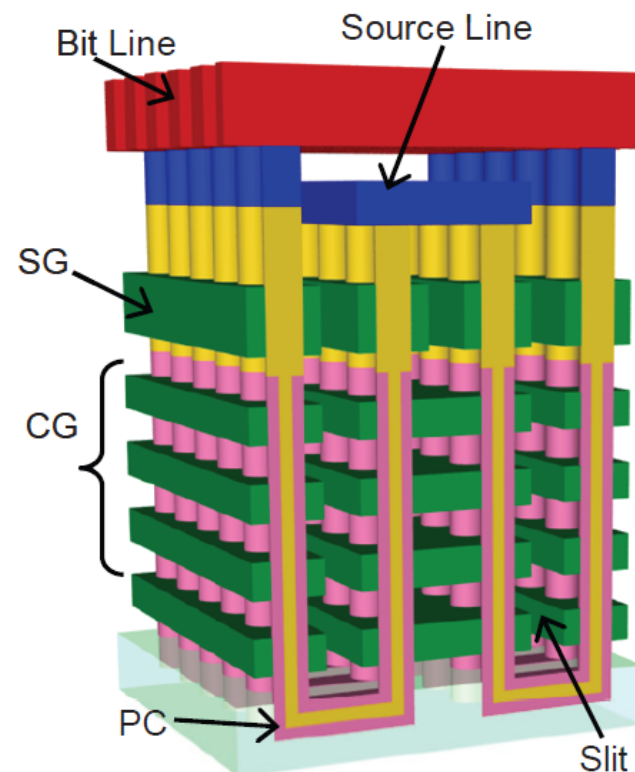


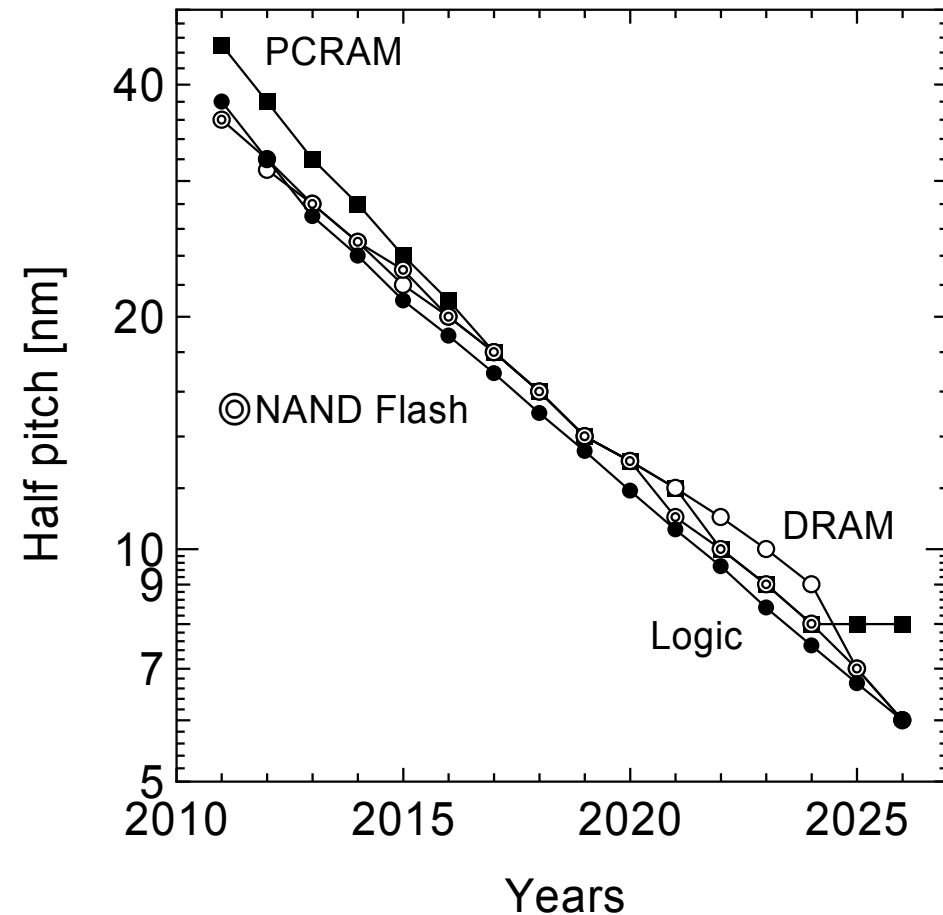
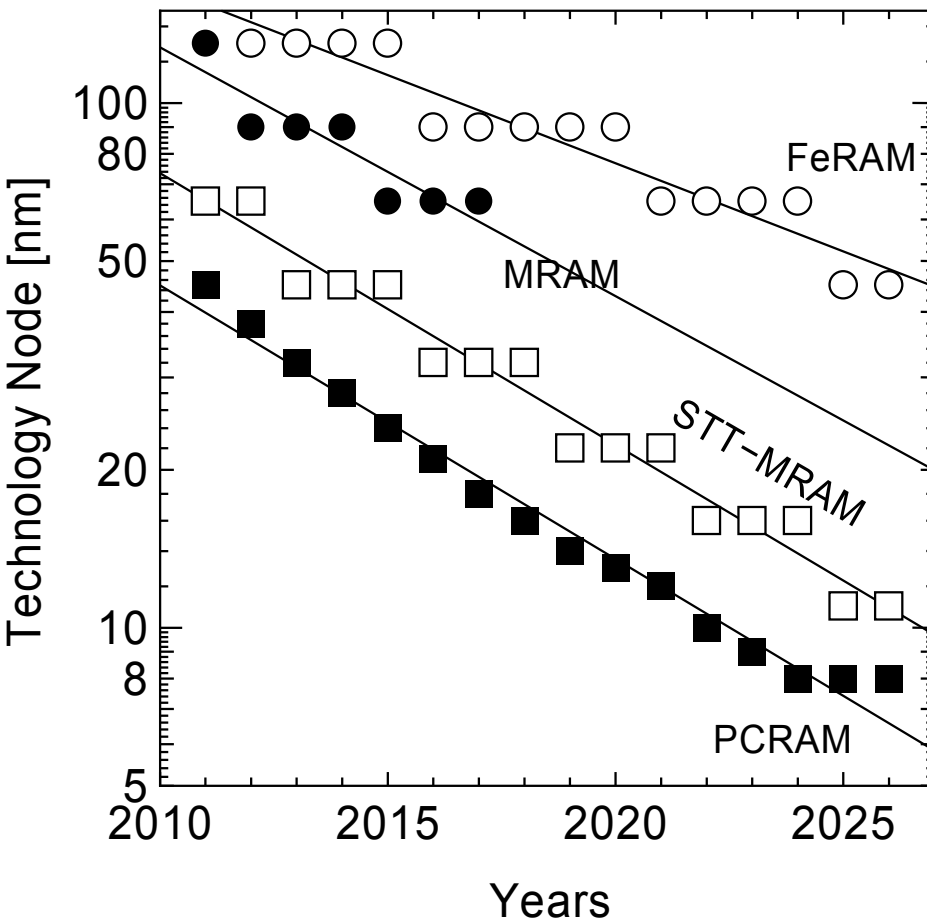
Fig. 1 Schematic of P-BiCS flash memory.



# PIDSデバイスの微細化比較

■ 新規NVMでは  
PCRAMが先行

■ Logicが牽引



# PIDS 2013年版の予定

## ■ ロジック

- クロック周波数増加ペースを13%/年から(8%/年程度に)鈍化させ、電源電圧・駆動時消費電力を低減
  - ◆ LOPを削除。LSTP→Low Power (LP)に改名
- FinFETの御利益を表現するため、ON抵抗( $V_{dd}/I_{on}/W_{\text{footprint}}$ )導入を検討: 日本提案
- MASTARに加えてPurdue大TCAD (nanoHUB)で予測
  - ◆ Tools及びFilesを公開化
- 長期的にはコンパクトモデル導入と回路シミュレーションを検討

## ■ メモリ

- 新規メモリのPIDS Table掲載可否決定予定

## ■ 信頼性

- 新材料・構造やLSIアプリ依存等で発生する可能性のある信頼性課題に注目

## ■ PIDS Chair交代

- Kwok Ng (SRC) → Mustafa Badaroglu (imec)



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## FEATURED



A Gentle Introduction to Nanotechnology and Nanoscience - in Online Presentations



Timothy Sands, Purdue University - Contributions: 11



Illinois ECE 440: Introduction to Crystal Properties Homework - in Teaching Materials



Boundary conditions in N-AlGaAs-pGaAs heterojunction - asked by Anonymous, in Answers

## NOTABLE QUOTE

*Questions and answers sections provided me with more than answers. They really got me interested in researching better.*

David A. Saenz, Purdue University (2012) - in Notable Quotes

## NEW IN RESOURCES

[Illinois] MCB 493 Lecture 4: Chapter 4 in Online Presentations, Mar 05, 2013

[Illinois] ECE 416 Lecture 17: SPR Sensors III in Online Presentations, Mar 05, 2013

ECE 695A Lecture 21: Introduction to Dielectric Breakdown

# RF & A/MS, 2011→2012

## ■ 基本的に2011を踏襲

### ● Device領域変更無

◆ CMOS: PIDS/Logic章を基礎にLayoutと寄生RCを考慮

◆ Si Bipolar

◆ III-V

◆ On-Chip Passives

◆ HV MOS

### ● System Driver章を 念頭に各デバイスの Figure of Merits (FOM)を明確化

◆ LNA, VCO, PA, ADC, SerDes

◆ 回路レイアウトも考慮

| Analog - Carrier Frequency Bands |                        |                                     |                    |
|----------------------------------|------------------------|-------------------------------------|--------------------|
| LF Analog<br>(0.0 GHz-0.4 GHz)   | RF<br>(0.4 GHz-30 GHz) | Millimeter-Wave<br>(30 GHz-300 GHz) | THz<br>(> 300 GHz) |
| Example applications             |                        |                                     |                    |
| Automotive controls              | Cellular               | 60 GHz point-to-point               | No products yet    |
| On-chip regulators               | WLAN                   | Imaging                             |                    |
| Power management                 | SerDes                 | Automotive radar                    |                    |
|                                  | ADC, DAC               | Wireless backhaul                   |                    |

Figure RFAMS1 Analog and Carrier Frequency Bands and Example Applications considered in formulating this Roadmap

# RF & A/MS, 2013年版の予定

## ■ Device領域

- High-Speed Bipolar

  - ◆ BEOL寄生インピーダンスを考慮し、大幅改訂予定

- HVMOS/Passive: メンバー募集中

## ■ 応用領域

- 高耐圧デバイスの検討

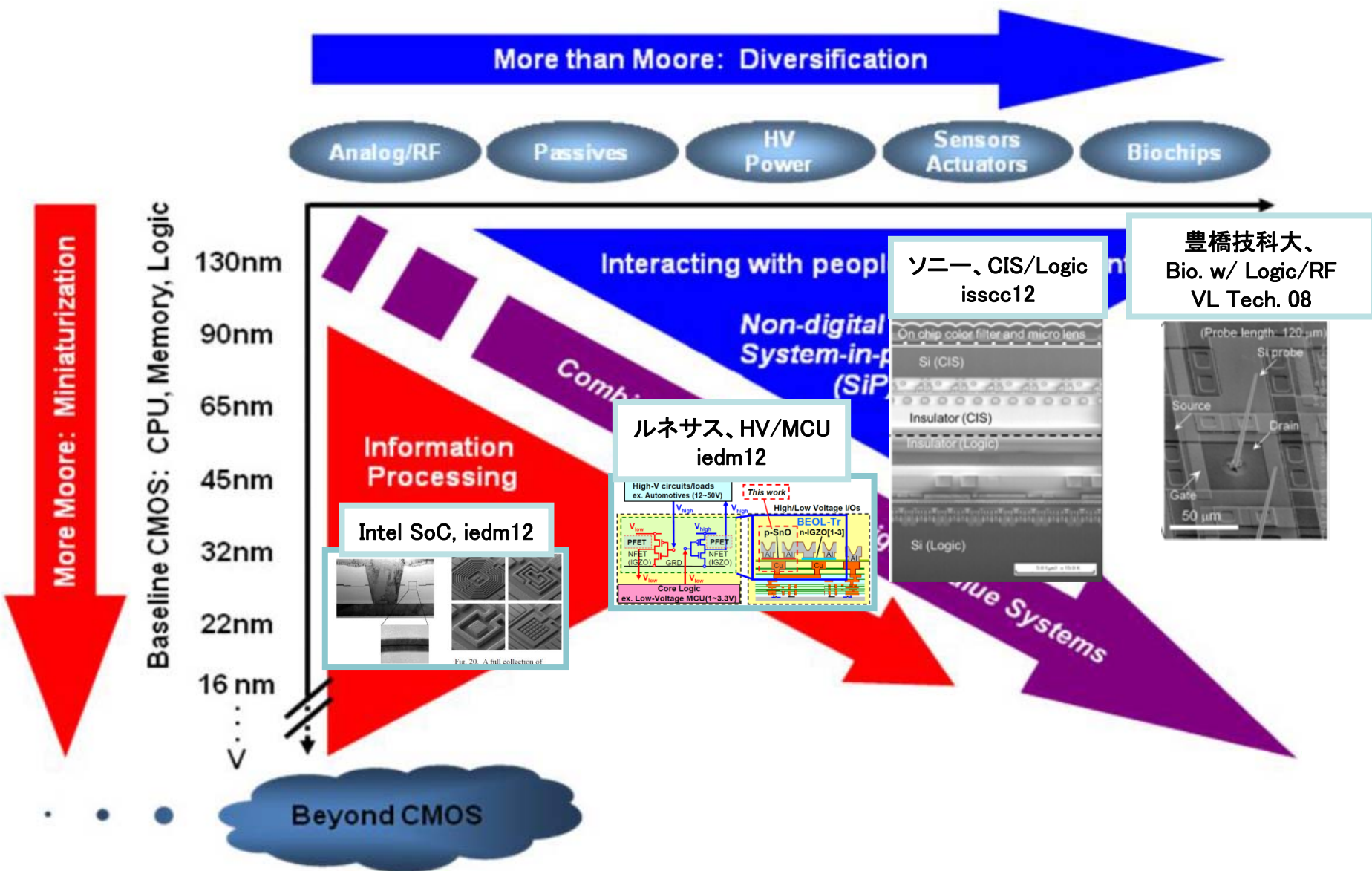
- 医療用途における異種Chip統合低消費電力化の検討

- THz imaging応用の検討

- 自動車用レーダーの評価

- RoadmapによるMore than Mooreデバイスへの貢献を評価予定

# More Moore + More than Moore



# まとめ

- WG6 (PIDS及びRF&AMS)の活動を報告した。
- 2013年度: WG6主査交代予定
- 今後に向けた提言
  - JEITA会員であるChip/Module企業のFab-light化に対応するため、STRJ WG6の活動形態・意義について議論を進める必要がある。